

EBIS Accelerator Controls Hardware Interface Design

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Power Supply Interface

The power supplies located on the EBIS platforms, as well as those associated with the Ion sources, LEBT, MEBT, HEBT, and LINAC, will be controlled through the use of Power Supply Interfaces (PSI). High-speed PSIs, which can generate analog functions at rates as fast as 100,000 setpoints per second, communicate with a VME based Function Generator (V233) module. Low-speed PSIs will be used to produce DC type reference point settings, and are controlled using a VME based Power Supply Controller (PSC) board. A PSI is primarily used to control a single power supply. However, a PSI can be configured to control two power supplies in a “push-pull” arrangement. In this case the PSI generates two analog outputs, one being a negative image of the other. For example, if one output is set to +3.5 volts, the other is set to -3.5 volts. Both high-speed and low-speed PSIs utilize fiber optic communication links, providing isolation between them and their associated controllers. This allows each PSI to be located on any voltage platform, close to its associated power supply. The characteristics of the analog and digital I/O signals of the PSI are defined in a separate document.

PSCs provide individual setpoint type control with limited readback capability, and are used for power supplies that do not require any type of sophisticated or lengthy setpoint function in order to operate. Each PSC has six independent channels, allowing it to communicate with up to six low-speed PSIs simultaneously. The PSC also provides operational commands (on, off, standby) to its assigned power supplies.

Utilizing its on-board memory, a V233 can send a series of consecutive setpoints, called a function. New setpoint are clocked out every 10 microseconds. The V233 is also PPM (Pulse-to-Pulse Modulation) compatible, capable of managing up to eight users. In addition, each user’s setpoint memory is double-buffered, allowing a new function to be downloaded while the current function is being transmitted. Readback data, typically comprised of an echoed setpoint, a power supply status word, and four digitally represented analog measurements, is stored in double-buffered memory as well. This allows data to be collected by the front-end processor after each cycle, without interrupting the data collection process of the present cycle. Each V233 has four independent channels, allowing it to communicate with four high-speed PSIs simultaneously. The V233 also provides operational commands (on, off, standby) to its assigned power supplies.

Every V233 is equipped with an Event Link decoder, which provides the means to start, stop, and generate a function in synchronization with other V233s. Each channel of every V233 derives its setpoint clock (100,000Hz) from the Event Link itself, which operates at 10MHz.

Figure 1 on the next page is block diagrams depicting the fiber optic interconnections between a V233 and four PSIs. Figure 2 shows the possible connections between a PSI and a power supply.

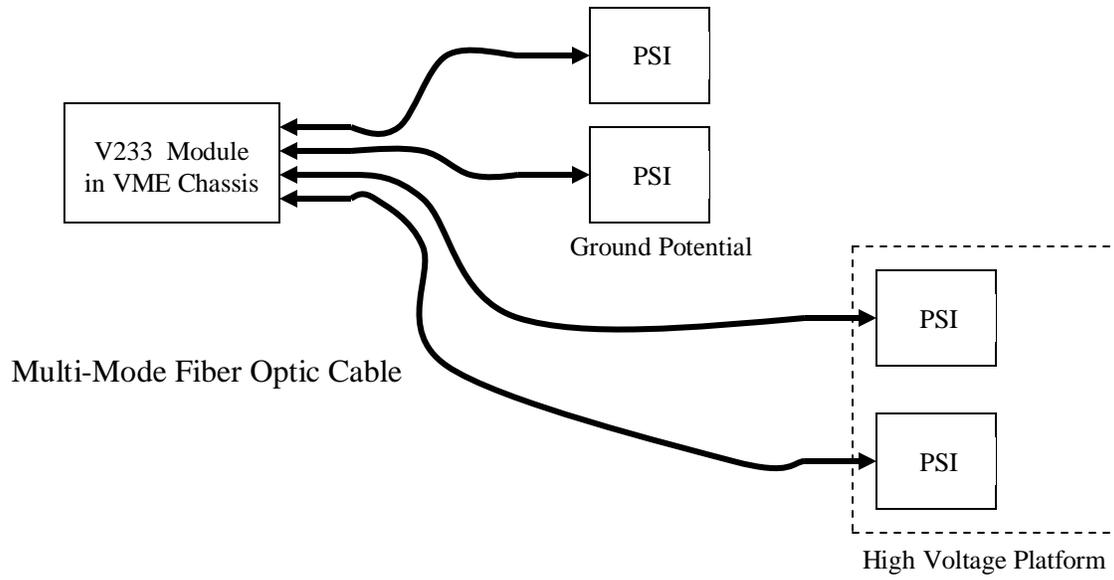


Figure 1. Typical V233 – PSI Connection

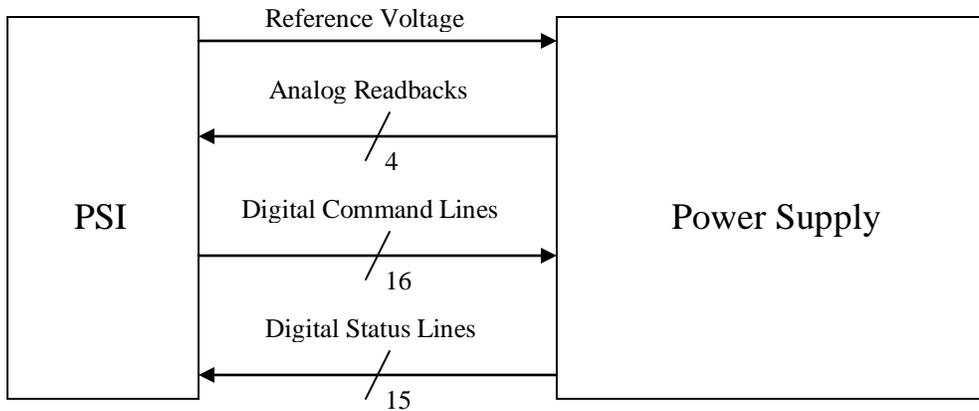


Figure 2. Possible PSI – Power Supply Interface

The EBIS design has a total of 163 power supplies requiring PSI type control. The PSI locations, corresponding numbers, and types are shown in Table 1 below.

Table 1

Control	EBIS Platforms	LEBT & ION Sources	MEBT	HEBT	LINAC
PSI/PSC – Single Output	6	21	8	22	4
PSI/PSC – Push-Pull	0	8*	0	0	0
PSI/V233 – Single Output	29	7	0	0	0
PSI/V233 – Push Pull	8*	17*	0	0	0

** Each PSI has complemented analog outputs for controlling two power supplies in a “push-pull” configuration.*

Many of the components within EBIS, LEBT, and the Ion Sources are capable of being switched at a 5Hz rate. The power supplies used in these areas will be controlled using a V233/High-Speed PSI combination. There are other elements that will not or cannot be switched at 5Hz, including those downstream of EBIS. Those power supplies will employ a PSC/Low-Speed PSI combination.

The amount of data that may be transferred to and from a V233 makes it impractical to have more than six or seven of them in any one chassis, so they will be evenly distributed within three VME crates. These will be referred to as EBIS Power Supply Control Chassis 1, 2 and 3. The transfer line power supplies, controlled strictly by PSI/PSC combinations, will have its their own chassis. This will be referred to as the Transfer Line Power Supply Control Chassis.

Seven power supplies downstream of LEBT are “pulsed” type supplies, each requiring a trigger to initiate a current pulse. This initiating trigger will be the same for all seven power supplies. In addition, external triggers are used by the PSCs to acquire readbacks at prescribed times. These trigger requirements will be satisfied by adding one Delay Module (V202) and two Fan Out Modules (V294) to the Transfer Line Power Supply Control Chassis.

One additional V202 module will be added to each EBIS Power Supply Control Chassis to provide PSC triggers, as well as miscellaneous maintenance, testing, and troubleshooting capability. As an example, V202 output pulses are synchronized to events, and may be used for triggering an oscilloscope at a precise time.

A V202 has eight individual channels that produce output pulses. Each channel can be programmed to trigger upon the occurrence of specific events on an Event Link. The output pulse can be delayed from the trigger point, and the length of the pulse is can be varied as well. Just as the V233, the V202 is PPM compatible, capable of managing up to eight users.

The V294 is used to fan out, or make copies, of TTL level input signals. It is configurable as far as the number of inputs and outputs it can accommodate, with a maximum of twelve total outputs.

Each power supply control chassis will also contain one Motorola Processor Module (MVME3100-1152), one Memory Module (MM6702CN-4M, and one Utility Module (V108). Tables listing the itemized boards in each power supply control chassis are shown below.

Table 2. EBIS Power Supply Control Chassis 1 Modules

Processor	MVME3100-1152	1
Memory Module	MM6702CN-4M	1
Utility Module	V108	1
Function Generator	V233	6
Power Supply Controller	PSC	2
Delay Module	V202	1

Table 3. EBIS Power Supply Control Chassis 2 Modules

Processor	MVME3100-1152	1
Memory Module	MM6702CN-4M	1
Utility Module	V108	1
Function Generator	V233	5
Power Supply Controller	PSC	2
Delay Module	V202	1

Table 4. EBIS Power Supply Control Chassis 3 Modules

Processor	MVME3100-1152	1
Memory Module	MM6702CN-4M	1
Utility Module	V108	1
Function Generator	V233	5
Power Supply Controller	PSC	2
Delay Module	V202	1

V294
V294
V202
Open
Open
Open
PSC
Open
V108
Memory Module
Processor

Figure 6. Transfer Line Power Supply Control Chassis

Table 6. Equipment Summary For Power Supply Control

VME Chassis	TBD	4
Processor	MVME3100-1152	4
Memory Module	MM6702CN-4M	4
Utility Module	V108	4
Function Generator	V233	16
Delay Module	V202	4
Fan Out Module	V294	2
PSC	520	12
High-Speed PSI/Single Output	TBD	36
High-Speed PSI/Push-Pull	TBD	25
Low-Speed PSI/Single Output	TBD	61
Low-Speed PSI/Push-Pull	TBD	8

Timing Trigger Signals

Discrete pulsed timing triggers are required for various EBIS apparatus and functions, such as switching, ion injection, and data acquisition. These timing signals must be well synchronized, with each other as well as all the controls. Furthermore, these timing signals must be distributed to various EBIS locations and voltage platforms, in a rather noisy environment, necessitating good isolation. This will be accomplished through the use of a fiber optic distribution system. Timing trigger signals are generated as standard TTL level signals. They are converted to light signals, and transmitted optically to their various destinations. Once there, the signals will be converted back to TTL, and driven by 50-ohm drivers to their final destinations.

A dedicated V233, located in the VME timing trigger chassis, will be used to generate 32 channels of timing triggers. Instead of transmitting setpoints serially to a PSI, channel 1 and channel 2 of this V233 will take each value read from setpoint memory, latch it into a 16-bit parallel buffer, and present the bits on the VME P2 backplane connector. The result is 32 individual digital channels, with each channel played out from a bit position in memory at a rate of 100KHz. Instead of loading the channel 1 and channel 2 memory with setpoint tables, the memory is loaded with timing trigger tables, constructed in such a way that the table will play out the desired string of binary 1's and 0's. In this way, a timing trigger channel can be programmed to provide a pulse stream having single or multiple pulses, with pulses of varying widths. The resolution of the start and duration of any pulse is 10 microseconds. In addition, because the V233's memory is double-buffered, a new timing trigger table can be downloaded while the current table is being played out. New tables can be made active upon the occurrence of a specific event.

There are a few instances, such as the injection trigger, where it will be necessary to have better timing resolution than the 10 microseconds provided by the timing triggers generated by the V233. In these cases, timing triggers will be used as external triggers to a V202, also located in the timing trigger chassis. Once triggered, the output pulse of a V202 can have its delay and width resolved down to 100 nanoseconds, providing a sort of "fine tuning" for the trigger signals. Two V202s will be available for this purpose, each having the capacity to accept up to four external triggers, thus providing eight "fine tuned" trigger signals.

Every V233 channel, whether it is used for setpoints or timing triggers, can be synchronized to start transmitting its data at the same time, through the use of a common event. Furthermore, each channel clocks out its data using a 100KHz clock derived from the same Event Link decoded by all V233s. The 100KHz clocks of all V233s are re-synchronized at the start of every function. Because of this ability to synchronize V233s, timing trigger pulses can be programmed to occur at any desired point in relation to the setpoint functions also being generated. When users are changed or tables are swapped, the synchronization between V233s is maintained.

Below is an example how to use a channel's timing trigger table in a V233 to generate 16 channels of timing triggers. Bit column D0 of the timing trigger table (memory) translates to Timing Trigger Channel 1, the D1 column is Channel 2, and so on. A small section of programmed memory and the resultant timing trigger channels are shown in Figure 7 below.

V233 Timing Trigger Table

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Address 0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	Address 1
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	Address 2
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	Address 3
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	Address 4
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Address 5

Resultant Timing Triggers

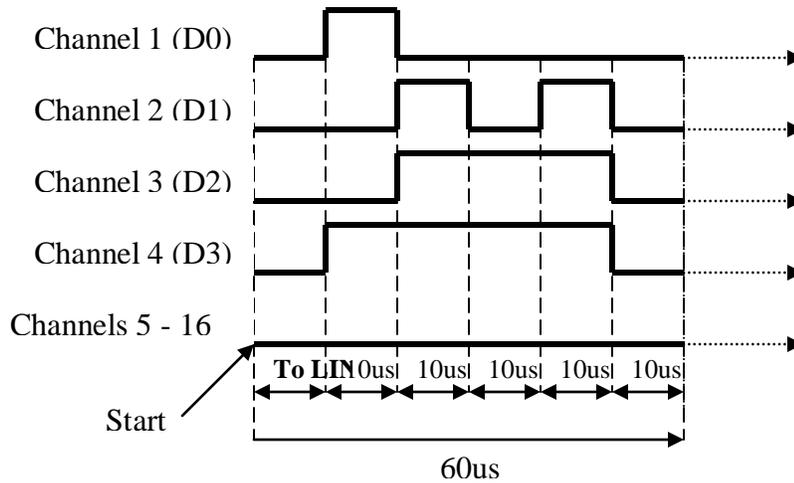


Figure 7

Pulsed Output Signals

In addition to the timing triggers described in the earlier section, there is a need for additional pulsed output signals generated by Delay Modules (V202). These modules will be located in the timing trigger chassis, and are in addition to the V202s described in the previous section, used to “fine tune” timing trigger outputs

The additional pulsed signal requirements are as follows:

Vacuum Shutters:	10
Emittance Measurements:	3
Ion Sources (3):	6

The nineteen signals listed above require three additional V202 boards. One of these V202s will have its outputs (8) converted to light, and transmitted to a high voltage platform.

Timing Trigger And Pulsed Output Signal Distribution

The timing triggers and pulsed output signals will be fanned out and distributed to equipment located on the various voltage platforms within the EBIS facility. The signals are generated by modules installed in the VME Timing Trigger chassis, located in a rack residing at normal ground potential. The signals are distributed on the VME backplane through the use of VME Overlay Modules, attached to the other side of the backplane's P2 connectors. These Overlay Modules perform the same function as ribbon cables, but provide controlled impedance, greater noise and crosstalk immunity, and a good mechanism for signal termination.

To deliver the timing trigger signals and pulsed output signals to remote destinations, the signals will be converted to light and driven across multi-mode fiber optic cables. This method of signal distribution serves several purposes. It allows the signals to be driven long distances, provides good noise immunity, and provides the isolation necessary for the signals to be sent to platform areas that are at different voltage potentials. The conversion of electrical signals to light will be provided by newly designed and built 8-channel Fiber Optic/50 Ohm Driver modules. Each Fiber Optic/50 Ohm Driver module (V195) will receive a group of eight TTL level timing trigger input signals on the VME P2 connector, and convert them to eight fiber optic outputs available on the module's front panel. In addition, each of the eight timing triggers will be fed into a 50-ohm line driver, also available on the front panel of the V195 module. These 50-ohm electrical outputs will be used primarily for local monitoring.

Individual multi-mode fiber cables will be used to carry the light signals to their various locations and platforms. Two spare cables to each unique voltage platform will also be provided. The fiber optic connector of choice will be the standard ST type connector.

After the timing trigger signals are delivered fiber optically to their various destinations, they must be converted back to electrical signals. The Fiber-to-TTL Converter, an adaptation of an existing fiber optic module design (V185), will be designed and built in tandem with the V195. The Fiber-to-TTL Converter will be housed in a 19-inch rack-mountable box, a standard 1U in height. Each unit will handle four channels, and will be equipped with an internal AC-to-DC power supply. These units will accept DC level fiber optic signals and convert them to standard electrical TTL 50-ohm outputs, available on front panel LEMO type connectors. Eighteen of these units are required to handle the signal distribution demands.

Once the light signals are converted back to electrical signals, they can be connected to their intended devices with individual 50-ohm compatible cables, provided by the user. These signals must have a 50-ohm termination to ground at the load.

Table 7 shows the itemized boards in the timing trigger chassis, and Figure 8 shows the chassis layout. Figure 9 is a block diagram of the signal distribution system.

Table 7. Timing Trigger Chassis Modules

Processor	MVME3100-1152	1
Memory Module	MM6702CN-4M	1
Utility Module	V108	1
Function Generator	V233	1
Fiber Optic/50 Ohm Driver Module*	V195	8
Delay Module	V202	5

Figure 8. Layout of Timing Trigger VME Chassis

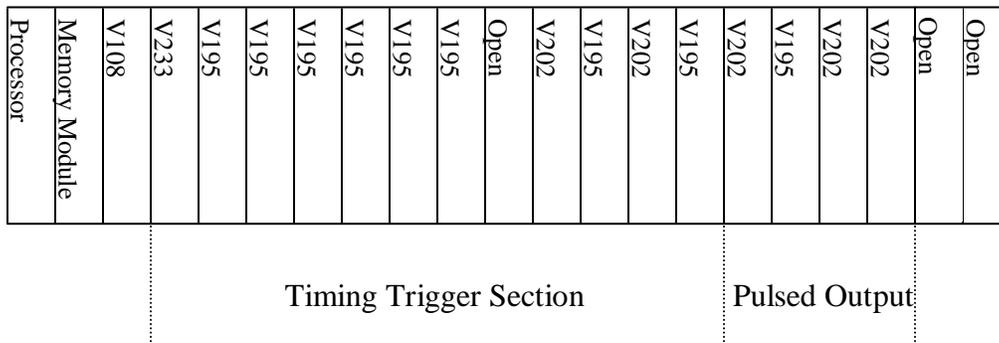
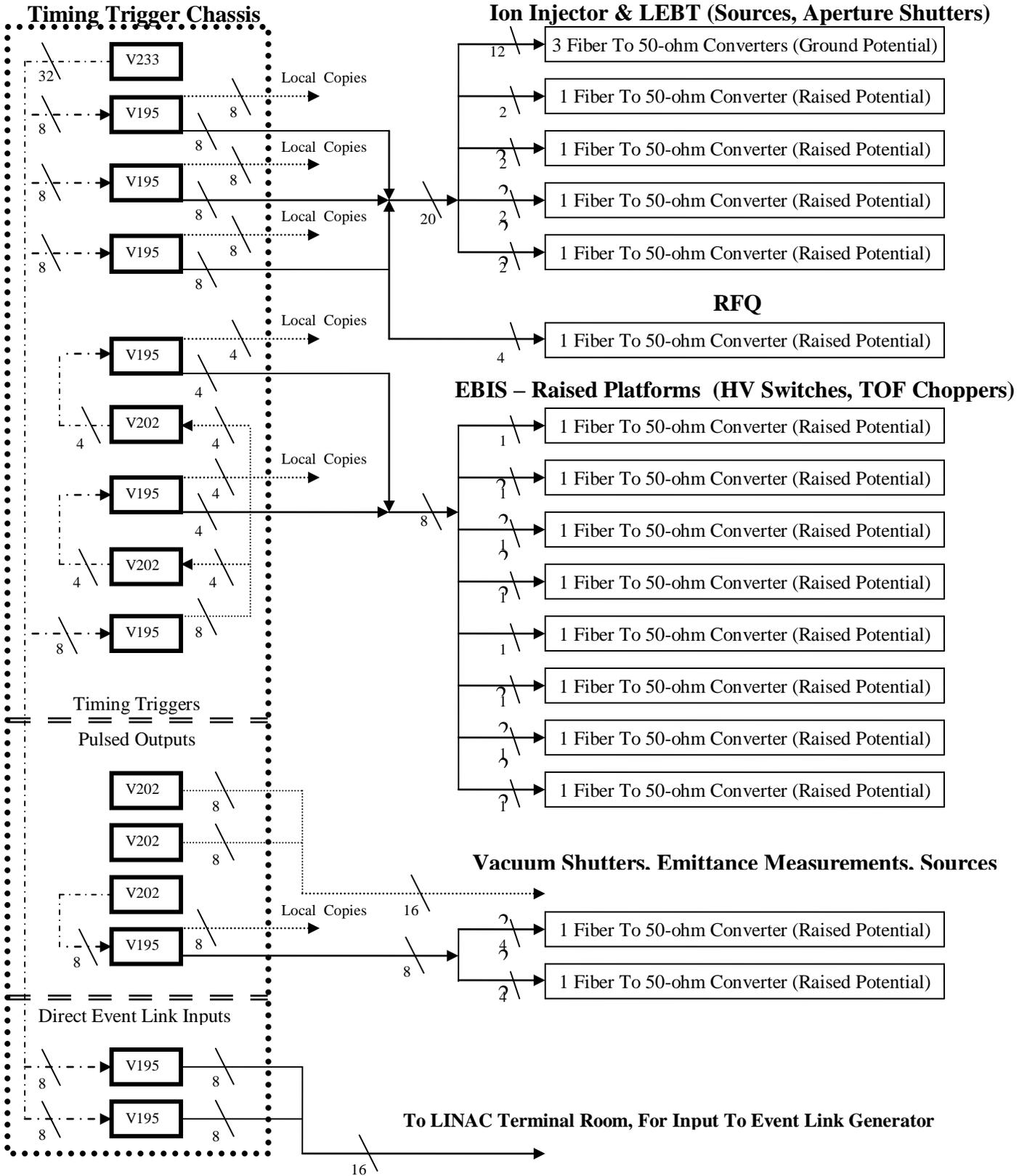


Table 8. Equipment Summary For Timing Signal Generation And Event Inputs

VME Chassis	TBD	1
Processor	MVME3100-1152	1
Memory Module	MM6702CN-4M	1
Utility Module	V108	1
Function Generator	V233	1
Delay Module	V202	5
Fiber Optic/50 Ohm Driver Module	V195	8
6 Slot Overlay Module	1320VLJ206	1
2 Slot Overlay Module	1320VLJ202	4

Figure 9. Timing Trigger And Pulsed Output Signal Distribution



Data Acquisition

Controls will capture the following 33 analog signals using spare PSI analog inputs:

Vacuum Reading:	5
Collector Cooling Water Temperature:	1
Collector Temperature:	1
Magnet Cooling Water Temperature:	2
Collector Current:	3
Electro-Static Steerer Voltage:	12
Y-Chamber Bender Voltage:	6
Trap Drift Tube Voltage:	1
Extraction Barrier Drift Tube Voltage:	1
Gun Barrier Drift Tube Voltage:	1

All signals will be conditioned by their “owners” to within a range of ‘0 to +10 volts’, or ‘-10 to +10 volts’, and will be referenced to their local platform common. The “owners” will also be responsible for the wiring between the signal conditioners to the PSI inputs.

PSIs have four analog inputs, with each input having sixteen bits of resolution. The typical PSI/Power Supply interface within EBIS only requires the use of two analog inputs for readbacks. The unused PSI analog inputs provide the capacity to collect analog data from high voltage platforms without adding separate data acquisition systems. Data is only sampled while a PSI is generating an output reference voltage. The sample rate is fixed at the rate the PSI is generating its reference voltage, which is either 10KHz or 100Khz, depending upon the controller.

Fiber Optic Infrastructure

Various serial links, networks, and pulses must be brought to and from EBIS using fiber optic cables. Many of these signals originate from or go to places that are a significant distance away. A fiber optic distribution system is in place in many areas that consists of fiber optic cable bundles and distribution boxes, known as MIC boxes. EBIS will make use of some of these existing MIC boxes and fibers, but four new MIC boxes will be added to expand the fiber optic infrastructure into the EBIS area.

930UEB will be used as the central point for tying the fiber optic infrastructure into EBIS. Existing MIC box 128A is located there, and connects to Building 957. This will be the source for the Reset Link and RTDL, both used in EBIS.

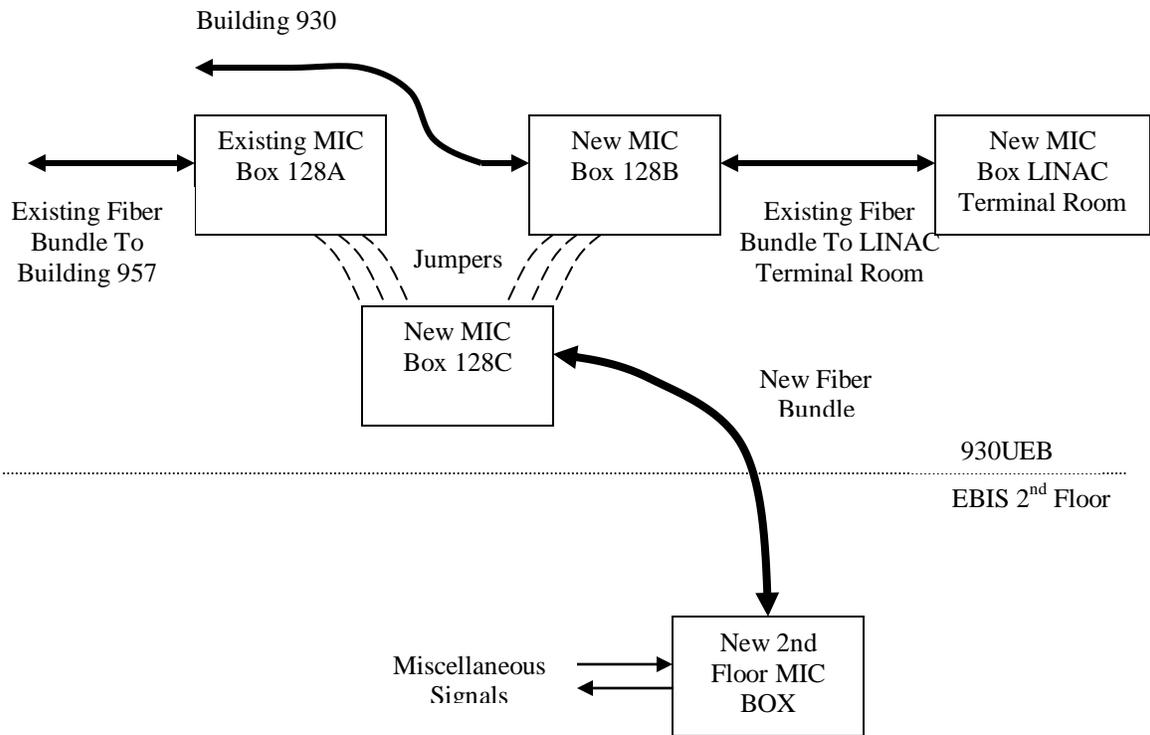
Also available in 930UEB is an existing fiber cable bundle that contains nineteen unused fibers. It runs from an area called the LINAC Terminal Room, in to 930UEB, and on to Building 930. The Terminal Room is located directly below the LINAC Control Room, which is where the LINAC Event Link is generated. EBIS needs access to this Event Link, and needs to be able to send pulses to the Event Link generator in order to initiate events on the link. The LINAC Terminal Room is also where EBIS will gain access the network infrastructure (.40 and .108 subnets)

To provide fiber optic paths to EBIS, a total of four MIC boxes will be added to the fiber optic infrastructure. New MIC box 128B, located next to MIC box 128A, will be used as a distribution center for the fiber cables that currently runs between the LINAC Terminal Room and Building 930. A second MIC box will be installed in the Terminal Room, and the existing fiber bundle will be terminated there. This will allow the transmission of signals between the 930UEB area and the LINAC Control Room.

A third MIC box, 128C, will be installed next to MIC box 128A and 128B. This box will be one end of the EBIS fiber optic trunk. Any remote signals that need to be routed from Building 957 or the LINAC Terminal Room to EBIS will be patched into MIC box 128C from their respective MIC boxes. The fourth MIC box will be located in the 2nd floor area of EBIS. A new fiber optic cable bundle will connect this MIC box back to MIC box 128C, thus connecting EBIS to the fiber infrastructure.

Figure 10 on the next page depicts the fiber optic interconnections.

Figure 10. Fiber Optic Infrastructure For EBIS



Event Link Distribution

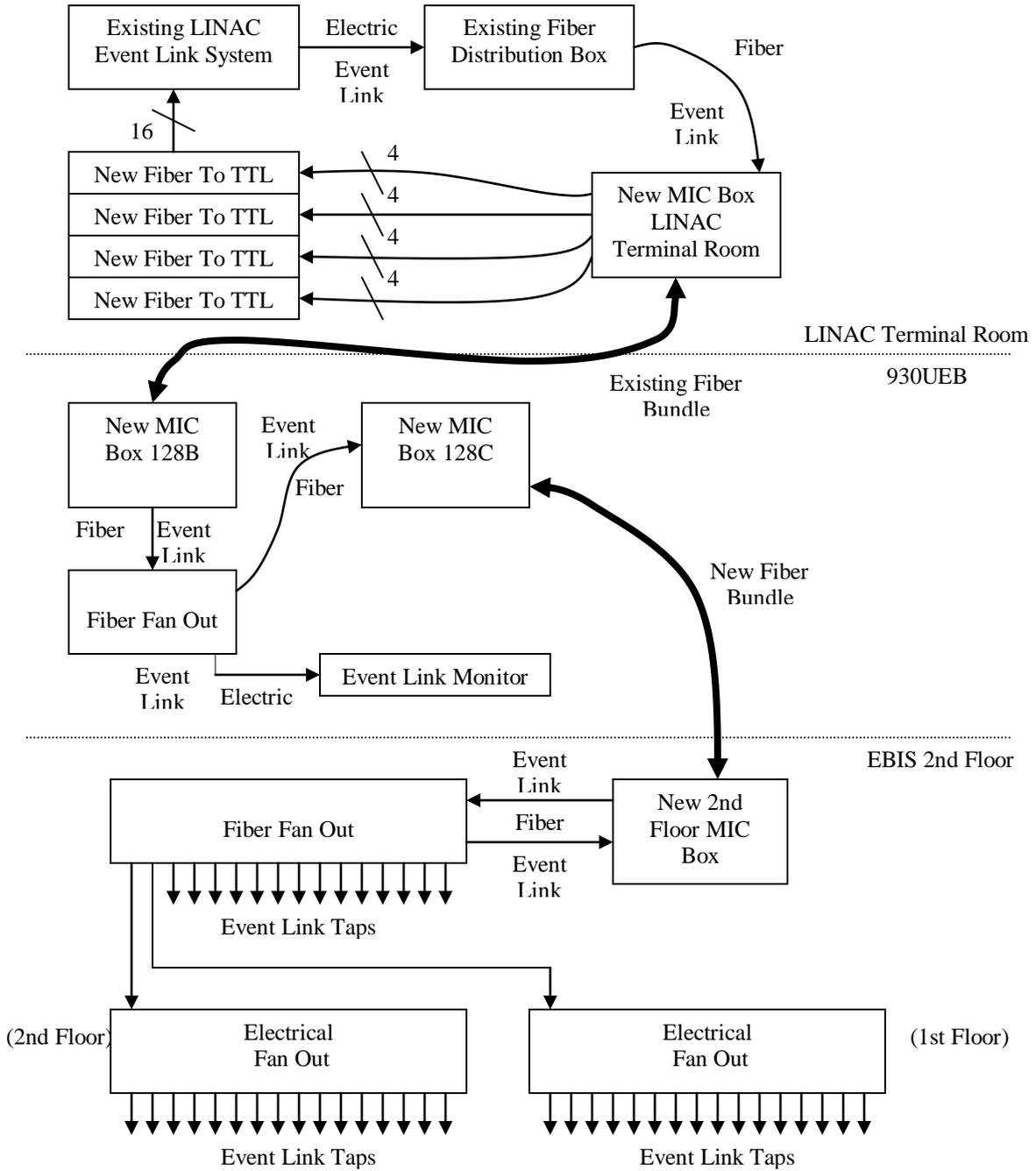
An Event Link is a serial timing link that provides synchronization to all equipment locations. Every V108, V202, and V233 module requires a connection to an Event Link. The LINAC Event Link will provide this functionality for EBIS. The VME chassis that houses the Event Link system is located LINAC control room.

Two mechanisms are used to generate events on the Event Link...commands and direct inputs. Paths for as many as sixteen direct inputs from the EBIS Timing Trigger chassis back to the LINAC Event Link system will be available in the form of an existing fiber optic cable bundle. Two V195s will be available in the Timing Trigger VME chassis to convert timing trigger electrical signals to light signals. At the Event Link chassis, four Fiber-to-TTL Converter units will convert the light signals back to electrical signals. From there they will be patched to inputs on existing Event Input Modules (V101).

The LINAC Event Link will be available fiber optically at the EBIS end of LINAC (930UEB, 2nd floor), in MIC box 128B. Presently, the LINAC Event Link is fed to a Fiber Optic Distribution box, which in turn is connected to an Event Link Monitor board in 930UEB. The existing distribution box will be replaced with a Fiber Fan Out box. (BNL Assembly 94028923). This unit has one fiber input, a re-transmitted fiber output, and 16 electrical outputs. The existing Event Link Monitor board will be connected to one of the electrical outputs of the Fiber Fan Out box. The re-transmitted fiber output will be fed to a new EBIS MIC box 128C, located close to MIC box 128B. At the new 2nd floor EBIS MIC box, the LINAC Event Link will be patched into a Fiber Fan Out box, making the LINAC Event Link available on the 2nd floor of EBIS.

Through the Fiber Fan Out box, there are 16 electrical sources of the LINAC Event Link. To provide more taps into the Event Link, two Electrical Fan Out boxes (BNL assembly D09-E2442-5) will be added. One will be located on the 2nd floor, and one on the 1st floor. Each box will receive one of the electrical outputs from the Fiber Fan Out box, and provide another 16 outputs. This will make 46 available taps for the Event Link. Fan out boxes can be added for expansion purposes.

Figure 11. LINAC Event Link Distribution

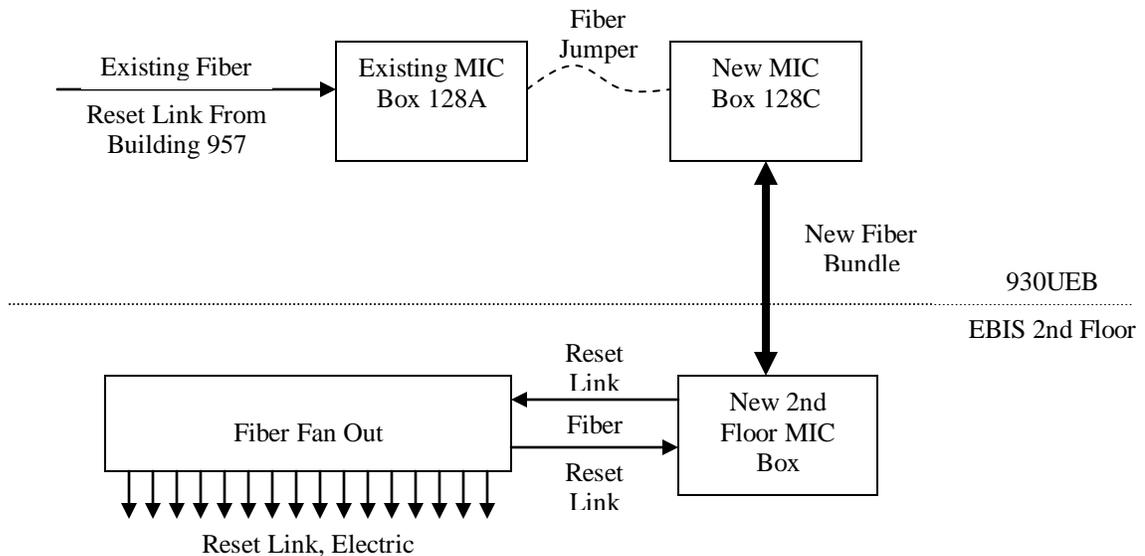


Reset Link Distribution And Reset Modules

The Reset Link is an independent communication link that provides remote reset capability for each VME chassis equipped with a V108 Utility Module. Coupled with an AC Power Reset Module, it provides a way of remotely interrupting AC power to a VME chassis or other piece of electronic equipment for the purpose of resetting or rebooting.

The Reset link is available in Building 957 as a fiber optic signal. It will be routed to existing 128A MIC box, and from there, to the new EBIS MIC boxes. A Fiber Optic Fan Out box will be used to convert the signal from fiber to multiple electrical outputs.

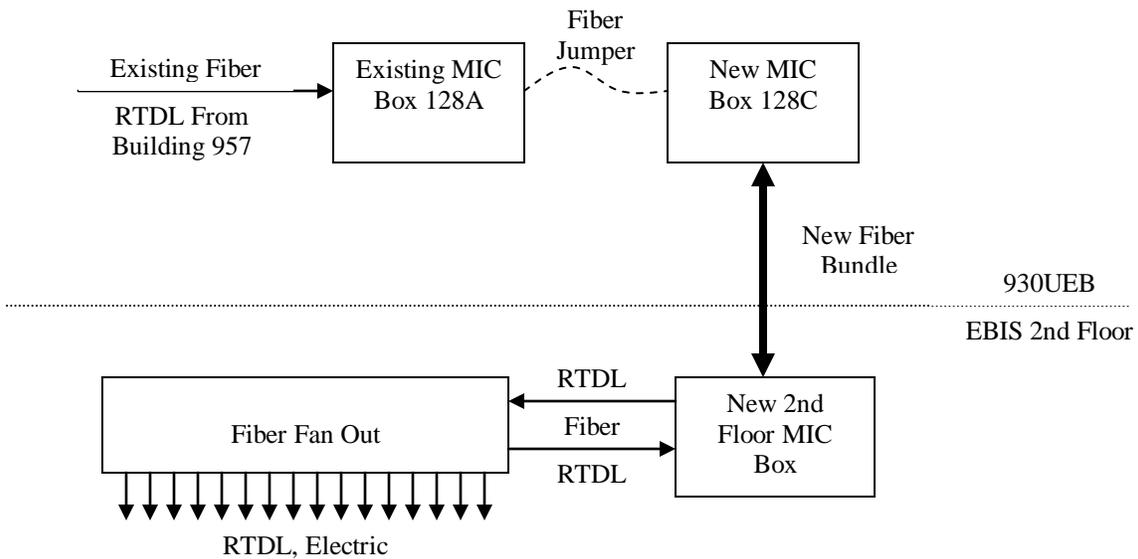
Figure 12. Reset Link Distribution



Real Time Data Link Distribution

The Real Time Data Link (RTDL) distributes various parameters around the accelerator complex, including time-of-day information, which is used by VME processors to time-tag data and events. The RTDL link is available in Building 957 as a fiber optic signal. It will be routed to existing 128A MIC box, and from there, to the new EBIS MIC box. A Fiber Optic Fan Out box will be used to convert the signal from fiber to multiple electrical outputs.

Figure 13. RTDL Distribution

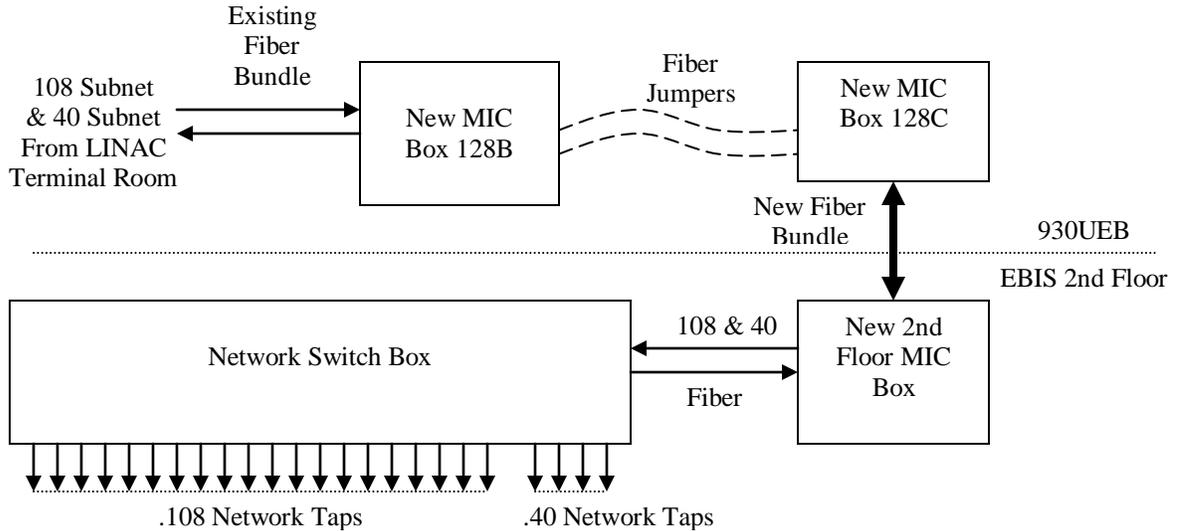


Network Distribution

Two networks will be provided for use by EBIS equipment. The .108 subnet is considered the operations network. All network communication capable equipment whose operation is vital to running EBIS will connect to this subnet. The .40 subnet is for use by all other equipment. Devices such as diagnostic equipment, temperature and humidity monitoring devices, and laptops will use this subnet.

Both subnets are available in the LINAC Terminal Room. They will be routed to the new 128B MIC box, and from there, to the new EBIS MIC box. A network switch box will be installed on the 2nd floor of EBIS. The switch will provide twenty-four network taps. The first twenty taps will be dedicated to the .108 subnet. The last four taps will carry the .40 subnet.

Figure 14. Network Distribution



Workstations

Three LINUX workstations will be provided for the EBIS facility. Two work consoles will be located on the first floor, and one on the second floor. The first floor consoles will be stationed in racks, providing a small work area for EBIS machine development and maintenance support. The second floor station will be placed on its own table and be primarily used for maintenance support.

In addition to the work consoles, a rack-mounted Alarms monitor and a color printer will be installed on the first floor.

A rack mountable 16-port Serial-to-Ethernet terminal server (Portserver TS 16, manufactured by Digi) will be installed on the 2nd floor of EBIS. This terminal server will provide a communications path for maintenance access the Front End Computers (FEC) located in every VME chassis.

Diagnostic System Interface

The following beam instrumentation devices as requiring control system interfaces to acquire and generate diagnostic signals:

Current Transformer (CT)	7 ea
Profile Monitor (PM)	3 ea
Faraday Cup (FC)	7 ea
Fast Faraday Cup (FFC)	1 ea

All devices are located at normal ground potential, requiring no special isolation for signal interfaces. A standard VME chassis will be provided, configured with the boards necessary to generate/acquire the signals described below.

Digital Outputs (VMIVME-2170A, 2 Boards Required)

Gain Control	(CT)	14 (2 per device)
Calibration Select	(CT)	3
Plunge Control	(PM)	3
Gain Control	(PM)	6 (2 per device)
Plunge Control	(FC)	7
Gain Control	(FC)	<u>14</u> (2 per device)
	Total	47

Digital Inputs (VMIVME-1160A, 2 Boards Required)

Local/Remote	(CT)	7
Local/Remote	(PM)	3
Local/Remote	(FC)	7
Status	(PM)	3
Status	(FC)	14 (2 per device)
Bias Trip Status	(FC)	<u>7</u>
	Total	41

Analog Inputs (VMIVME-3123, 2 Boards required)

Output Signal	(PM)	6 (2 per device)
Output Signal	(FC)	<u>7</u>
	Total	13

Two analog boards are necessary to allow the simultaneous capture of data from the Profile Monitors and the Faraday Cups, which use independent clocks for data acquisition.

Timing pulse signals are also required for instrumentation systems. The timing pulses will be generated by two Delay modules (V202), and be distributed using two Fan Out modules (V294).

<u>Timing</u>		<u>V202 Channels</u>	<u>V294 Outputs</u>
Calibration Pulse	(CT)	1	none
Reset	(PM)	1	3
Clock	(PM)	1	3
Start Integrate	(FC)	2 (EBIS injection & Transfer Line)	8
Stop Integrate	(FC)	2 (EBIS injection & Transfer Line)	8
Scope trigger		1	none
Misc. Channels (Local Testing)		<u>4</u>	<u>none</u>
	Total	12	22

In addition to the previously listed signals, fifteen “fast analog signals” need to be available for monitoring with an oscilloscope. Using three VME multiplexer modules (Agilent E1366A), the fifteen signals will be multiplexed down to four, and then connected to the inputs of a four-channel oscilloscope. The scope and associated wiring will be provided by Instrumentation. The scope will communicate over an Ethernet network. The monitored signals are listed below.

Fast Analog Signal	(CT)	7
Fast Analog Signal	(FC)	7
Fast Analog Signal	(FFC)	<u>1</u>
	Total	15

The table below shows the itemized boards in the Instrumentation Chassis.

Table 9. Instrumentation Chassis

Processor	MVME3100-1152	1
Memory Module	MM6702CN-4M	1
Utility Module	V108	1
Delay Module	V202	2
Fan Out Module	V294	2
Digital Output Module	VMIVME-2170A	2
Digital Input Module	VMIVME-1160A	2
Analog Input Module	VMIVME-3123	2
Multiplexer Module	E1366A	3

Vacuum System Interface

The vacuum system has the following interface requirements:

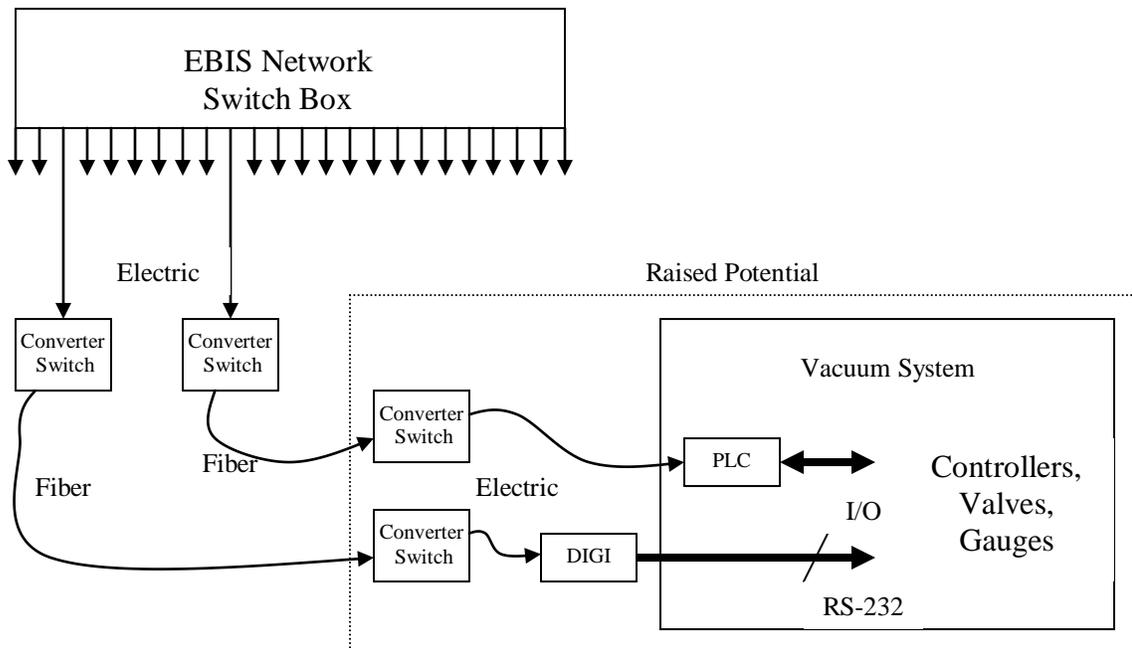
- 2 Ethernet connections at ground potential
- 2 Ethernet connections at high potential
- 17 Ethernet-to-RS232 ports at ground potential
- 9 Ethernet-to-RS232 ports at high potential
- Access to existing Controls infrastructure

The EBIS Vacuum system is comprised of PLCs, Pump Controllers, Valves, and Gauges. One system will be at ground potential, and one at a high voltage potential.

Ethernet connections via network switch boxes to the system at ground potential are already available. To provide Ethernet connections at the high potential system, converter switches will be used. (CS14-i, manufactured by GarrettCom Inc.) Converter switches convert electrical Ethernet signals to fiber, and visa versa. Digi TS 16 Port Servers will be used to provide Ethernet-to-RS-232 conversion.

The figure below depicts the network connections for the vacuum system located at a high voltage potential.

Figure 15. High Potential Vacuum System Network Connections



RF System Interface

The following equipment will be provided for configuration and installation as part of the RF system:

2 VME 64X chassis	
2 Processor Modules	(MVME 3100-1152)
2 Utility Modules	(V108)
2 Memory Modules	(MM6702CN-4M)
4 Delay Modules	(V202)
4 Fan Out Modules	(V294)

1/2/07