

# Instrumentation Division Report

# Microelectronics

**Development of Application Specific  
Integrated Circuits (ASICs) for BNL/DOE  
Experimental Research Programs**

**Staff: 3 scientific, 2.5 professionals**

**Publications in 2006: 21**

Gianluigi De Geronimo, Ph.D.

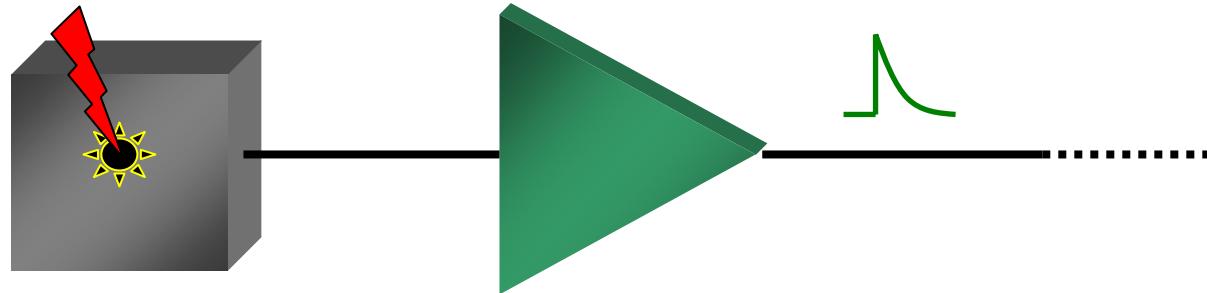
Presentation to the DOE HEP Program Review

APRIL 18, 2007

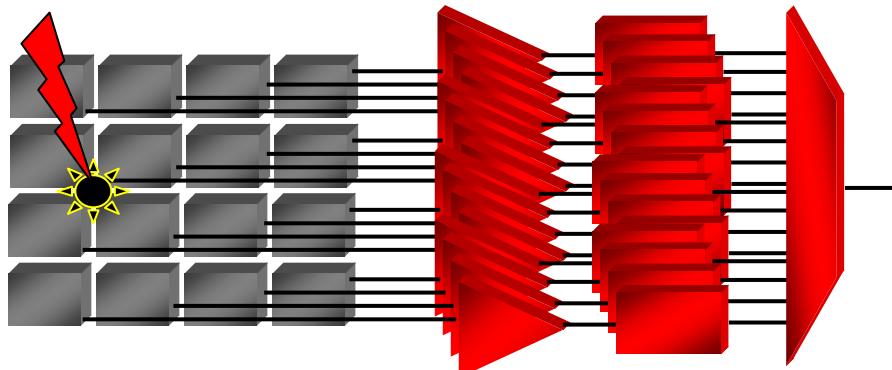


# From Electronics to Microelectronics

Electronics for radiation detectors consists of low noise readout of the signals generated in the sensor by ionizing radiation



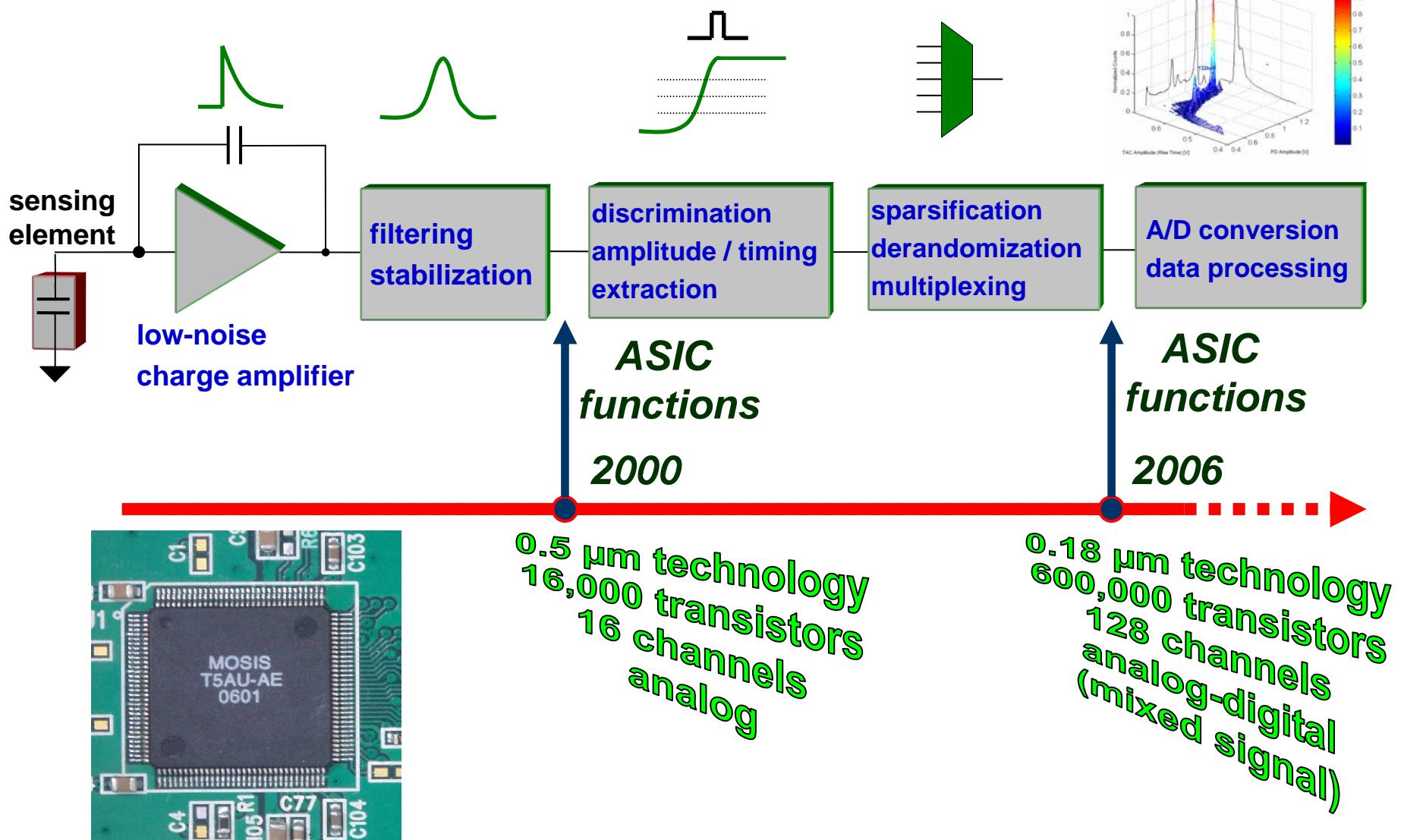
Low density, low functionality → discrete electronics



High density, high functionality → integrated circuits

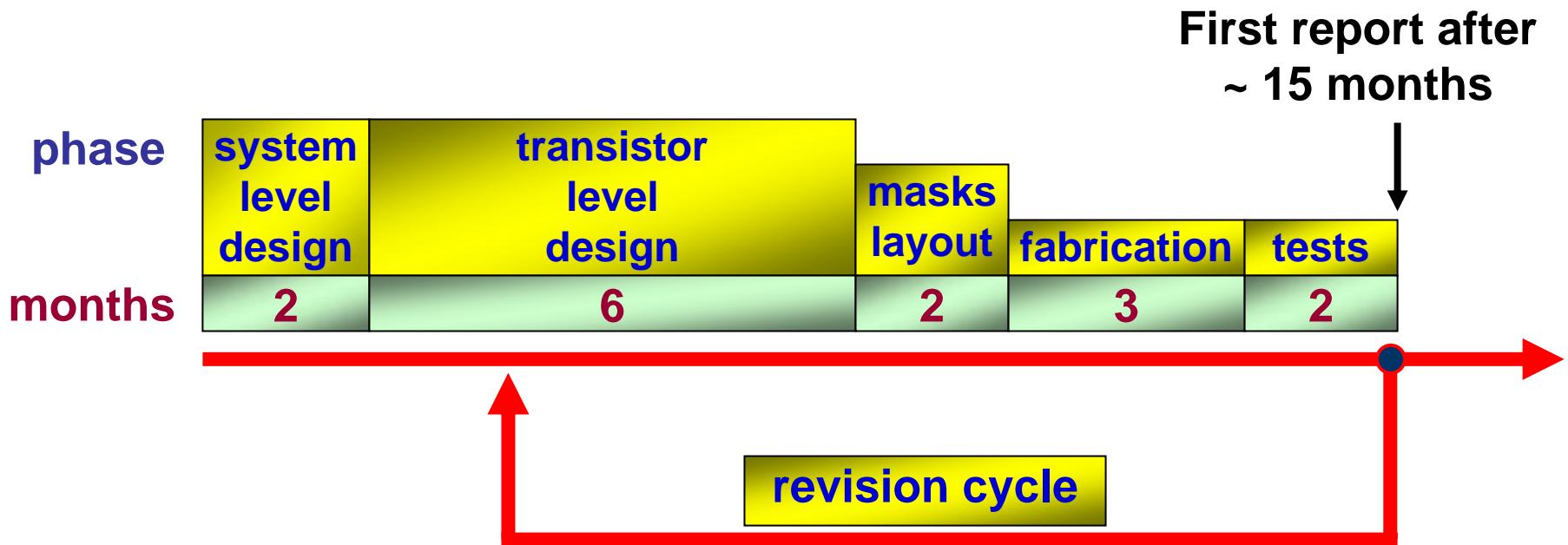
# Integration

## Typical electronics channel



# ASIC Design Flow

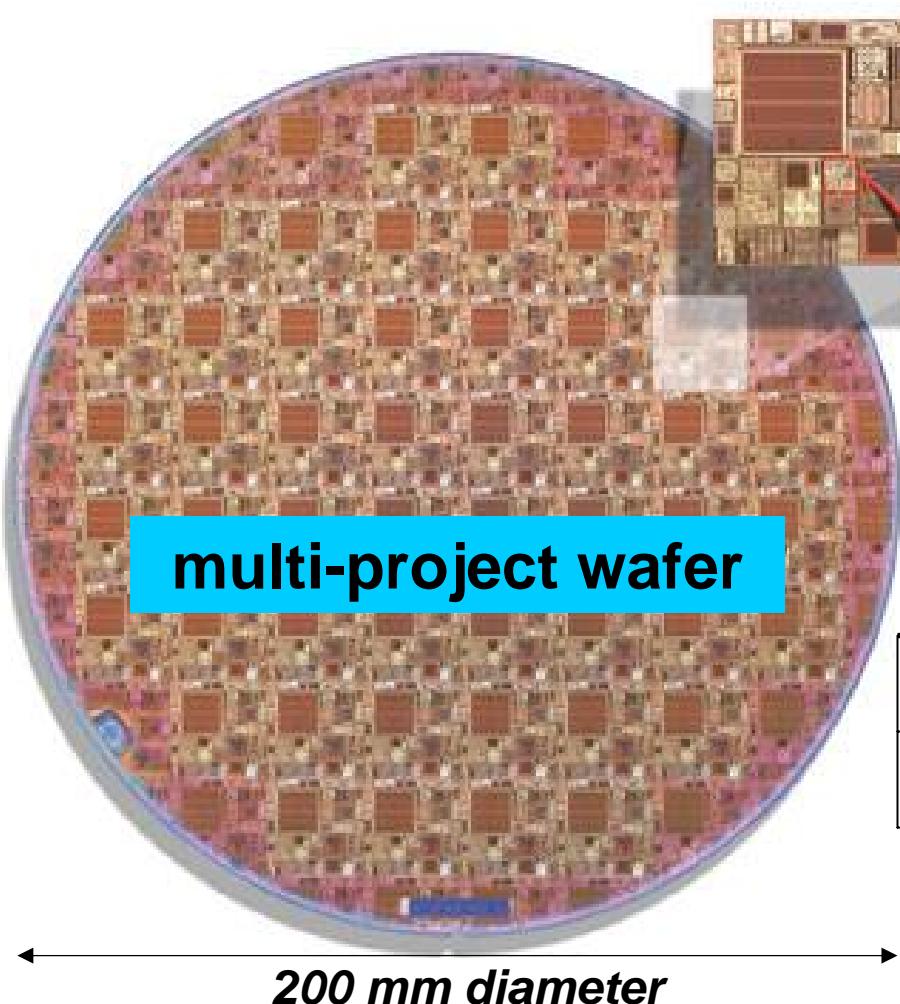
Higher complexity means more resources and expertise, longer development time and ultimately higher risk



From concept to ready-for-production:  
2 - 3 years (depending on complexity)

# ASIC Fabrication

Major foundries accept designs from multiple customers



20 mm reticle

**BNL ASIC is here**  
( $10 \text{ mm}^2$ ,  $\sim 30,000$  transistors)

	multi-project	dedicated
samples	tens	thousands
cost	\$ 20,000	\$ 200,000

**Ideal for prototyping  
and low volume**

## About our group

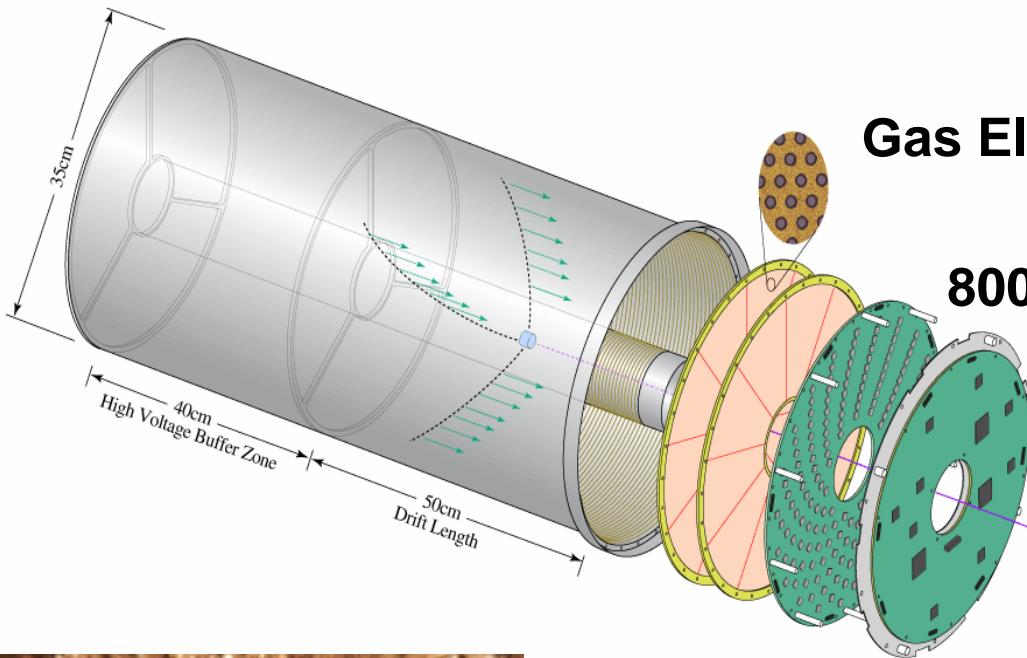
**We have an established worldwide  
reputation as leaders in low-noise ASIC design**

**In the last 10 years we developed more than 30 ASICs  
for applications in:**

- **Particle and Nuclear Physics**
- **X- and Gamma-ray Spectroscopy and Imaging**
- **Medical, Security, Industrial**

**Some examples from the  
past three years ...**

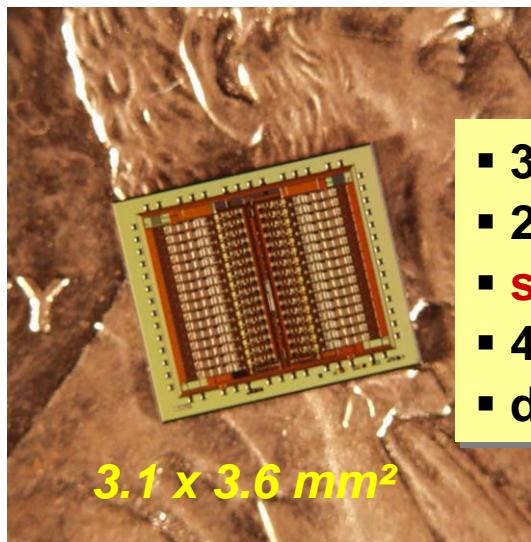
# ASIC for the Laser Electron Gamma Source TPC



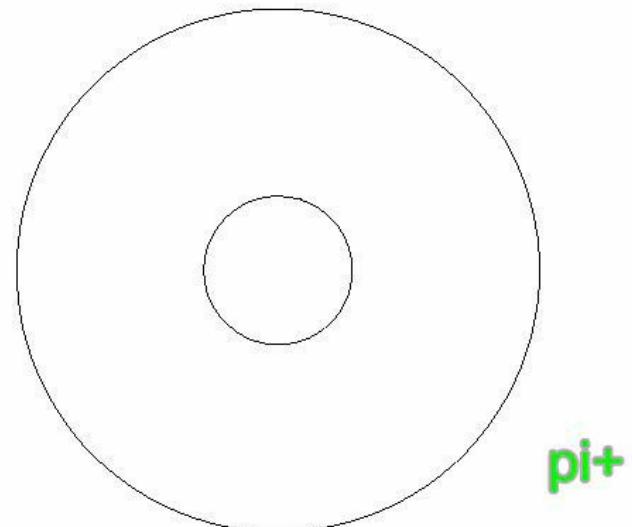
## Gas Electron Multiplier

8000 anode pads read out in less than 400  $\mu\text{s}$  due to unique sparse readout

## Charged Pion production



- 32 channels
- 230 e<sup>-</sup>, 2.5 ns resol.
- sparse readout
- 40,000 transistors
- dev. time: 16 months

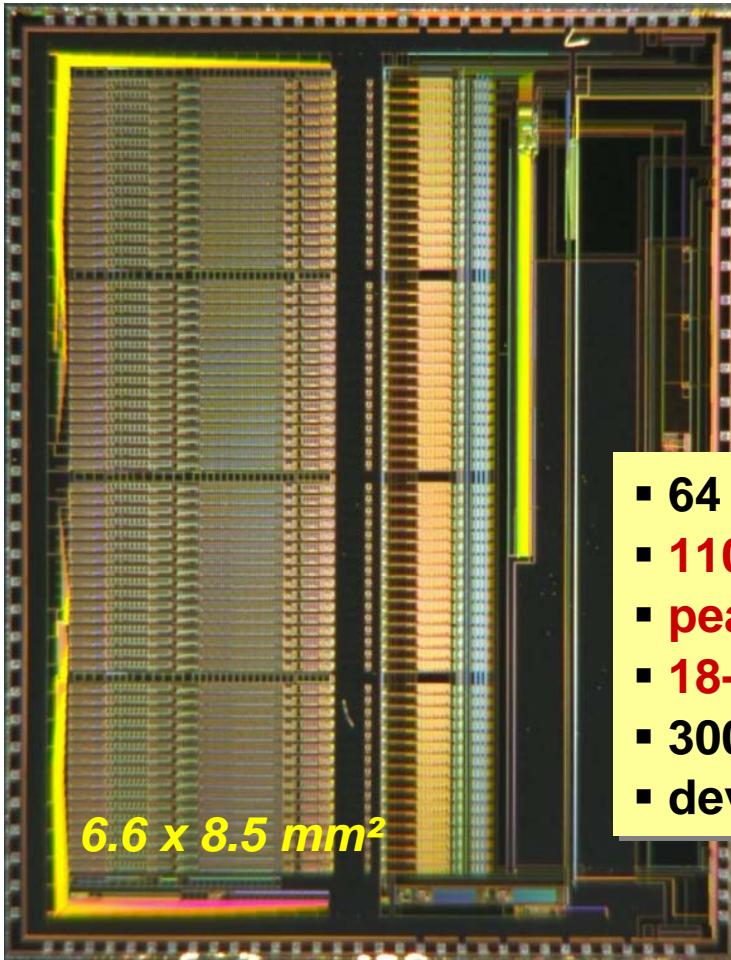


pi+

# ASIC for Spallation Neutron Source Instruments

## Unity-Gain $^3\text{He}$ Gas Detector for Small Angle Neutron Scattering

40,000 anode pads, each  $25 \text{ mm}^2$ , global rate  $10^8 \text{ n/s}$

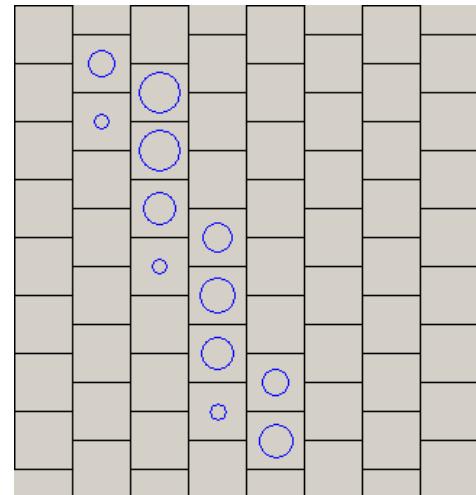


$6.6 \times 8.5 \text{ mm}^2$

- 64 channels
- 110 e<sup>-</sup>, 1.5 mW/ch.
- peak detector ADC
- 18-bit timing
- 300,000 transistors
- dev. time: 20 months

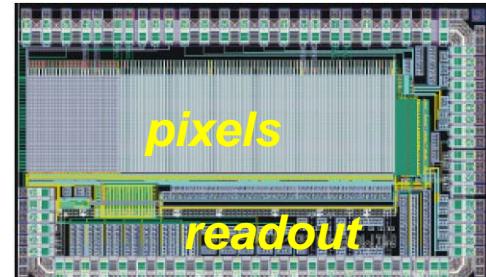
Count rate capability two-orders of magnitude greater than any existing instrument due to unique design, combining unity gas-gain and low-noise ASIC

test of 8x8 pad  
with  $\alpha$  particles

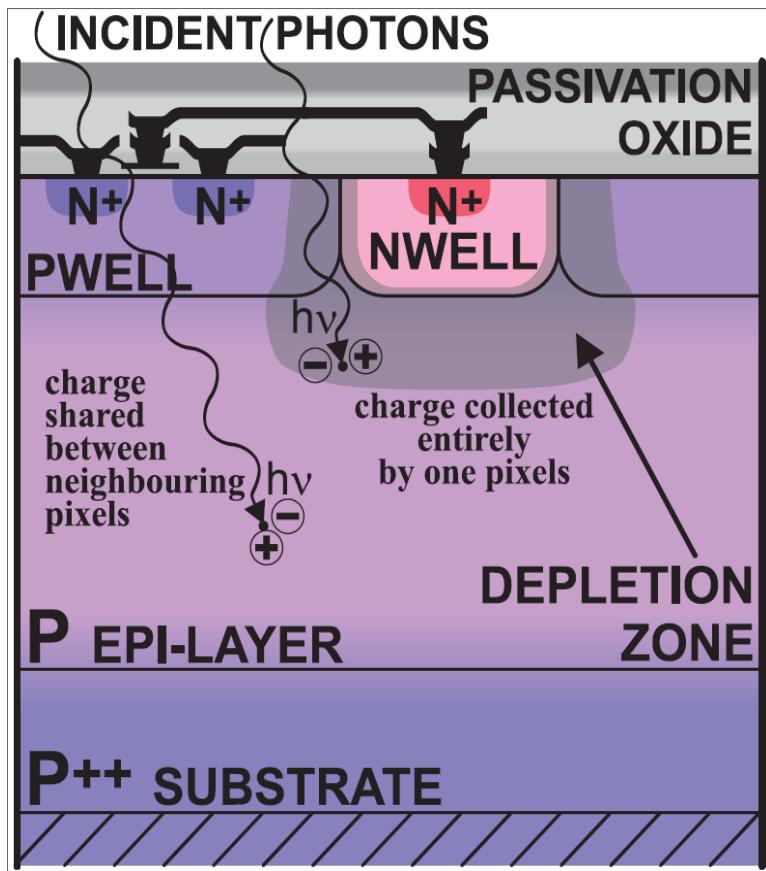


# Monolithic Active Pixel Sensors (MAPS)

Sensor and readout in single entity for high-density (mega-pixel) applications (e.g. STAR and ILC vertex detectors)



G. Deptuch et al.



## ← *MAPS in commercial CMOS*

Good radiation tolerance and low-cost but poor Charge Collection Efficiency (few hundreds electrons spread by diffusion among several pixels in hundreds of nanoseconds → impact on S/N !)

## *Research to improve CCE*

- Drift assisted collection (BNL LDRD)
- Silicon-on-Insulator (BNL-FNAL)

# ASICs for Synchrotron Applications

**HERMES**



**SCEPTER**



- 32 channels front-end
- sub-20 electrons resolution
- **spectroscopy, photon-counting**
- **high-rate**
- **180,000 transistors**

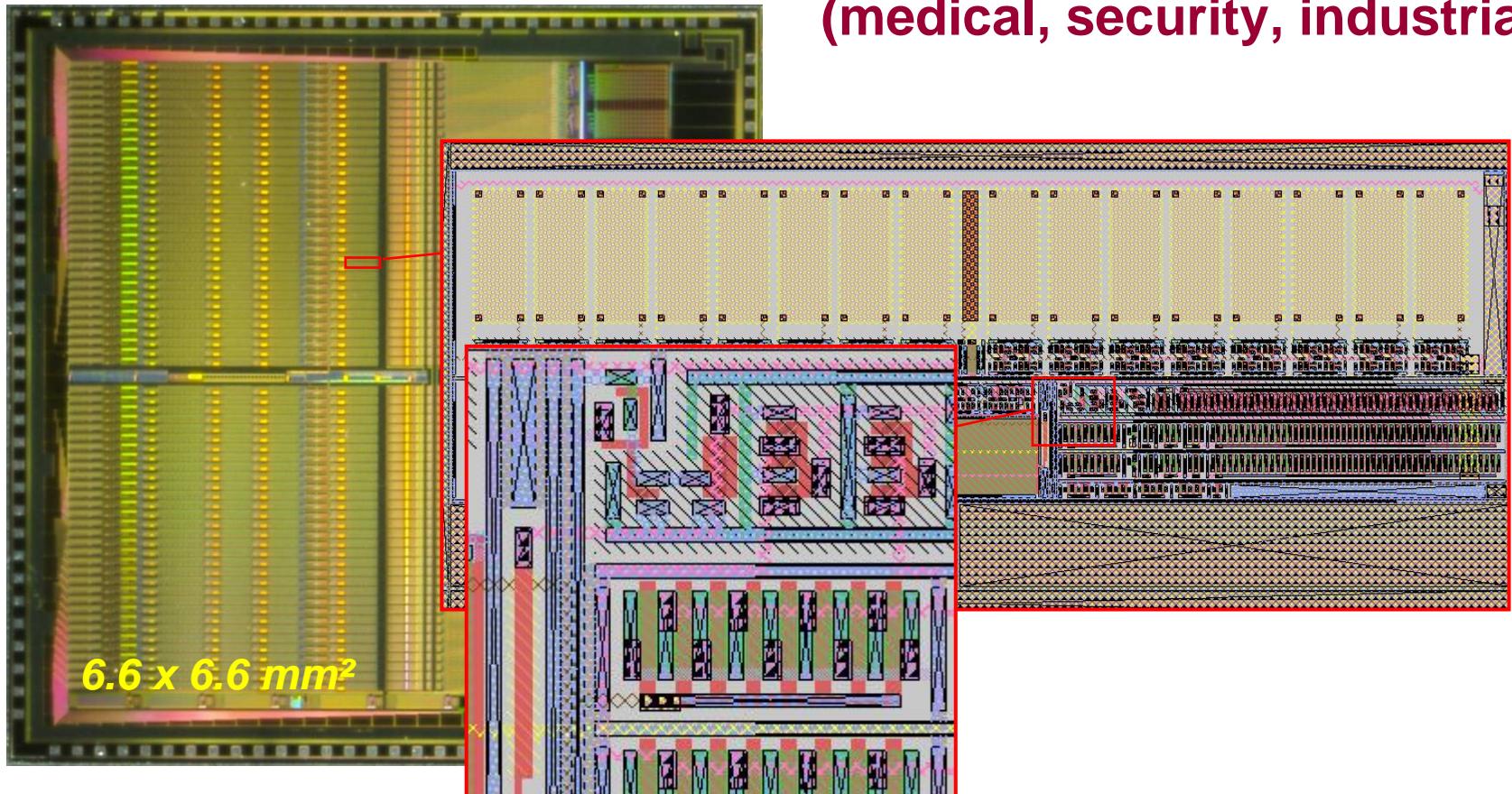
- **32 channels processing**
- **peak detection, sparsification, derandomization, multiplexing**
- **energy, timing and address**
- **high rate**
- **36,000 transistors**

For high-rate high-resolution spectroscopy and  
photon-counting experiments at NSLS and NSLS-II  
(EXAFS, powder diffraction, fluorescence microprobes)

# ASICs for Cadmium Zinc Telluride (CZT) Detectors

We provide ASICs to all CZT-related  
research in BNL and to major CZT industries

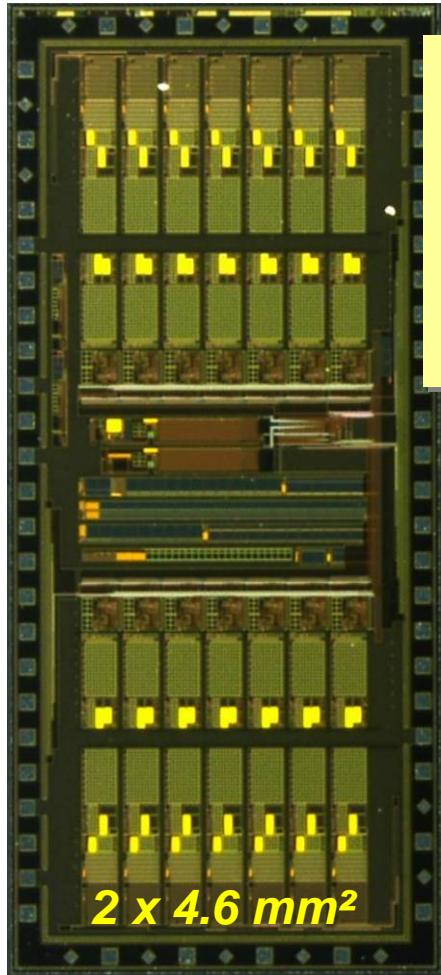
**ASIC for ultra-high-rate photon counting applications  
(medical, security, industrial)**



# Ultra-Low Noise ASIC for Moon Elemental Mapping (NASA)

## X-ray Spectroscopy with Semiconductor Drift Detectors

500 cm<sup>2</sup> detector, 15 mm<sup>2</sup> pixels



- 14 channels
- sub-10 electrons resolution, 1.2 mW/ch.
- peak detection and sparse readout
- 30,000 transistors
- dev. time: 15 months

### Interest from:

- Dave Nygren (LBNL) for his new Ionization Imaging Chamber (search for  $0-\nu \beta\beta$  decay)
- NSLS, NSLS-II, NJIT for high-resolution high-rate synchrotron applications

## Other ASIC Projects

- ❖ **ATLAS:** Cathode Strip Chamber (3 ASICs)
- ❖ **ATLAS:** Calorimeter Upgrade (SiGe front-end)
- ❖ **PHENIX:** Time Expansion Chamber
- ❖ **STAR:** Silicon Vertex Tracker
- ❖ **SLAC:** Scattering Experiments at Linac Coherent Light Source
- ❖ **UNM:** Dark Matter (Dinesh Loomba)
- ❖ **NRL:** Compton Imager (DHS), X-ray Navigation System (NASA)
- ❖ **MEDICAL, SECURITY, INDUSTRIAL:** Micro-PET, 3D Position  
Sensitive Detector (UM, DHS), Co-planar Grid Detector (LANL)
- ❖ **CRADAs:** eV Products (CZT), Digirad (Medical), CFDRC (MAPS),  
Photon Imaging (Silicon), Symbol Technologies (Wireless)  
- our patented circuit solutions are licensed to industries -

**Until now our success in responding to ASIC requests  
was based on the use of public domain CAD tools**

**We are now approaching ASIC requests  
with over one million transistors**

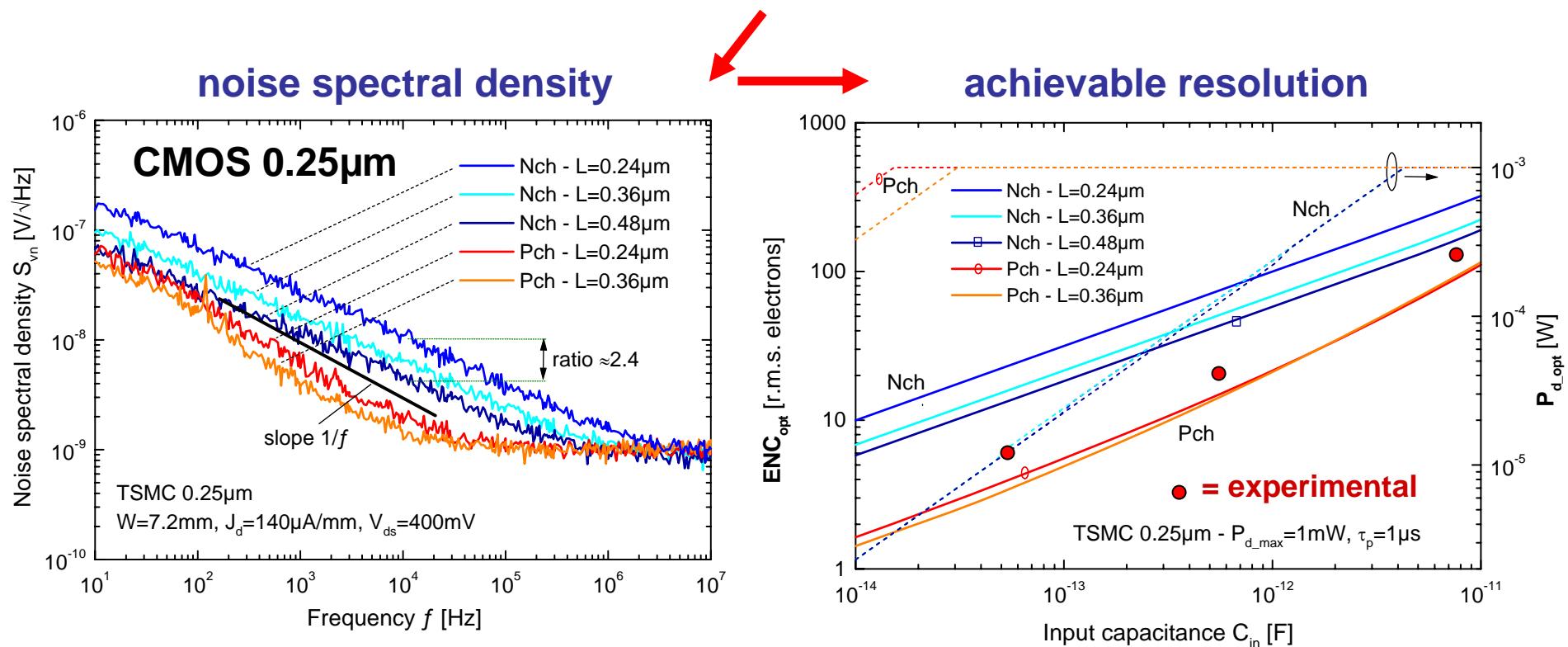
**With these tools BNL won't be able to respond to ASIC  
requests and to follow the state-of-the-art in ASIC development  
(we will lose principal ASIC designers at the Ph.D. level)**

**BNL ASIC group is in critical need  
for industry-standard tools  
(that other National Labs have)**

# **Backup slides**

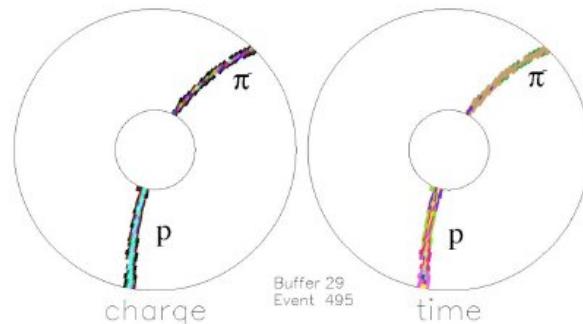
# Technology Characterization

## Design of low-noise front-ends requires extensive noise characterization

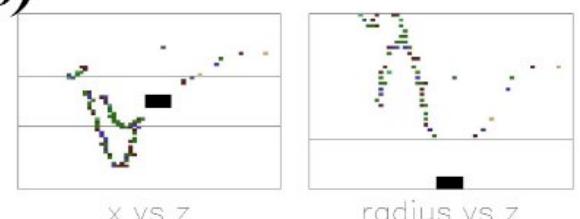
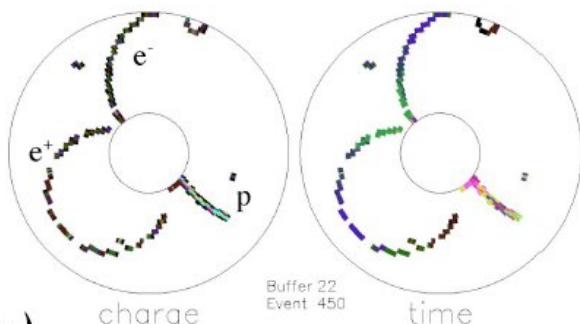


## *Sample TPC events*

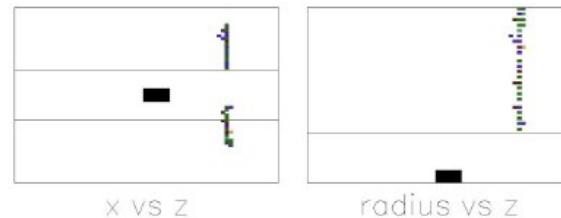
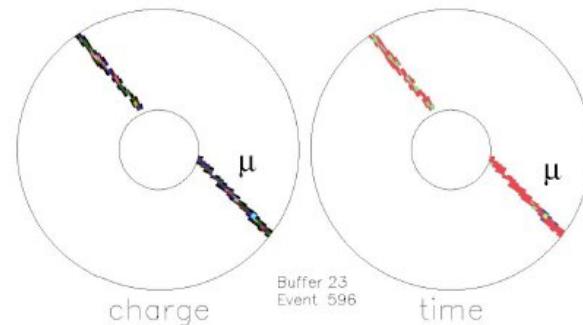
$\gamma n(p)$   
 $\downarrow$   
 $\pi^- p(p)$



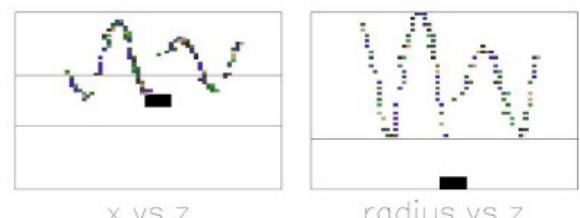
$\gamma n(p)$   
 $\downarrow$   
 $\pi^0 p(p)$   
 $\downarrow$   
 $\gamma(e^+e^-)\gamma p(p)$



*Cosmic*  
 $\mu$

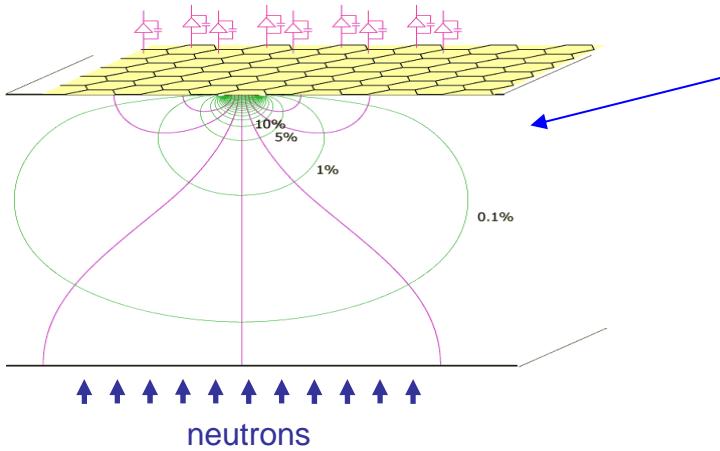


*atomic*  
 $e^-$   
*spiral*



# SANS ASIC for Unity-Gain Gas Detector

## Small Angle Neutron Scattering Experiments at SNS (Oak-Ridge)

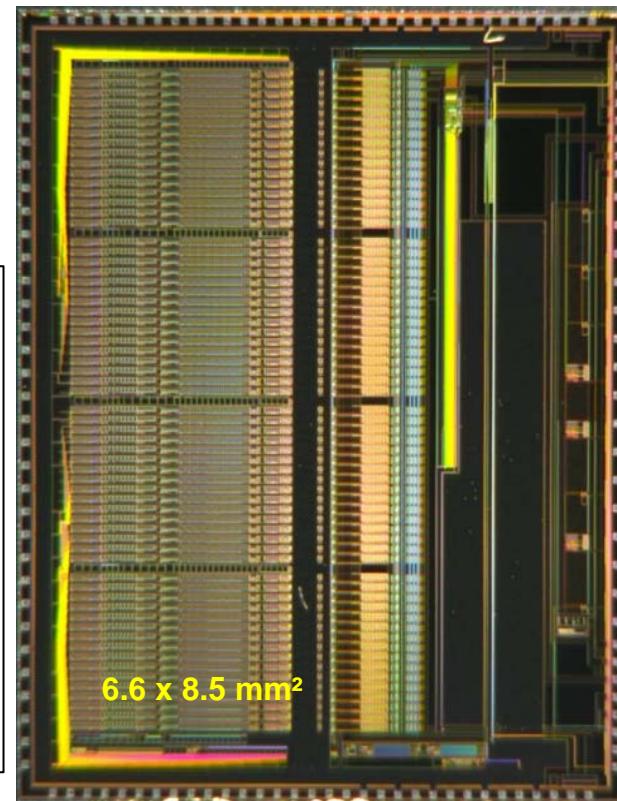
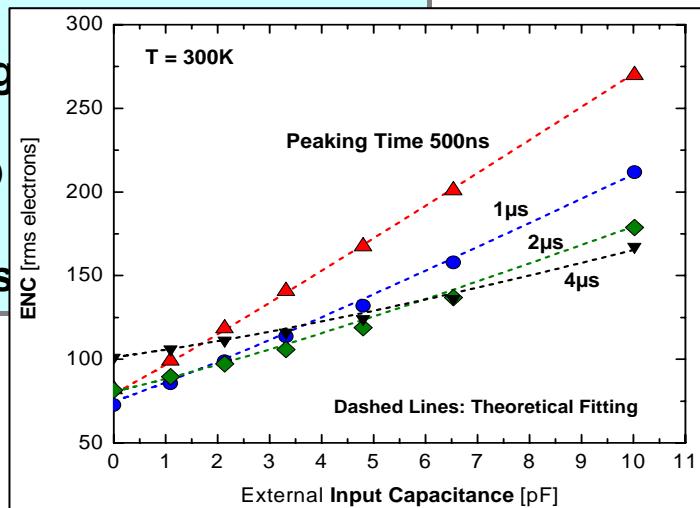


- Low-noise front-end → unity gas-gain
- Single-pad induction without Frisch grid
- ${}^3\text{He}$  pressure for max 3-pad charge sharing
- Prototype:  $48 \times 48$  pad array
- Full size:  $196 \times 196$  pad array ( $10^8$  n/s)
- Pad  $25 \text{ mm}^2$ ,  $5 \text{ pF}$ , rate  $5 \text{ kHz}$
- One **ASIC** for each  $8 \times 8$  pad array

### SANS ASIC

- 64 channels (preamplifier, shaper, discriminator, peak detector, 6-bit ADC, 18-bit timestamp)

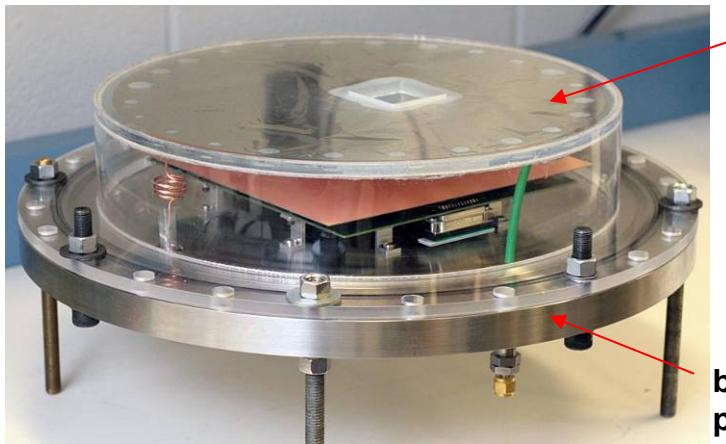
- CMOS  $0.25 \mu\text{m}$  technology
- $110 \text{ e}^-$  resol.,  $1.5 \text{ mW}/\text{ch.}$
- sparse readout and FIFO
- 300,000 MOSFETs
- develop. time: 20 months



G. De Geronimo et al., NSS (2006)  
collaboration with ORNL

# SANS ASIC for Unity-Gain Gas Detector

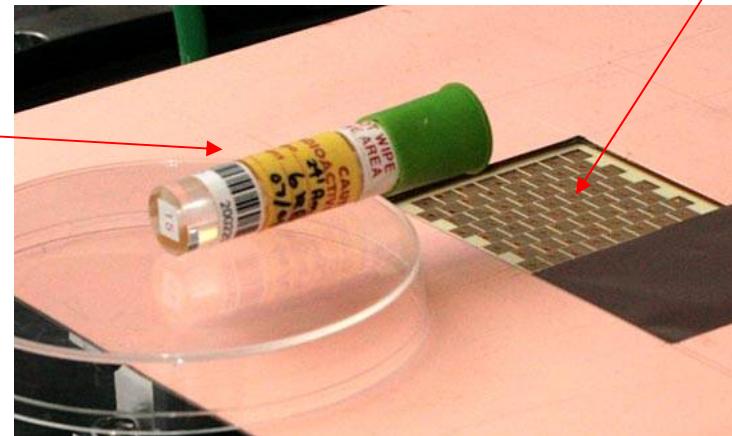
## Preliminary measurements with $\alpha$ particles



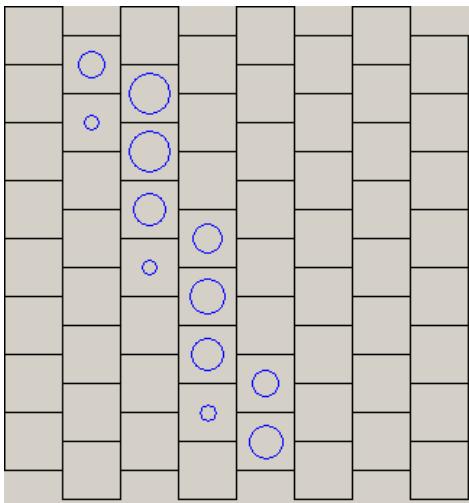
Lucite cover

5.5 MeV  
 $\alpha$  source

bottom of  
pressure  
vessel



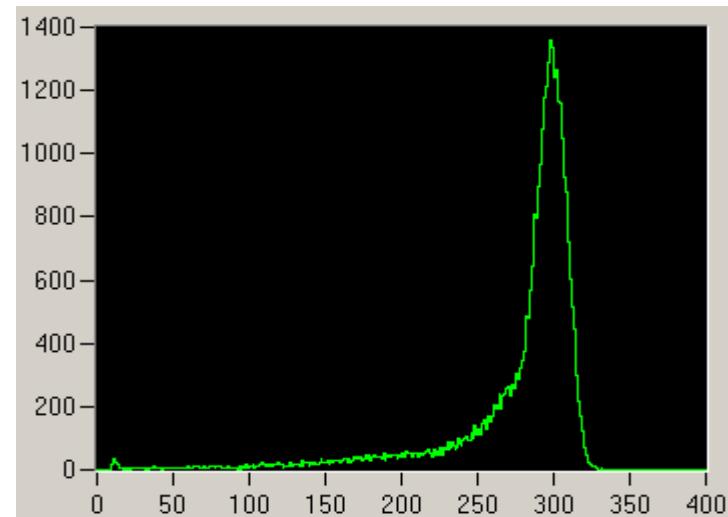
8 x 8  
anode pads  
(ASIC on  
other side)



$\alpha$  tracks recorded  
by the 8x8 pad array  
in P-10 gas.

G. Smith et al. (2007)

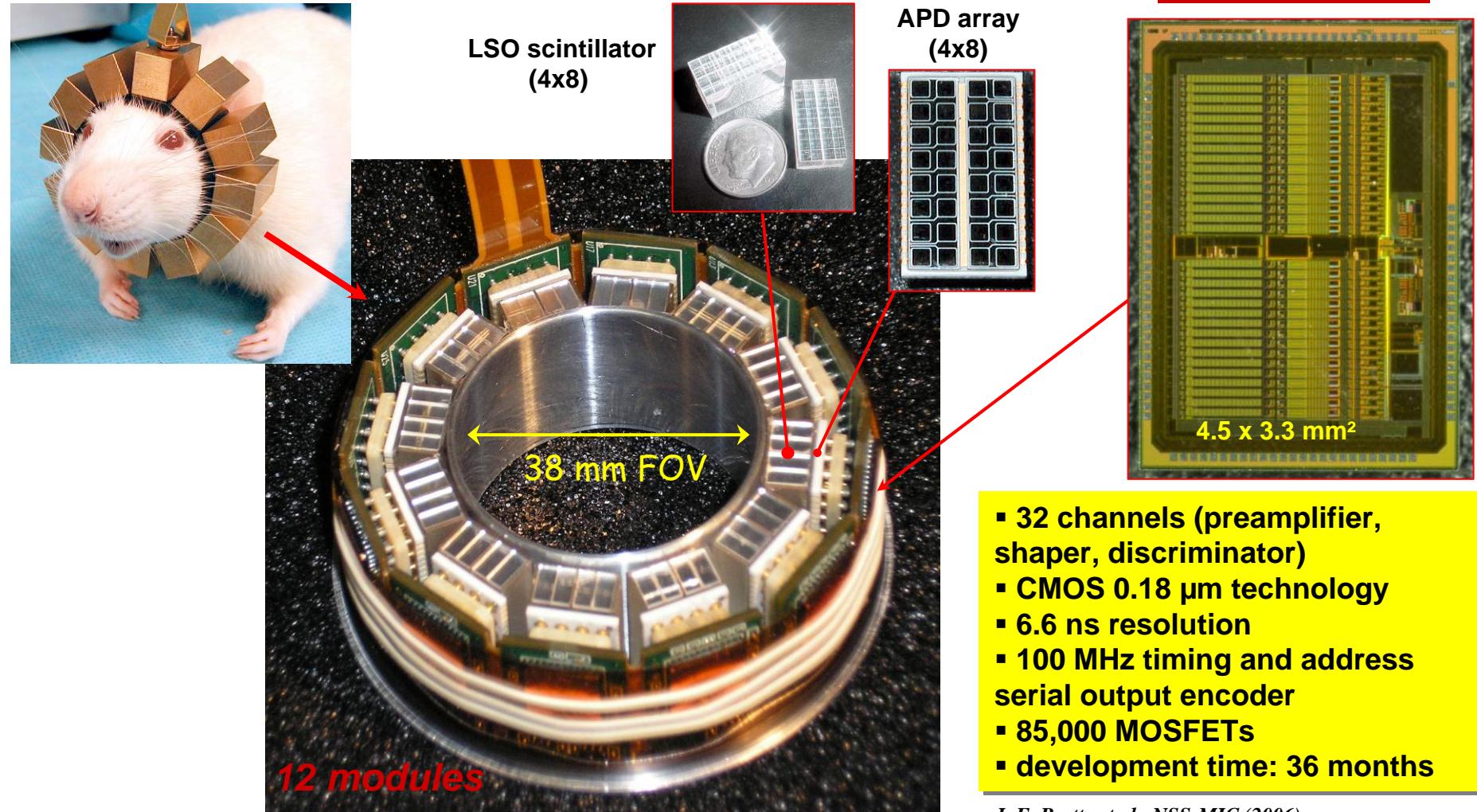
histogram of total  
charge deposited on  
the pads from the  $\alpha$   
tracks.



This detector will have a count rate capability two-orders of magnitude greater than any existing device due to unity-gain low-noise design

# ASIC for the Rat Conscious Animal PET (RatCAP)

## RatCAP ASIC

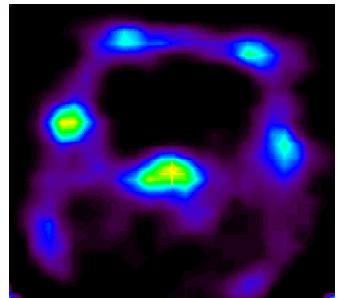


J. F. Pratte et al., NSS-MIC (2006)

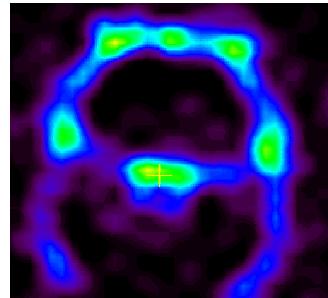
# RatCAP Progress, PET-MRI and Wrist Scanner

## RatCAP

$^{18}\text{F}$  fluoride bone scan, 1.3 mCi



RatCAP



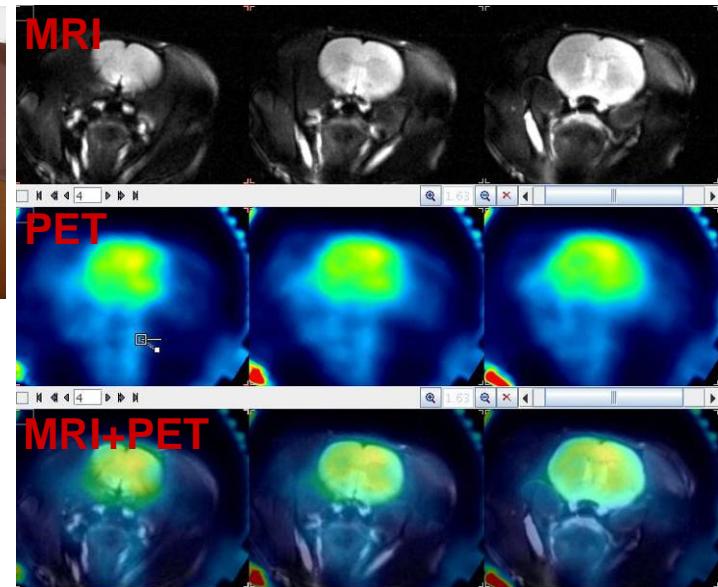
microPET R4  
commercial, non-mobile

## PET-MRI

rat brain images

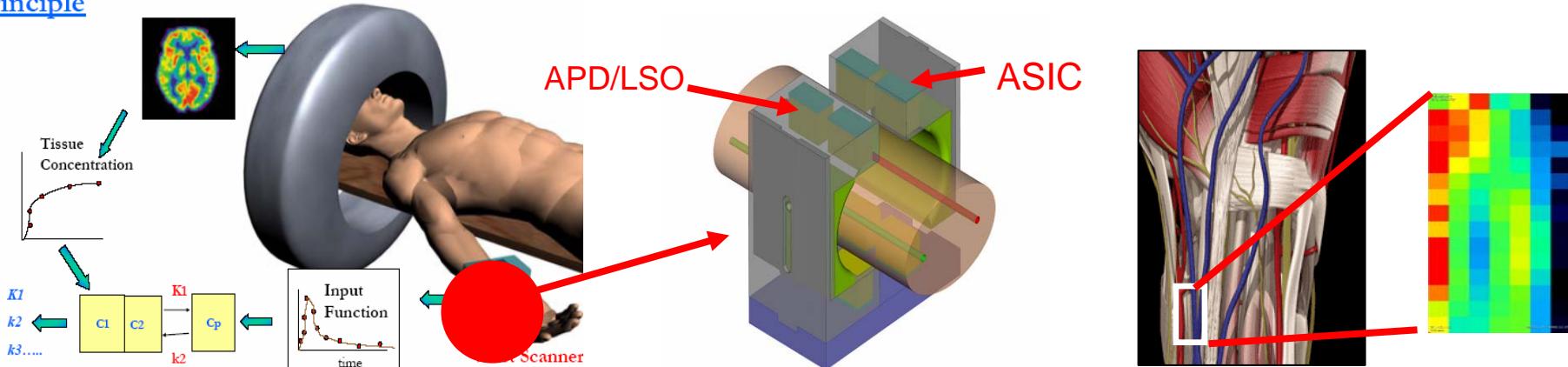


D. Schlyer et al., NSS-MIC (2006)



## Wrist Scanner

### Principle



Non-invasive measure of the radiotracer concentration

Summed planar image from 1 pair of detector blocks for the first 1 minute.

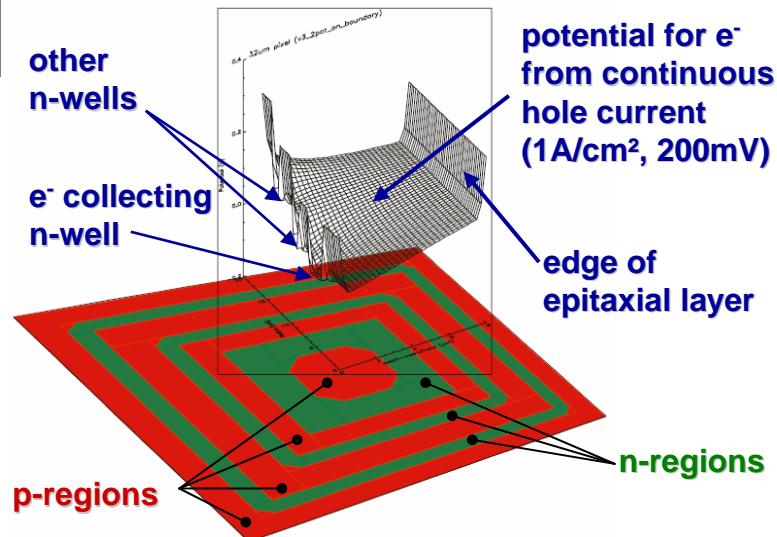
# Monolithic Active Pixel Sensors (MAPS)

## • “Field assisted” MAPS in bulk CMOS

BNL LDRD project - (P. Rehak et al.)

Continuous hole current provides drift field

- ✓ Improved CCE (collection in tens of ns)
- ✓ N- and P-channel MOSFETs available



## • MAPS in SOI CMOS

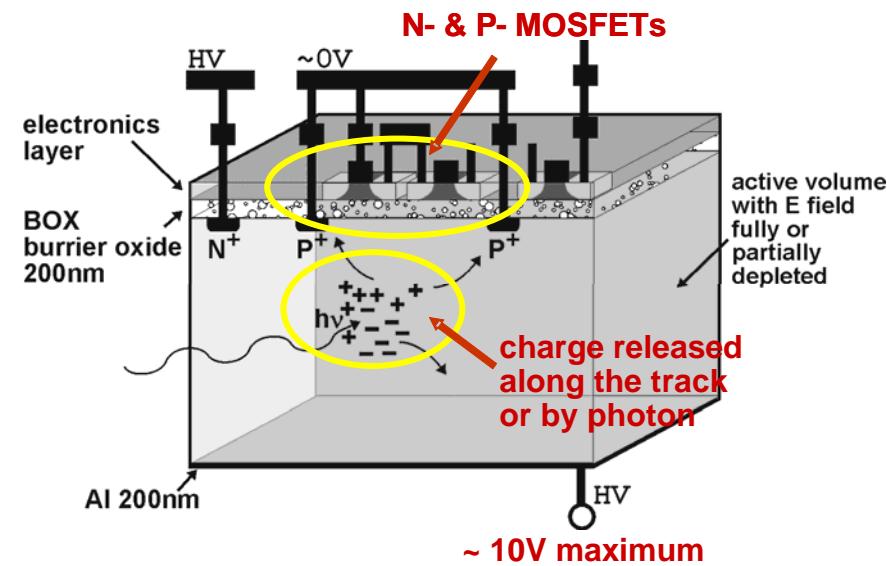
BNL-FNAL collaboration (G. Deptuch et al.)

Silicon on Insulator (SOI) technology

→ bonding wafers with low and high resistivity using Silicon oxide bond

- ✓ Improved CCE (active region 50 μm)
- ✓ N- and P-channel MOSFETs available

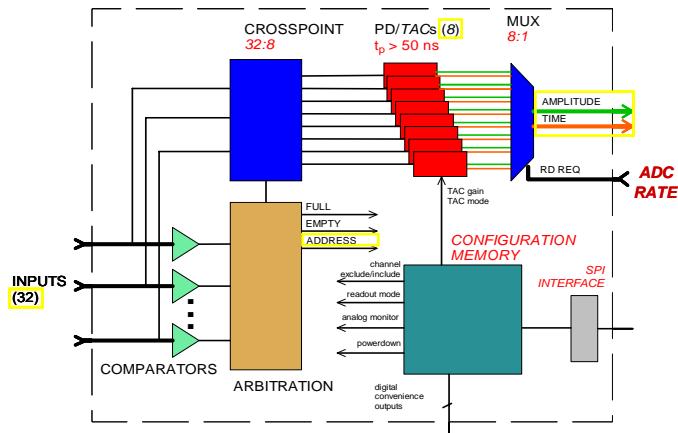
? mutual coupling an issue



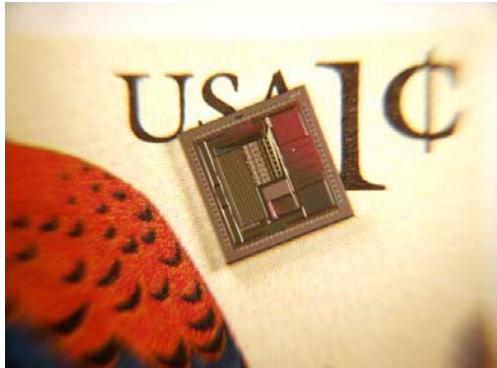
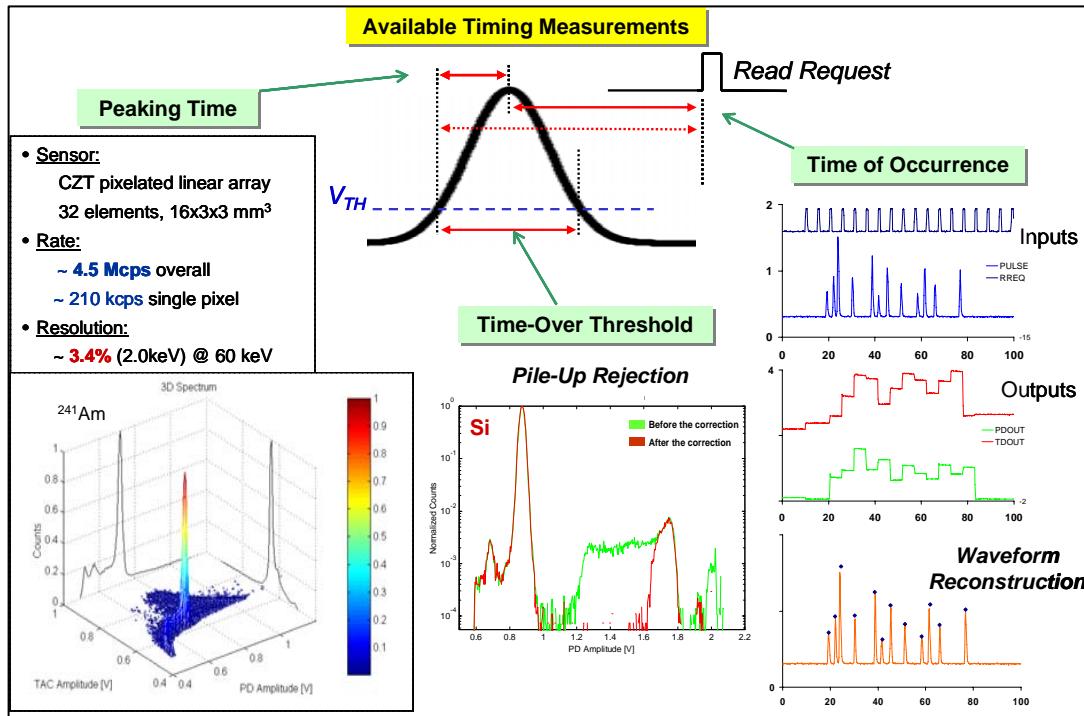
► Towards 3D Integrated Circuit Technologies

PDD ASIC for NSLS Experiments - Fluorescence Microprobes

# Peak Detector Derandomizer (PDD) ASIC

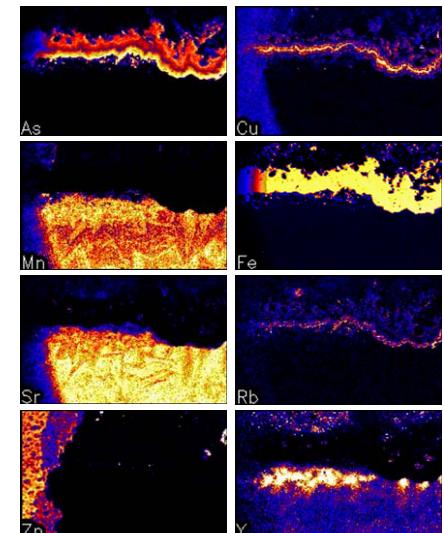
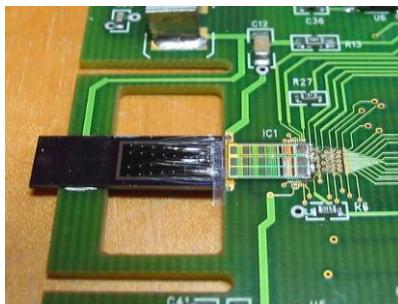


- 32:1 multiplexing of shaped input signals
  - amplitude, timing, address per event
  - self-triggering, sparse, derandomize



# Fluorescence Microprobe Results

# *Elemental mapping of Fiji Pyrite sample*



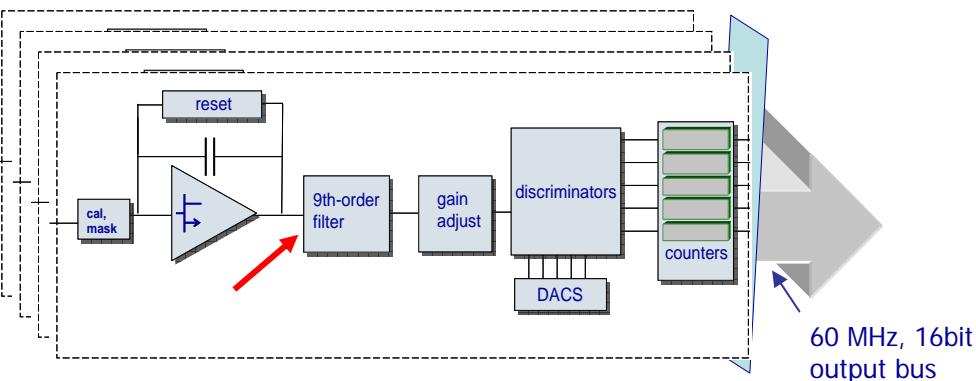
G. De Geronimo et al., NIM A484 (2002), NIM A505 (2003)

TNS 50 (2003), IEEE NSS Proc. (2005)

A. Dragone et al., NSS (2005) - P. Siddons et al. NSS (2006)

# ASIC for High-Rate Counting with Multi-Energy Discrimination

Collaboration with eV PRODUCTS (CdZnTe)

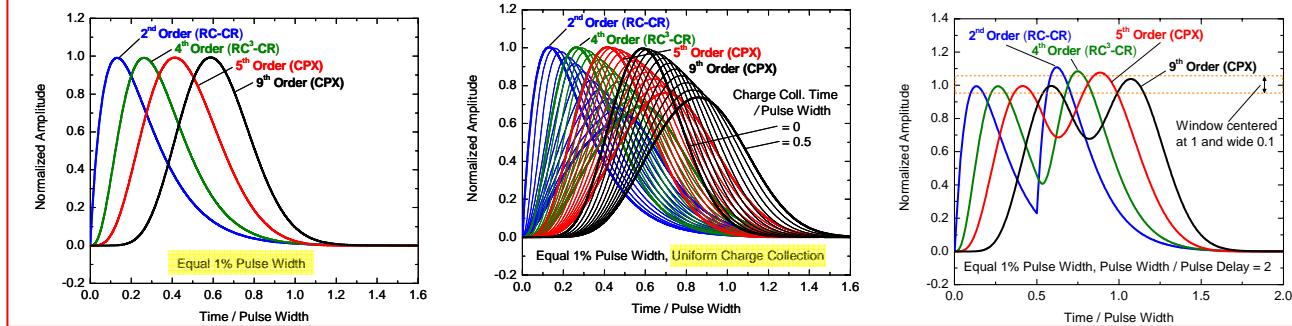


- 64 channels, each implementing:
  - low-noise charge preamplifier
  - **9<sup>th</sup> order shaper** 40ns - 360ns with BLH
  - settable coarse gain 8 mV/keV - 32 mV/keV
  - 5 x (discriminator + 16-b counter)
  - gain and offsets trimming (3-bit)
  - **simultaneous measurement and readout**
- five 10-bit DACs for thresholds
- 2048 registers, buffered analog monitors
- 0.25 $\mu$ m CMOS, 5 mW/ch., 600,000 MOSFETs



die photo, size: 6.6x6.6 mm<sup>2</sup>

## Impact of shaper order on resolution, ballistic deficit, pile-up



**Progress:  
delivered**

