

Detector R&D

D. Peter Siddons

NSLS Detector group

Inst. Div. Microelectronics Group

Inst. Div. Semiconductor Lab

CSIRO, Australia

Outline

- NSLS Detectors
- LCLS detectors
- Emerging Technologies for Sensor/ASIC Integration
- Requirements for NSLS-II Detectors
- Proposed R&D Plan

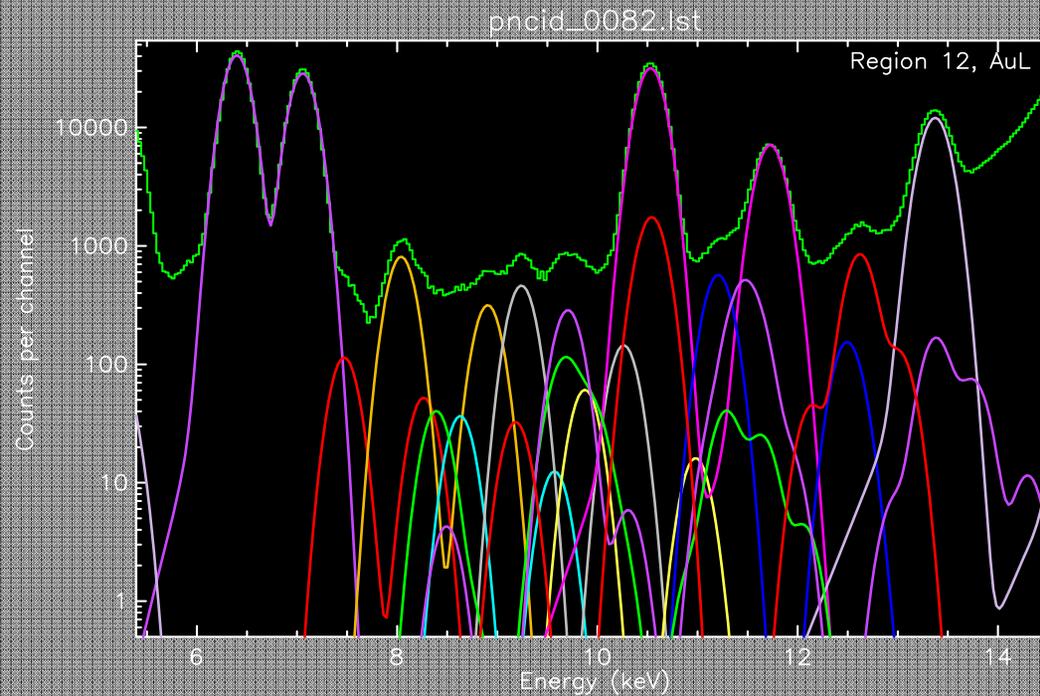
NSLS Detectors

- A series of detectors for selected SR applications has been developed over the past ~5 years
- Key technologies:
 - Silicon pad and strip detectors (Inst. Div.)
 - CMOS ASICs (Inst. Div.)
 - Packaging, fixturing, DAQ (NSLS)
- Significant performance advantages due to the ability to utilize highly parallel architectures

Need to unfold complex overlaps ...

Hough *et al.*, 2005

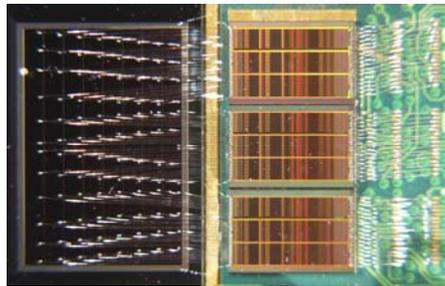
PNC-CAT, APS



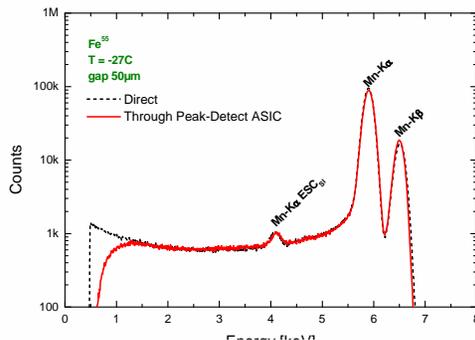
The MAIA Project



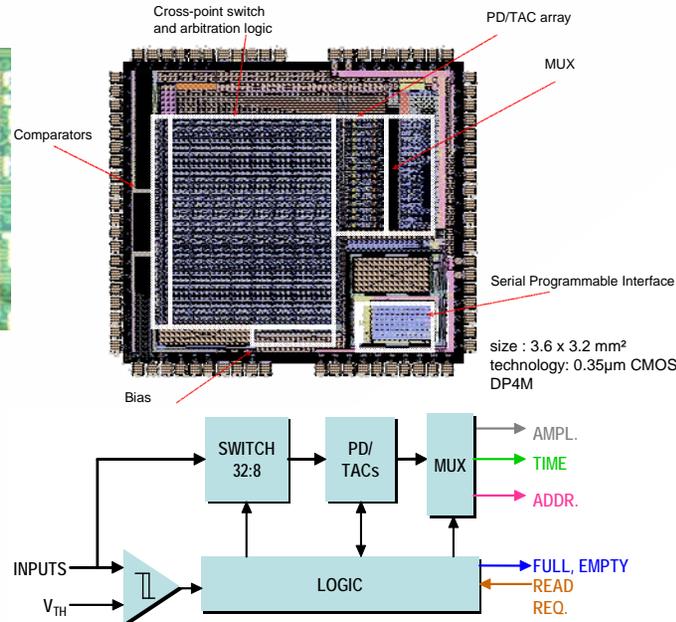
Si pad sensor



preamp/
shaper
ASIC



Peak detector – derandomizer
- multiplexer ASIC



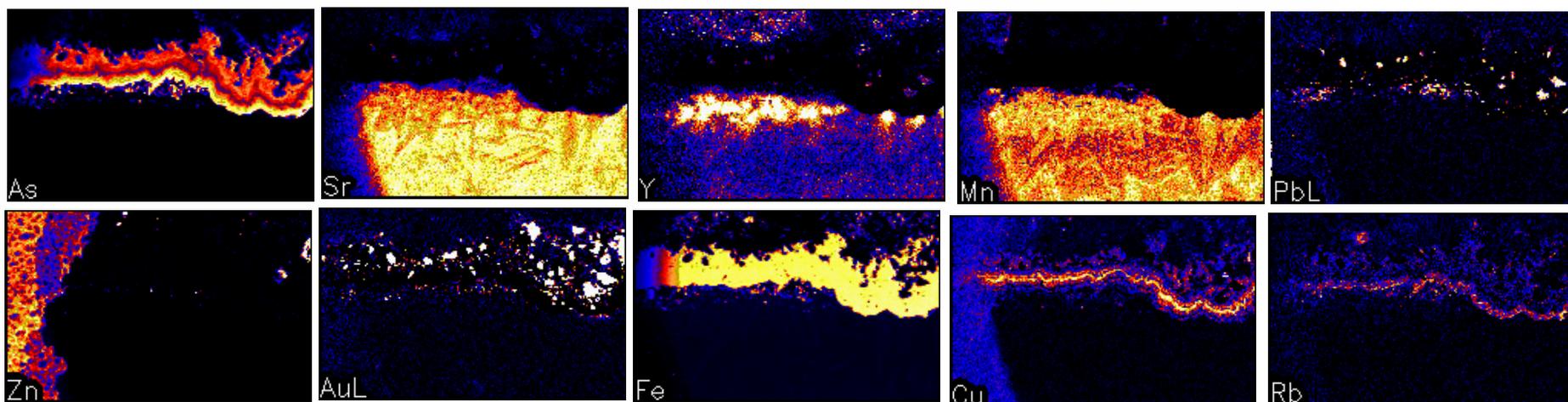
size : 3.6 x 3.2 mm²
technology: 0.35µm CMOS
DP4M

pipelined, parallel processor
and digitizer



- **Preamp/shaper ASIC** achieves 184eV resolution (Mn K α).
- 32-channel peak detecting derandomizer and multiplexer with time-over-threshold for pileup rejection.
- Metal absorption mask demonstrated to control charge sharing between detector elements.
- Close coupling of data acquisition from stage control for fast scanning (XY sampled into data stream).
- **Dynamic Analysis** method demonstrated for imaging of SXRF data off-line (APS sector 2; PNC-CAT, sector 20).
- DA real-time deconvolution demonstrated at **10⁸ events/second** using HYMOD.

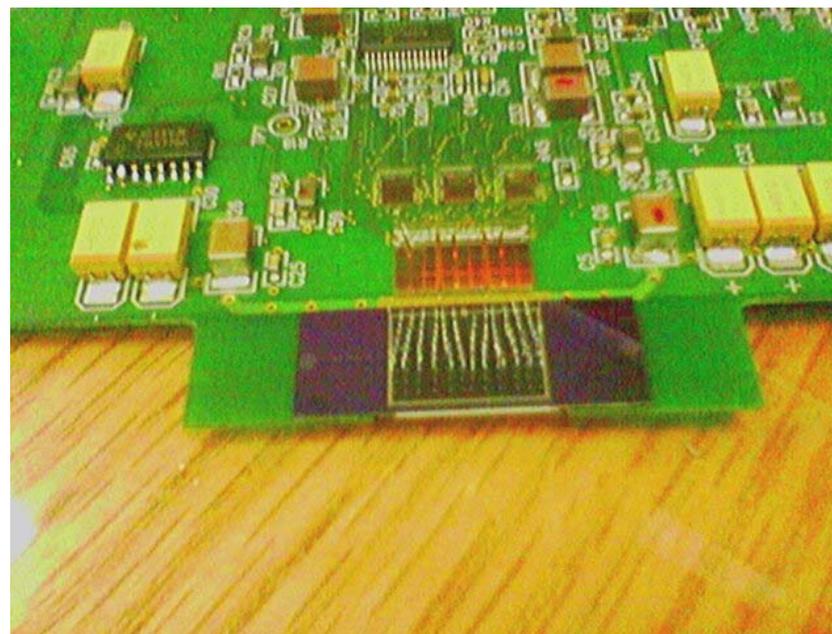
Rapid XRF Elemental Mapping (BNL/CSIRO collaboration)



- Prototype experiment using 32-element silicon detector and BNL's readout ASIC plus CSIRO fast processing hardware and software at NSLS X27A beamline.
- These X-ray elemental images of a sample of Fiji pyrite were collected in "Maia 32 - HYMOD data acquisition" format and the data reduced at National Synchrotron Light Source, BNL.
- The event data were analyzed using the CSIRO Dynamic Analysis method, which enables quantitative, true-elemental images to be un-mixed from the generally complex PIXE/SXRF energy spectrum.
- 800 x 500 pixels of 10um x 10um, collected in about 5hrs. This is extremely fast for such a large pixel array.

Recent upgrades

- 96 element Maia system
 - 3 improved Hermes ASICs
 - 3 Scepter ASICs
 - 96-pad sensor
 - Single Hymod-II analysis board
 - Integrated stage scanning



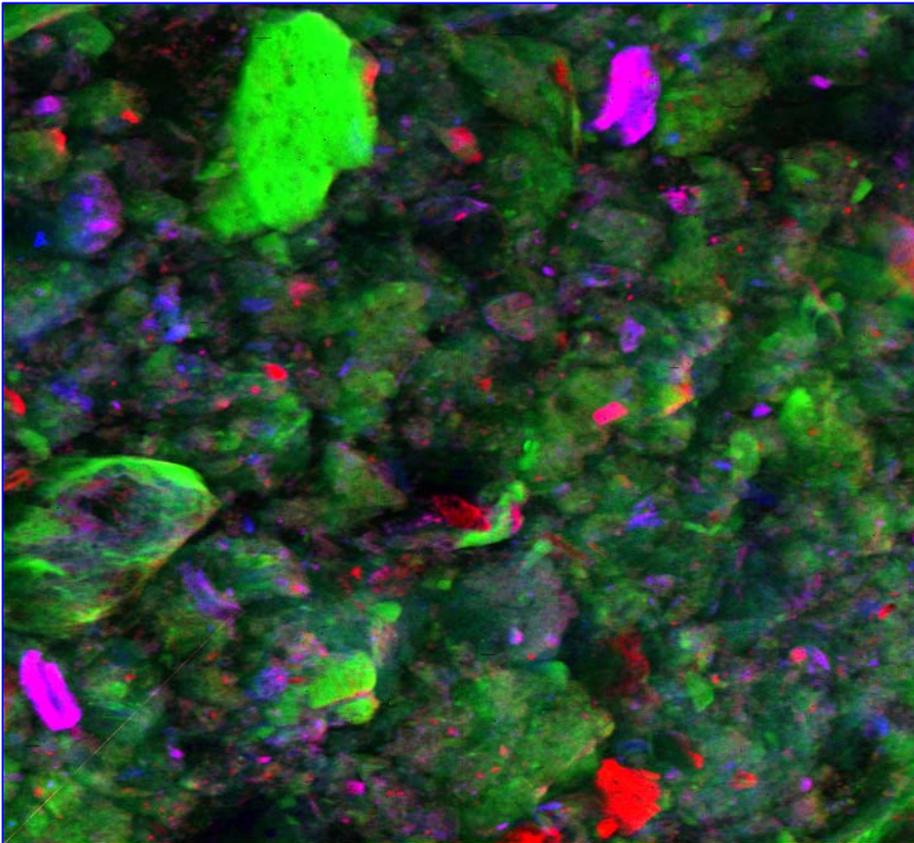
Tests of the Maia-96 system

Some examples from NSLS **September 2007 experiment**

*96 detectors (3 x Hermes, 3 x Scepter)
HYMOD2 processor and fast ADCs
Drive stage XY (up to 10 mm/s)*

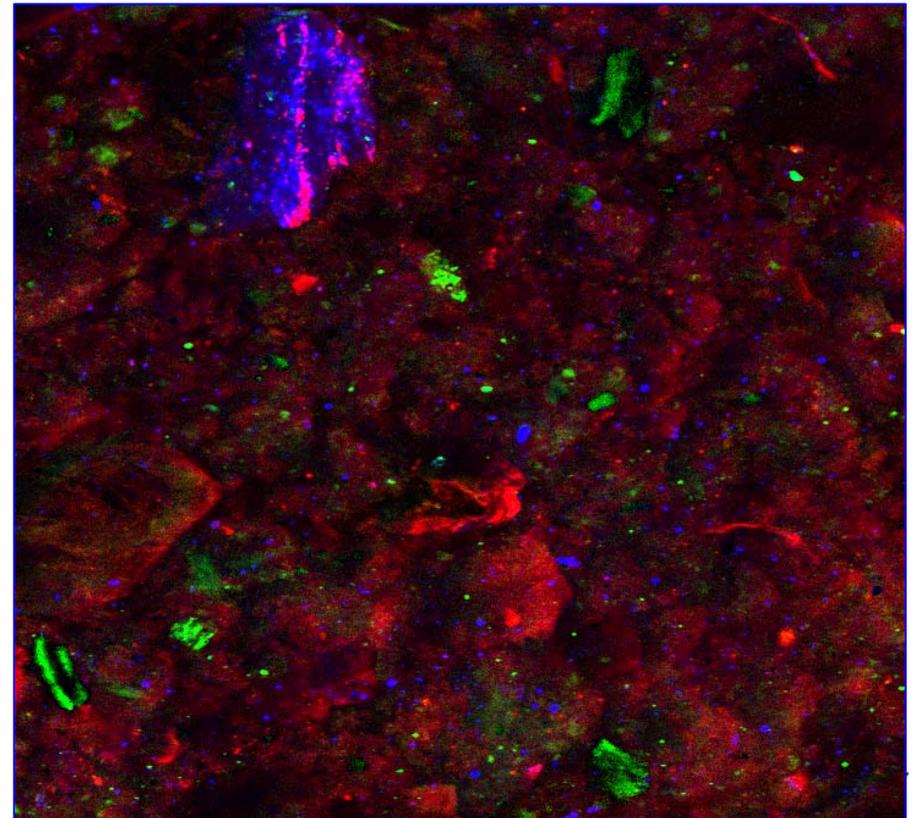
Short run (#297): Rock sample, Stawell Vic, Australia

1467 x 1467 pixels (11 x 11 mm²)
6 hours (10 ms dwell per pixel)
7.5 x 7.5 μm² pixels



Fe-Rb-As RGB composite

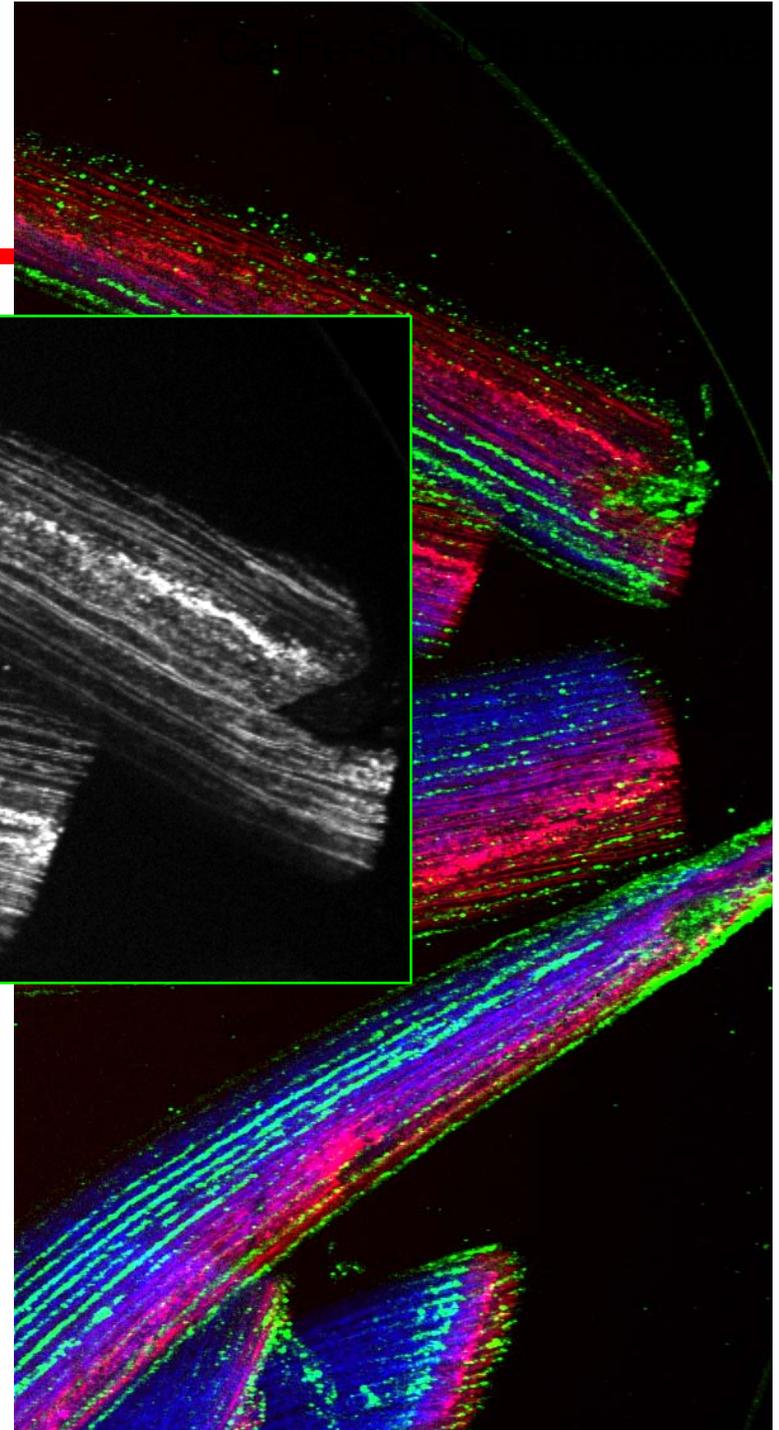
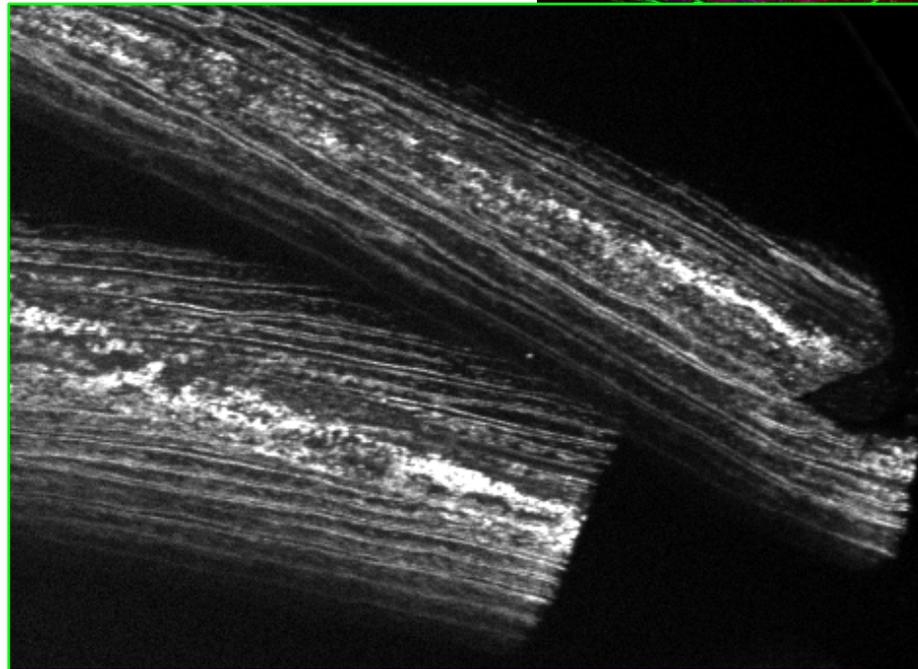
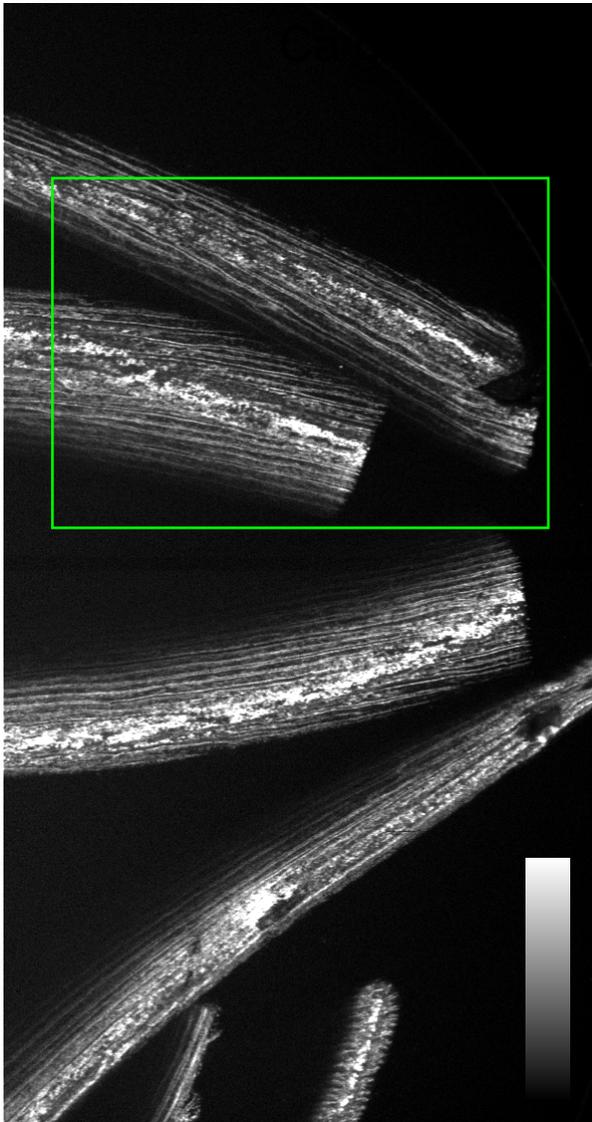
Zn-Pb-Y RGB composite



Tests of the Maia-96 system

Some examples from NSLS **September 2007 experiment**

Long run (#295): Acacia stems, Western Australia



1200 x 2267 (9 x 17 mm²)
5.7 hours (7.5 ms dwell)
7.5 x 7.5 μm² pixels

Tests of the Maia-96 system

Some examples from NSLS **September 2007 experiment**

Long run (#204): Iron-oxide nodules, Rose Dam, WA

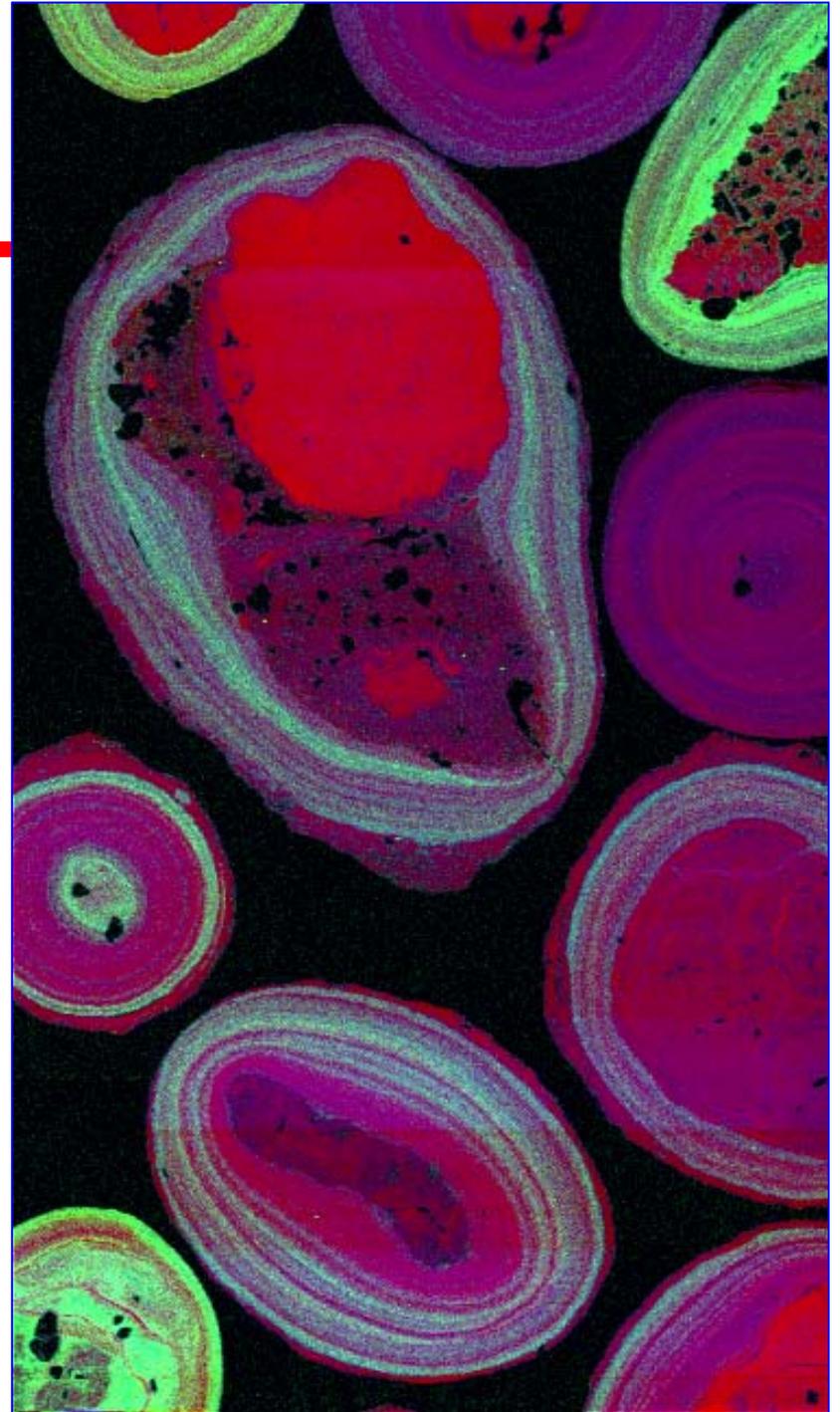
1625 x 2625 pixels (13 x 21 mm²)

6.3 hours (**5 ms dwell** per pixel)

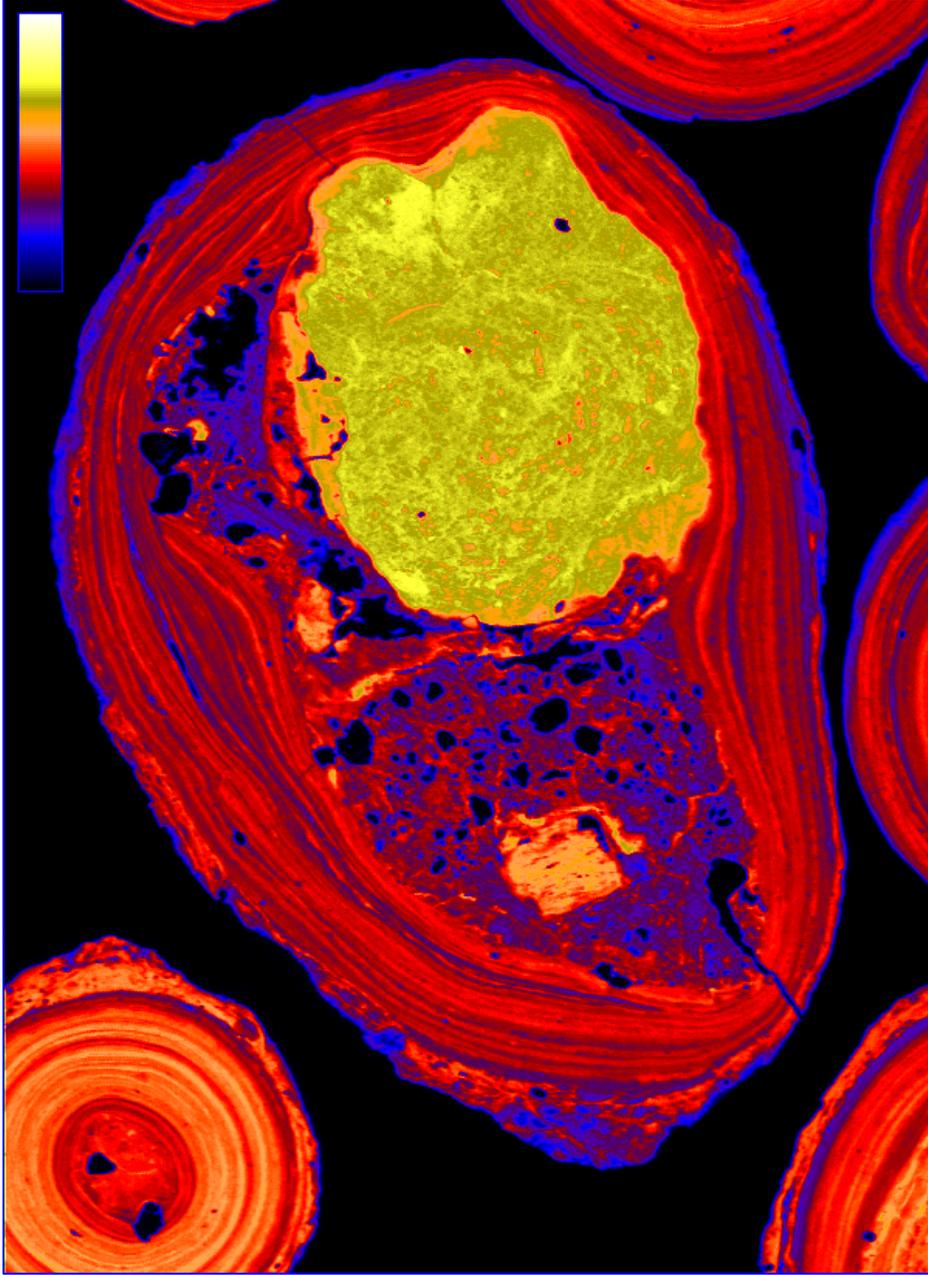
7.5 x 7.5 μm² pixels

0-2 MHz count rates → good image counting statistics

Fe-Y-Cu RGB composite



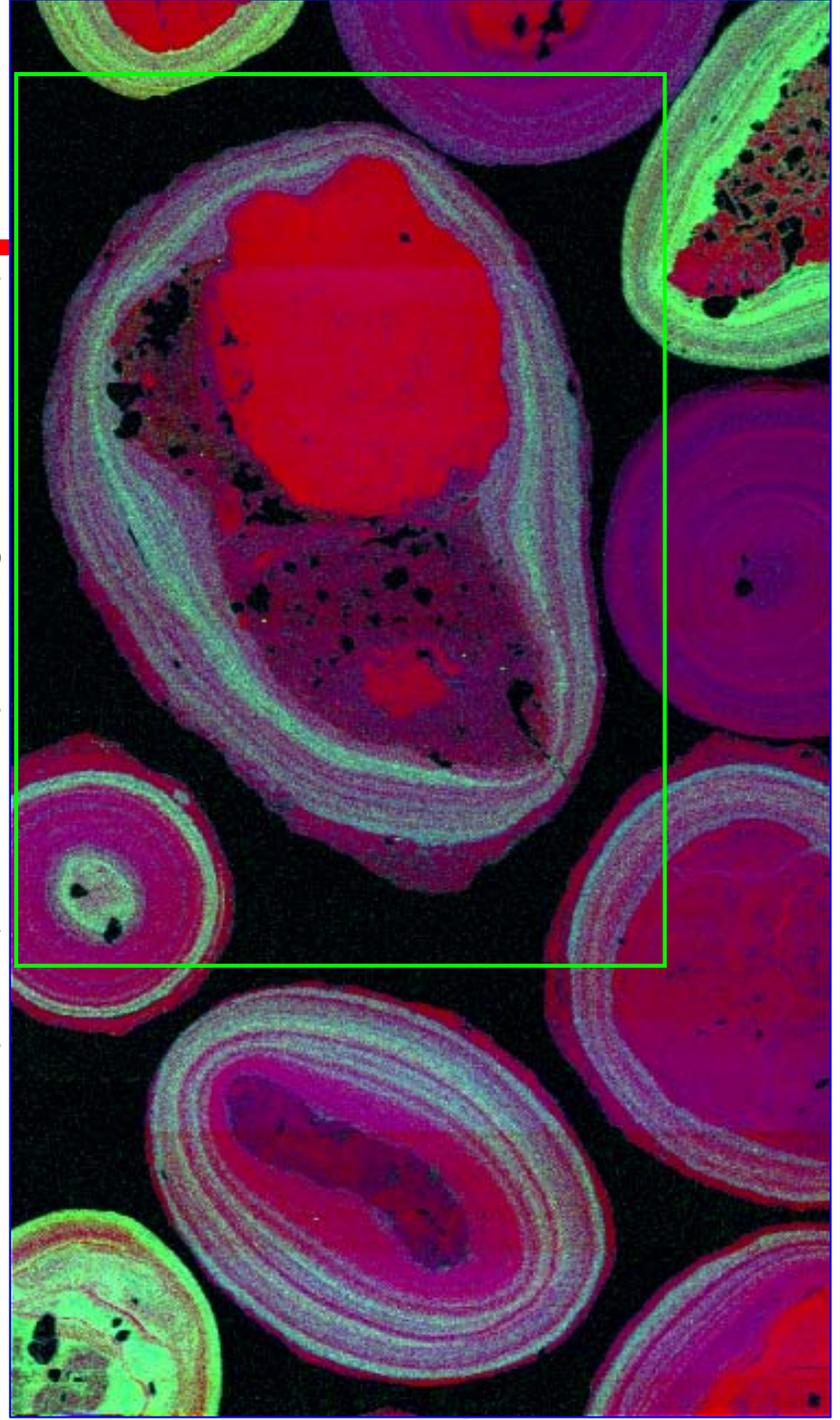
Tests of the Maia-96 system



Iron oxide nodules, Rose Dam WA

11

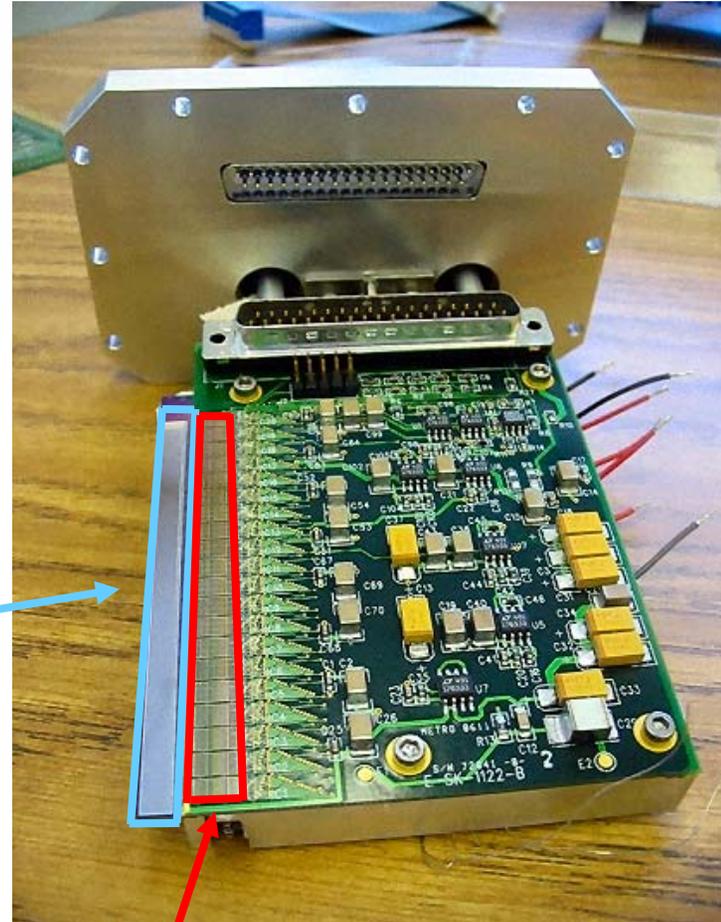
Fe-Y-Cu RGB composite (1500 x 2624 pixel images, 13 x 21 mm²)



Detector for Diffraction Applications

- 80mm long silicon PSD
- 640 channels, ASIC readout
- 125um pitch
- 4mm wide
- 0.4mm thick
- 350eV energy resolution @ 5.9keV

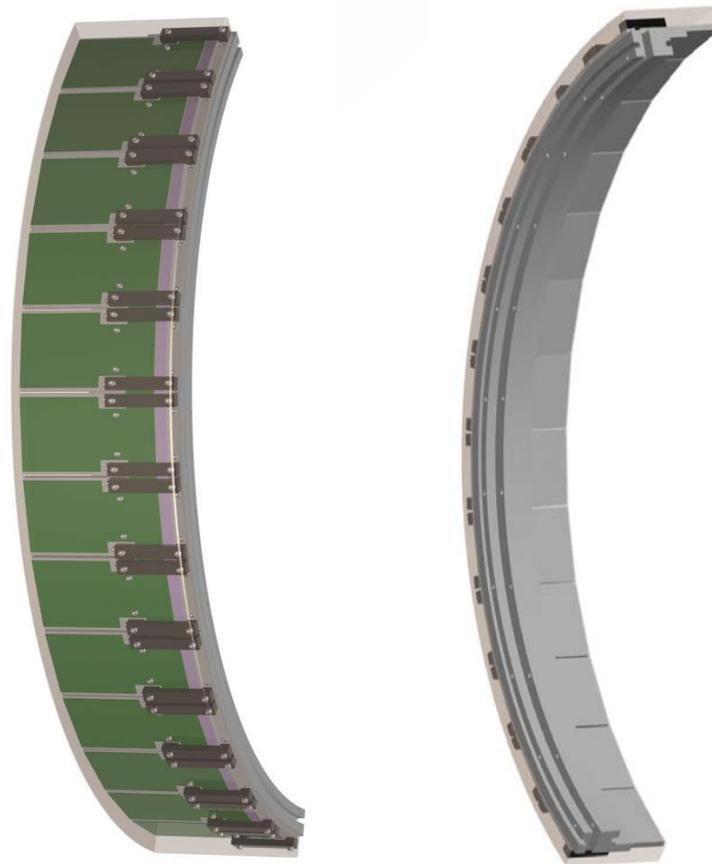
sensor



20 ASICs

Large array for NSLS

120 degrees
~7000 channels
0.014 deg. Resolution
~1ms readout time
~350eV energy
resolution



LCLS detectors

Imaging detectors

- Integrating detectors because of LCLS time structure
- Large dynamic range (detector #1)
- Very low noise (detector #2)

XAMPS Pixel structure

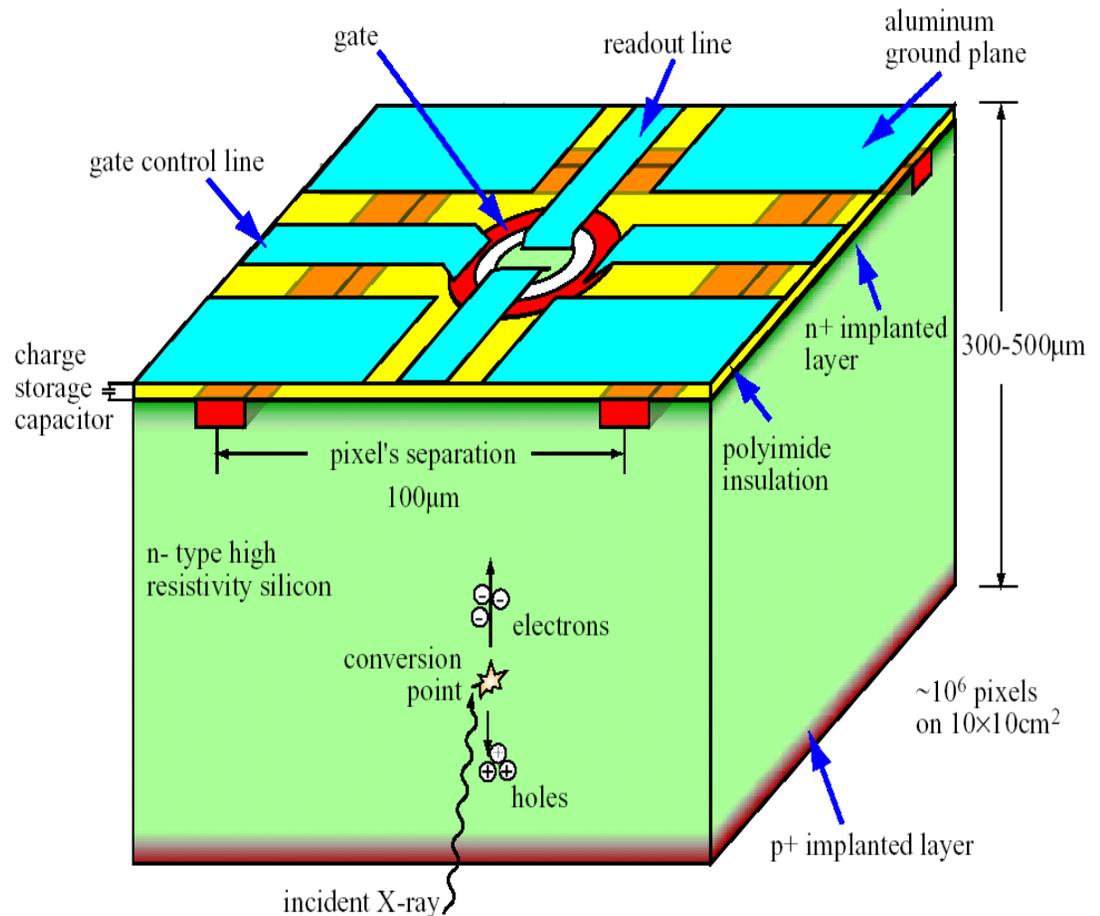
Low-resistivity n+ layer is formed by deep implant.

JFET switches are fabricated in this layer

Charge is produced by photo-ionization

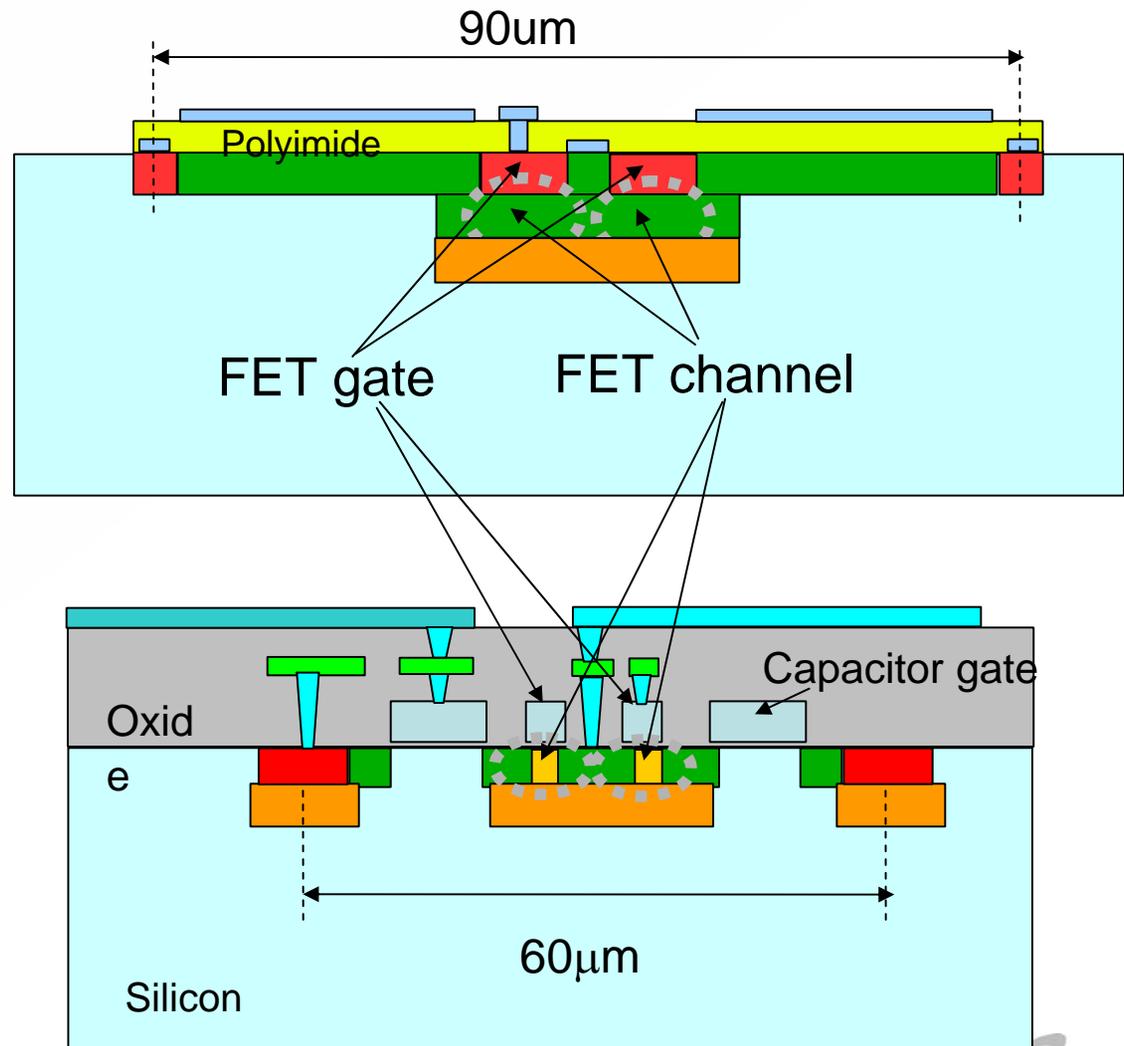
Electrons collect under pixel (switch is OFF)

Charge is read out by turning transistor ON, connecting stored charge to a buss-bar, and read out by a charge-sensitive amplifier.



JFET vs MOSFET structure comparison

- Both start with high-res. wafer, but BNL's is known good, IBM's is unproven.
- Both make implants on both sides of the wafer
- BNL's process needs careful alignment between layers
- IBM's process is self-aligning for several key layers
- If successful, IBM's process allows more complex circuits to be designed than BNL's



Readout system

Row-by-row readout, 1us/row

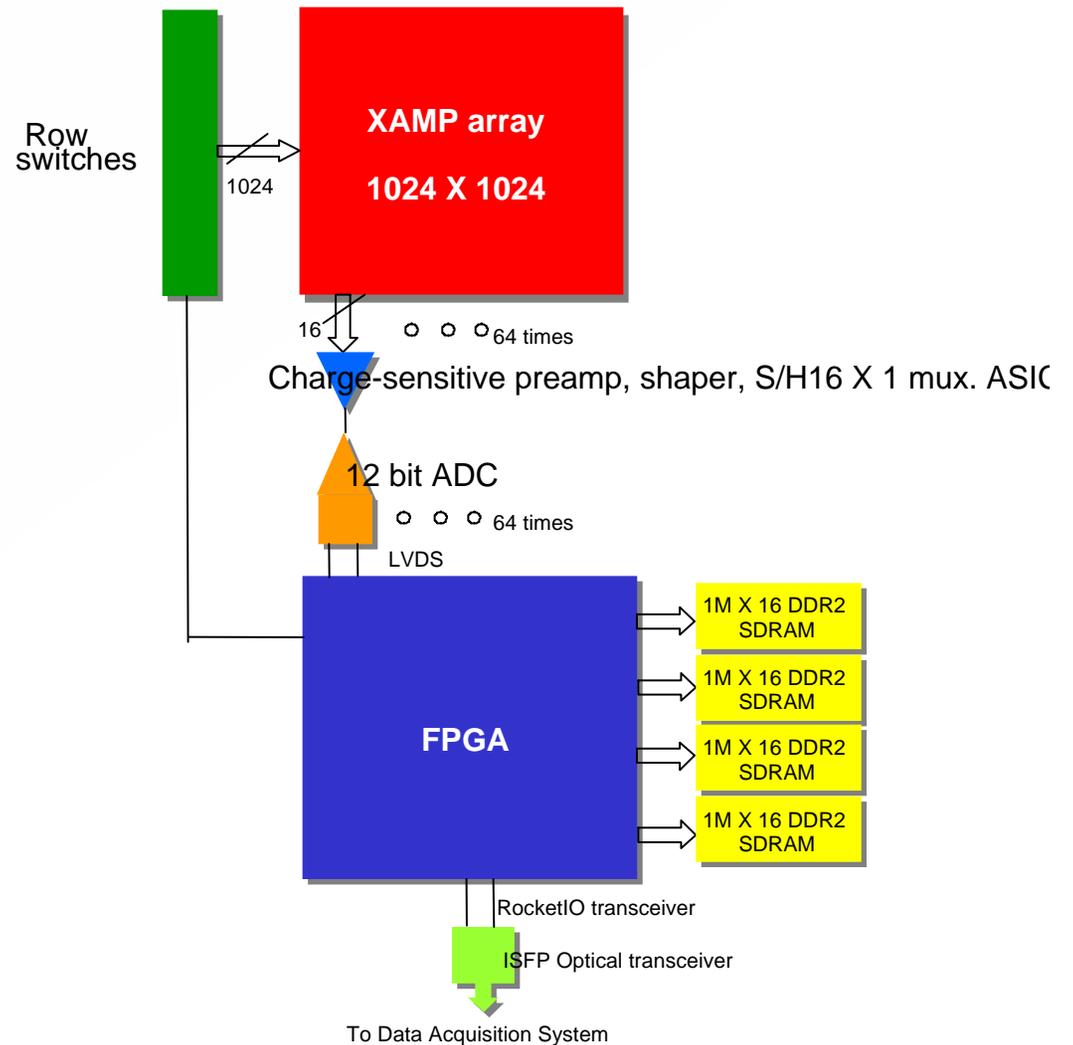
8 Fast (>20MHz) 8-channel
ADC's multiplexed e.g. x16
columns = 1024

2GB/s instantaneous raw data
from ADCs

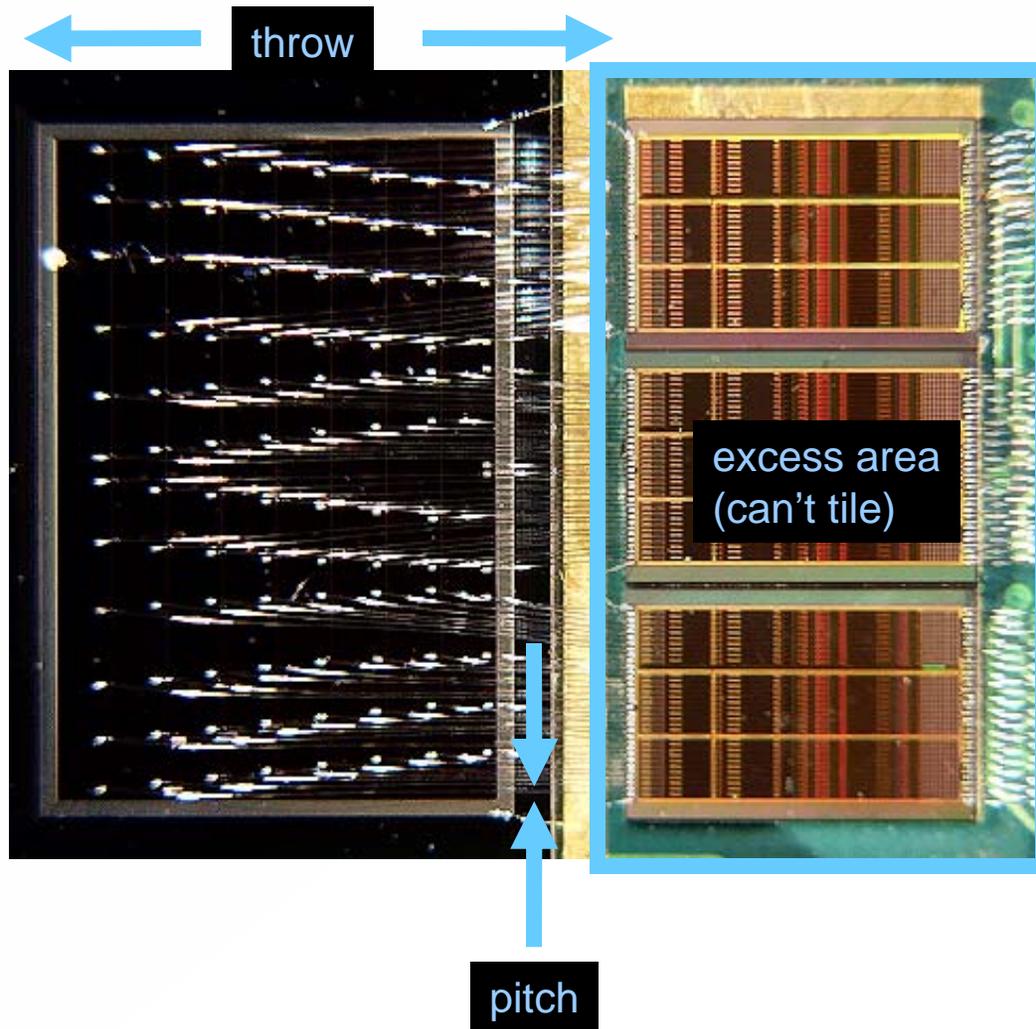
250MB/s averaged, i.e. to be
stored, based on 120Hz
cycle. More if rep. rate is
upgraded.

Data streamed through FPGA
to fast memory and terabyte
disk store.

- FPGA does background correction



Limitations of Wirebonded Interconnection



NSLS-II detectors will require:

- larger area
- finer pixels
- mosaic construction

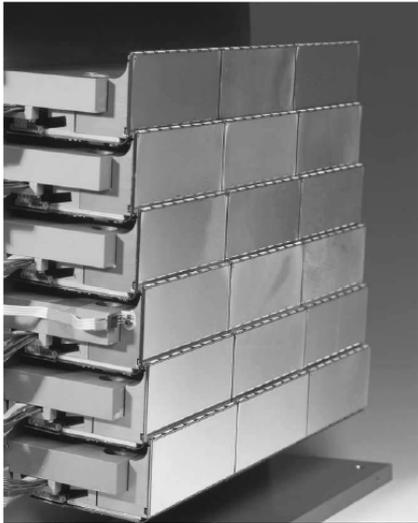
Monolithic Approaches for Sensor/ASIC Integration

- Common Technology
 - sensor in CMOS process (MAPS)
 - transistor in sensor process (DEPFET, XAMPS)
- Charge-Shifting
 - capture charge in a potential well and physically move it to output port (CCD, CDD)
- Physical Connection
 - bump bonding (PbSn, In)
 - direct wafer-wafer bonding

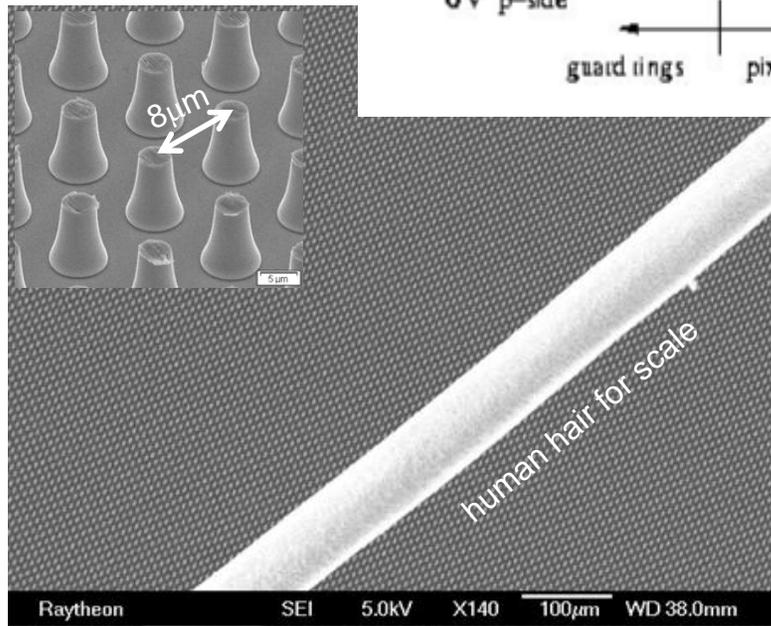
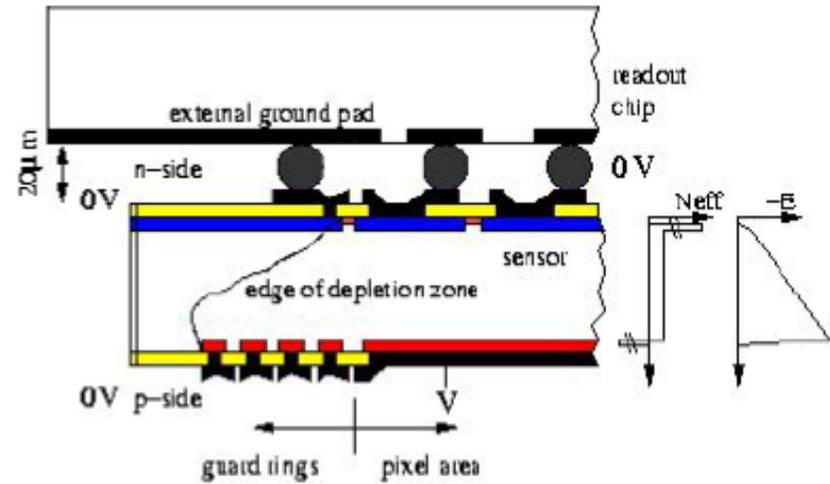
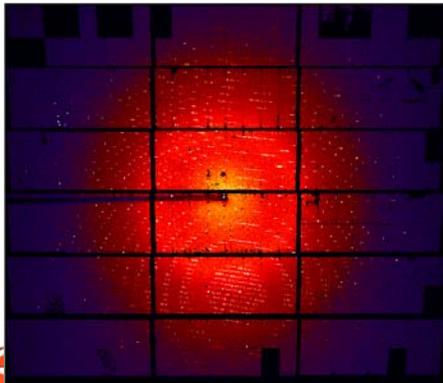
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 - **direct wafer-wafer bonding**

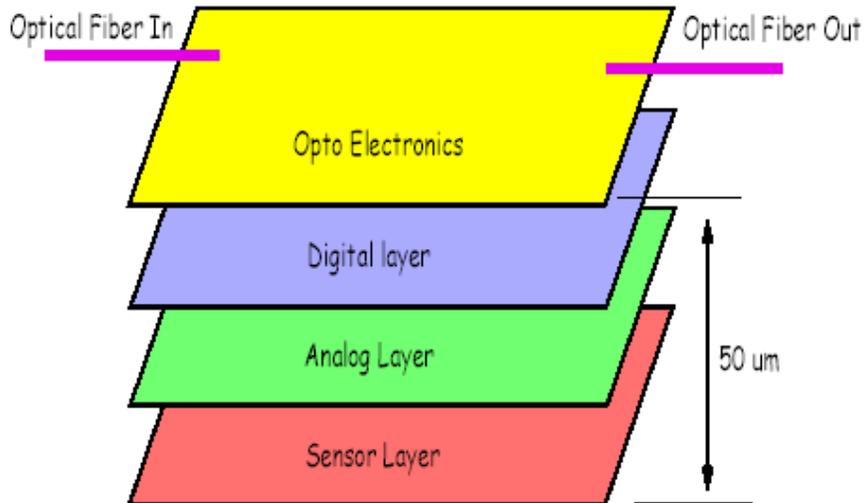
Bump-bonding: Examples



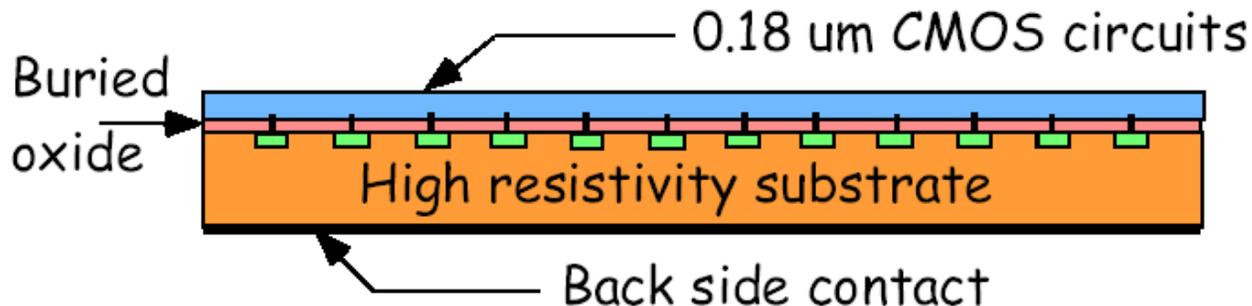
PILATUS 1M
Swiss Light Source
XXMpixels



direct wafer-wafer bonding



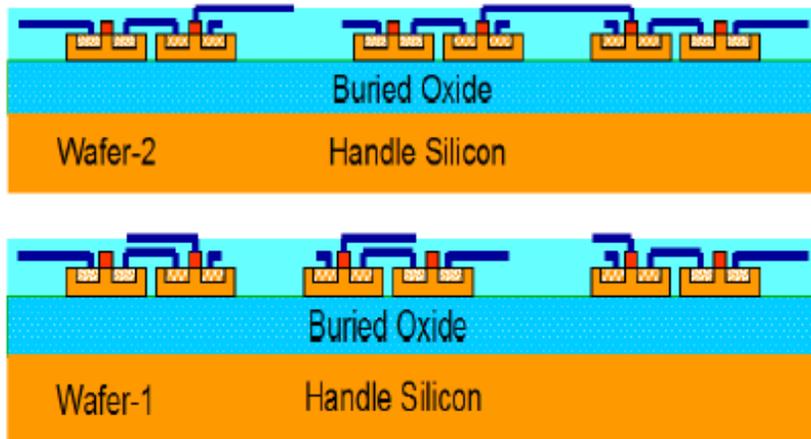
- Ultimate goal is monolithic integration of any technology
- Immediate push in industry is for reducing wireload distribution in digital ICs
- Science applications being pursued in optical/IR imaging, HEP tracking
- FNAL and KEK have active HEP designs
- Processes available at Lincoln Labs, JPL, OKI Semiconductor, IBM (?)



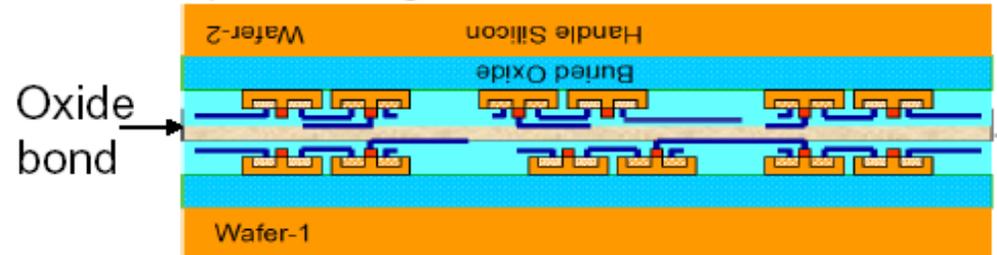
Process flow for 3D Chip

- 3 tier chip (tier 1 may be CMOS)
 - 0.18 um (all layers)
 - SOI simplifies via formation
- Single vendor processing

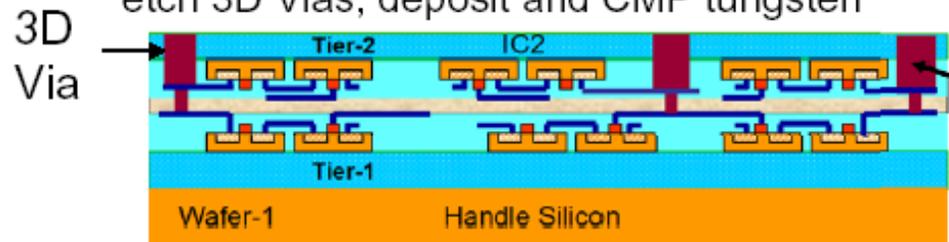
1) Fabricate individual tiers



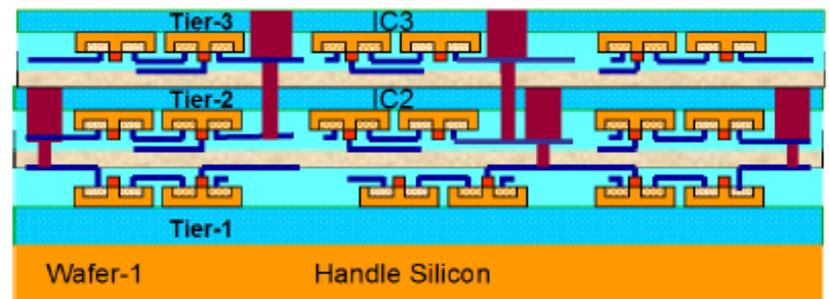
2) Invert, align, and bond wafer 2 to wafer 1



3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



Goals for BNL SR Detector Development

A 'monolithic' photon-counting pixel detector

- 3D version of Pilatus
 - Smaller pixels
 - Better yield

A pixelated detector with spectrum-per-pixel

- Simultaneous spectroscopy/diffraction detector
- energy and spatial resolution
- Laue diffraction
- x-ray microprobes with microdiffraction and fluorescence analysis on the same sample position with the same detector

A pixel detector with multiple-tau time autocorrelation electronics on each pixel

- megapixel detector with on-pixel correlators can provide sufficient sampling density to access the sub-microsecond domain
- 3D technology will provide the necessary integration density

A Monolithic Photon-counting pixel detector

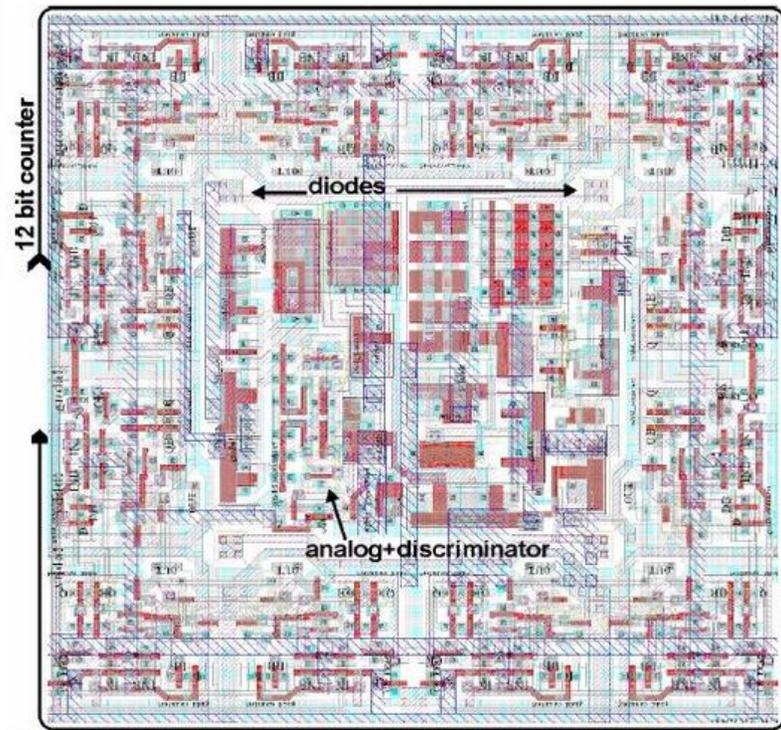
26 x 26 um (G. Deptuch, 2006)

- 280 transistors
- Built using standard SOI CMOS
- Impossible to properly prepare 'detector'.

Bonding CMOS and sensor after sensor implant gives full control over interfaces

60 x 60 um pixel would allow ~1500 transistors

- Better analog circuits
- More bits
- Double-buffering (no dead-time for readout?)



R&D Plan

- None is planned as part of NSLS-II program
- Independent proposal to DOE is imminent
 - It will propose to research the 3D concept in collaboration with IBM, with the three detectors outlined above as end goals.
 - 6-year program
 - Significant cost
 - 3 IBM FTEs + 5 BNL FTEs
 - ~\$1M/year non-FTE expenses

Beamline R&D

- Photon BPMs
 - Many beamlines are specifying very tight beam stability requirements
 - Part of responsibility to control that will fall on beamline optics
 - Need photon BPM capable of 0.1um measurement accuracy
 - None currently exist
- IO monitors for microprobes
 - Some of most demanding stability requirements come from nanoprobes and such.
 - Particularly difficult for soft x-ray zone plate instruments
 - Destructive
 - No space
- These R&D costs ARE part of the project