

Front-End Electronics for the Silicon Partition of the Phobos Detector at RHIC

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Abstract--The Phobos experiment at the Relativistic Heavy Ion Collider (RHIC) at Brookhaven National Laboratory uses silicon pad detectors to measure charged particles from Au-Au collisions. We describe here the front-end electronics which instruments the 135,000-channel silicon partition of the detector. The system records pad "hits" and 12-bit pulse height data for later reconstruction of charged-particle trajectories, and for identification of particle species using the dE/dx method. The compactness of the detector puts challenging spatial and power dissipation constraints on the design of the electronics; the proximity of the silicon sensors and front-end chips to the heavy ion collisions presents a challenge in terms of dealing with latchup. We describe the design features of the principal elements of the front-end including the silicon detector modules, the front-end controller, and the data concentrator. The performance of the system and our experience with the latchup protection during the first two physics runs are presented.

I. INTRODUCTION

The Phobos experiment at RHIC is searching for new states of matter in heavy ion collisions at a center-of-mass energy of 200 GeV per nucleon pair. The detector is designed to measure the multiplicity of charged particles produced in these collisions, and to track and identify a small subset of the particles. It performs these tasks using an array of silicon pad detectors. The silicon is distributed in a multiplicity detector which provides 4π coverage, a vertex locator, and two spectrometer arms. Additional information for charged particle identification is provided by a 960-channel, scintillator/phototube, time-of-flight system. A detailed description of the apparatus can be found in [1].

The front-end electronics for the silicon partition serves 135,000 channels: 56,000 channels in each of two spectrometer arms, and 23,000 channels in multiplicity and vertex detectors. Because of projective geometry and the differing needs in the spectrometer, multiplicity and vertex systems, the physical form of the detector modules varies somewhat throughout the detector. The various requirements are met using modules which have from one to four sensors served by as many as sixteen, 64- or 128-channel front-end chips.

Despite this marked variation in its physical form, the front-end system has a uniform readout structure comprised of the elements shown in Fig.1. A detector module, composed of silicon sensors and front-end chips on a hybrid, connects via a short cable to a nearby front-end controller. The controller digitizes the event data and sends it via G-Link to a data concentrator; the latter collates the event data into serial streams and transmits them over optical fibers to the data acquisition (DAQ) system [2]. Together the front-end and DAQ systems handle event rates up to 200Hz with raw data of 260kB/event, and the DAQ system sends data to the RHIC central data storage system at a sustained rate of 30MB/s. Zero suppression of the data is presently handled off-line.

The following sections of the paper cover the design features of the different system components in the front-end electronics. In particular we describe how the challenges posed by spatial and power dissipation limitations are met; how the high data rate is handled; how the system is partitioned for the safety of the silicon detector modules; and how the problem of latch-up is handled.

II. DESCRIPTION OF SYSTEM COMPONENTS

A. Silicon Detector Modules.

The silicon sensors are single-sided and cut from 100-mm wafers. A minimum ionizing particle (MIP) traversing one of these 300 μm -thick sensors releases a charge of about 3.6 fC. The sensors [3] all have approximately the same active area but, in terms of the number and shape of pads, they vary markedly throughout the detector because of their function and distance from the interaction region. In the multiplicity detector a module consists of a single sensor attached to a 4-layer printed circuit board which carries a single front-end chip. The detector modules serving the vertex detector and spectrometer arms are composed of multiple sensors attached to hybrids; the latter are 6-layer thick-film circuits on alumina substrates which carry the front-end chips. Examples of the spectrometer modules are shown in Fig. 2.

1) Front-end chips

The front-end chips are from the commercially-available line of VA integrated circuits [4,5,6]. These chips have a dynamic range of 100 MIPs and are configured in 64- and 128-channel versions. A partial, functional block schematic of

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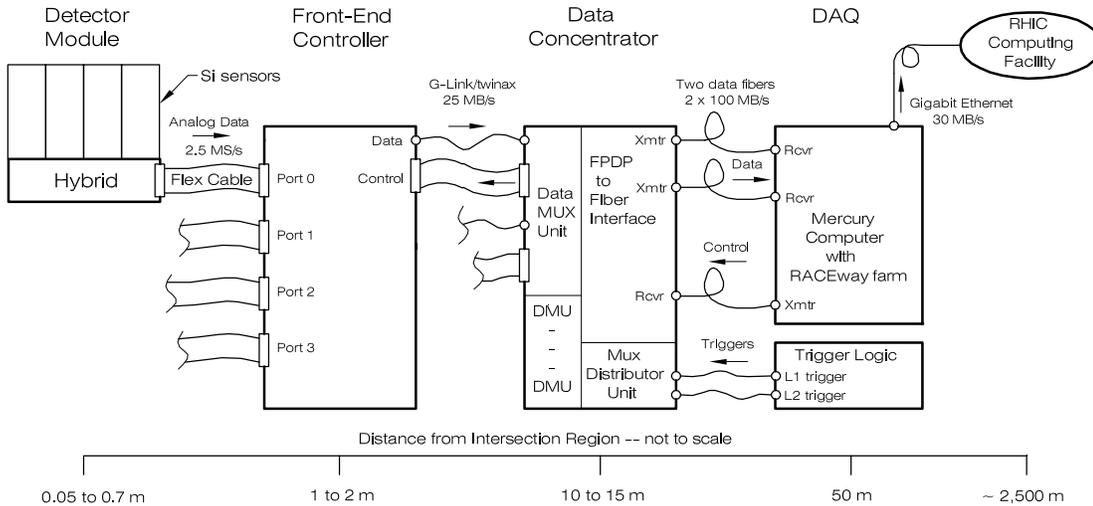


Fig. 1. Block schematic of Phobos readout system.

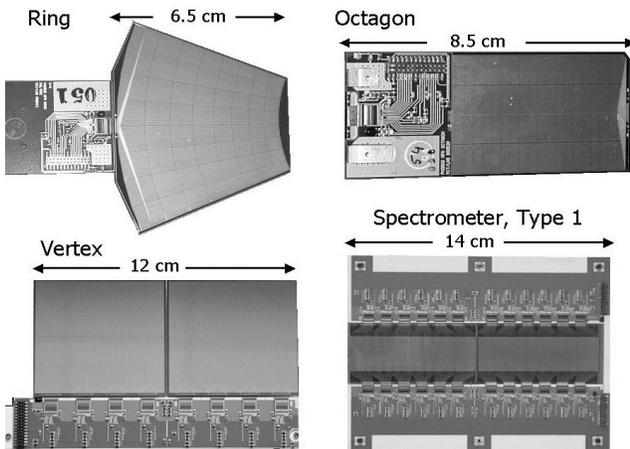


Fig. 2. Examples of Phobos silicon pad detector modules.

the chip is shown in Fig. 3. Each channel of the chip contains a charge-sensitive pre-amplifier; the charge integration peaks in 100 ns with a 10 pF source capacitance, and the decay time constant is adjusted to at least 50 μ s. The pre-amplifier is followed by an RC-CR shaping stage, with peaking time of 1.1 μ s, and a track-and-hold stage. A suitably delayed version of the event trigger switches the chip from track to hold to capture the peak of the signals on their respective hold capacitors. During readout an output control shift register (not shown) sequentially selects the hold capacitor in each channel and connects it to the output stage which drives differential output currents onto the analog bus. The output is enabled only when there is a "1" present in the shift register. The "Shift_out" from the shift register feeds the "Shift_in" input of the next chip. A second shift register (not shown) on the chip is invoked only during test/calibration. The calibration step input signal (0 to 190mV max.) is fed via an off-chip, 2 pF calibration capacitor to an internal bus on the chip, and the test shift register connects this bus to each channel's input in turn. A detailed discussion of the calibration system and its performance is given in [7].

The VA chip's control shift registers and bussed differential analog output allow several of the chips to be concatenated on one hybrid. This renders the connection requirements between hybrid and front-end controller uniform across the system, that is, makes the connections independent of the number of chips per detector module.

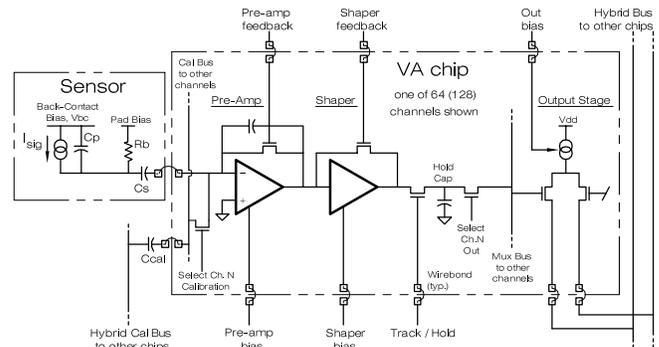


Fig. 3. Partial, functional block schematic of the VA front-end chip.

2) Hybrids

The hybrids use thick-film circuits on alumina substrates that provide good thermal conduction of the heat generated by the VA chips (about 1.3 mW/channel) to the water-cooled aluminum mounting frames. The circuits are composed of six layers: three signal layers on the top side, and on the bottom a layer each for ground and the two power rails (V_{dd} : +2 V, V_{ss} : -2 V). Of the three signal layers, two accommodate the 200 μ m pad pitch at the control side of the VA chip, and the third carries a bus which connects all chips to the I/O connector, a 30-pin header, at one end of the substrate. The densest substrate is 148 mm in length, carries twelve 128-channel chips, and has a total current draw of 0.9A on -2 V and 0.15A on +2V. Since the VA chip uses power rails of only ± 2 V, we used gold thick-film conductors to minimize the load-induced voltage drops along the length of the substrate. Top-side components include the VA chips and

their associated biasing resistors, bypass capacitors, a calibration signal attenuator, the calibration capacitors, and a temperature sensor. Bottom-side components are restricted to the 10 k Ω limiting resistors and 4.7 nF/ 200 V bypass capacitors that serve the back-contact electrode of each silicon sensor.

B. Front-End Controllers

The detector modules are powered, controlled and read out over flex cable by front-end controller (FEC) modules located 2 m from the silicon array. Because of their proximity to the detector, the FECs – and the crates which house them – are custom-designed to meet tight spatial constraints. The FEC is a 6U-high, 25 mm-wide, 220 mm-deep module composed of a signal board and a daughter power board with power regulators. There is no crate back-plane: the control signals and data are cabled directly to the module's respective data multiplexer unit in the Data Concentrator. Low-voltage, DC power is distributed on a busbar system at the rear of the crate and is jumpered to the FEC's power board.

1) FEC Signal Board

A block schematic of the signal board is shown in Fig. 4. The signal board has four ports; each port controls and reads out a detector module. In addition to providing the control signals for the VA chips, each port uses a serially-loaded 12-bit, octal DAC to provide programmable bias for the sensor's back-contact and a set of biases for the VA chips. Each port uses a 12-bit, scanning ADC to monitor these biases and the substrate temperature; the digitized values are appended to the event data at readout time. The port also contains a calibration module [7]; beyond its important role of calibrating the analog front-end, the calibration system also tests the full functionality of the front-end system beginning at the VA chip inputs.

To reduce deadtime, the detector module's readout chain is divided into two strings to be read out simultaneously. Each string sources a differential analog signal and a digital signal, "Shift out", which flags that the last channel of the string has been read. The string circuit in each port of the signal board contains a differential receiver, a differential pipelined 12-bit ADC, and a 2k-word x 18-bit FIFO which can store two events worth of data from up to 1,000 channels; the maximum number of channels/string in our system is 768. The string circuit also contains a built-in pattern generator for testing the data chain beginning at the FIFO input.

The FEC uses a field programmable gate array (FPGA) to coordinate the activities of the module in each of four modes: Set-up; Test; Calibration and Run. At power-on, the FPGA's internal logic is configured from a PROM. The configured FPGA then reads a second PROM containing information specific to each port including safe, initial bias levels for the sensor and VA chips, and the number of channels per string. In the Run mode, the FPGA idles with the VA chips in tracking mode; upon receiving a version of the Level 1 trigger delayed by 1.1 μ s, the FEC sends "Hold" to the VA chips

causing them to capture the peak of the channel signals. At the Level 2 trigger, the FEC begins reading out the strings into their respective FIFOs. When this process is complete, the controller unloads the FIFOs in sequence and appends a trailer block with temperature and bias values for each port. A G-Link interface in the FEC transmits this event data at 25 MB/s over a 10 m, twinaxial cable to a data multiplexer unit in the Data Concentrator. If a Level 2 trigger is not received within 10 μ s of the Level 1 trigger, the FEC puts the VA chips back in tracking mode.

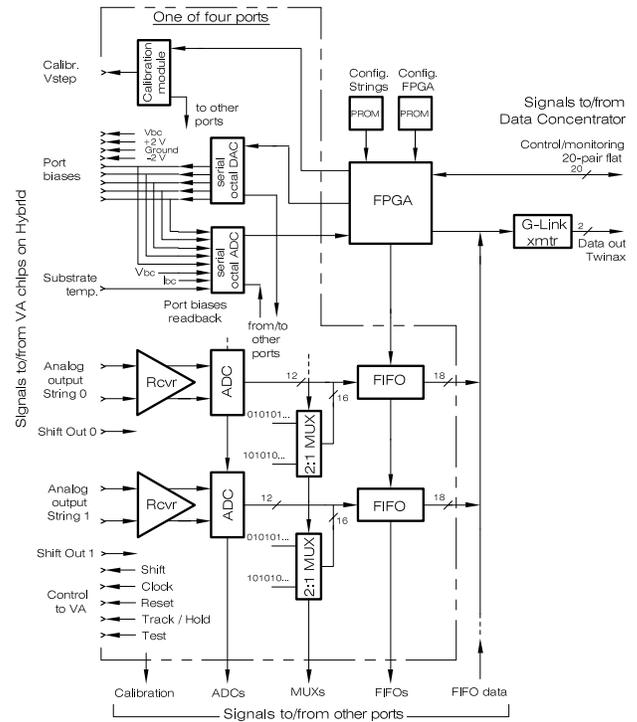


Fig. 4. Block schematic of Front-End Controller's signal board.

2) FEC Power Board

Because of the rather fragile nature of the silicon system, we chose to partition its DC power distribution system at the port level: each port has its own ± 2 V regulators for the VA chips (and the drivers and bias circuits which control them), a programmable 0 to +200V regulator for the sensor back-contact bias (V_{bc}), and ± 5 V regulators for the port's analog front-end. A single, +5V regulator provides power for the digital logic and serves the whole board. Since the VA chip has no ESD protection at its detector signal inputs, the V_{bc} regulator is designed to limit the rate of change of its output voltage; this in turn limits to a safe level the back-contact-to-pad capacitive charging/discharging currents at the VA chip inputs.

To further protect the VA chips, we use low dropout regulators fed from ± 3.3 V supplies; the worst-case voltage applied to the VA chips due to regulator failures is 6.6V which is still within the voltage rating of the process (1.2 μ m, N-well CMOS) used for fabricating the chips. The 5V regulators are fed from 6V, and the four DC inputs to the

power board, $\pm 3.3\text{V}$ and $\pm 6\text{V}$, are supplied by a power unit which handles up to 8 FECs -- potentially as many as 64,000 channels. The power unit is located about 2 m from the FEC crate; it is controlled and monitored via CANbus, and it also provides monitoring for the fan cooling units attached to the crate.

3) Latch-up Protection

With energetic beams of heavy ions circulating in the collider, the possibility exists for sending unusually large amounts of radiation through the sensors and front-end chips of the silicon detector modules: if part or all of the beam clips the wall of the beam pipe, the fragments from this "fixed target" collision are sent in a very forward direction in close proximity to the beam pipe in the intersection region. Because the plane of the sensors and chips of the detector modules near the beam pipe are aligned with the axis of the pipe, a rogue particle can travel several millimeters in a given sensor or chip.

If a charged fragment from the collision passes through a front-end chip, the charge it deposits in the bulk of the chip causes the parasitic transistors (inherent in the CMOS structure) to suddenly turn on, latch up, and conduct abnormally large currents which disable the chip [8]. Normal operation can only be recovered by first turning off the power to the hybrid and then later resetting the power.

Fig. 5 shows a block schematic of the latch-up protection circuit integrated with each port of the power board. A dual comparator monitors the voltage drops across the inductors in the π -filters at the outputs of the $\pm 2\text{V}$ regulators. If either voltage drop exceeds a fixed threshold, the comparator circuit disables both regulators and activates the crow-bar circuits which rapidly discharge their respective output lines. This action is taken within a few tens of microseconds of the radiation-induced event. The power is re-applied a few seconds later by sending a global power reset signal from the counting room.

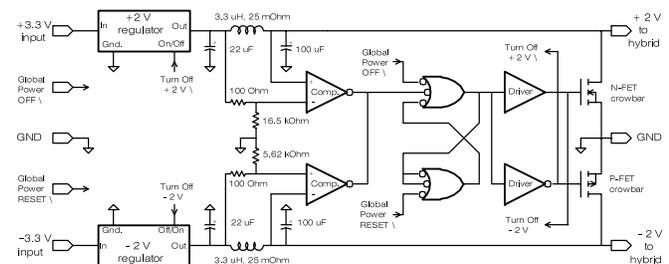


Fig. 5. Functional schematic of latch-up protection circuit on power board.

A rogue, charged fragment passing in the plane of a silicon sensor can produce an abnormally large current in the input of the front-end chip. Unfortunately it is not possible to quickly remove the sensor back-contact voltage to protect sensors and chip inputs in the same manner described above for latch-up protection. As mentioned earlier, a sudden change in back-contact bias only exacerbates the situation by injecting large currents into the unprotected input of the front-end chip.

C. Data Concentrator

Shown in Fig. 6, the data concentrator multiplexes and collates the data from the FECs into two bit streams for transmission to the DAQ system. Triggers from the counting room are sent to the data concentrator where they are opto-coupled and fanned out to the front-end system. All FECs are unloaded in parallel; each FEC transmits its data at 25MB/s via G-Link over twinaxial cable to one of two ports of a data multiplexing unit (DMU) in the data concentrator. The DMU interfaces control and monitoring signals to and from the FECs over 20-pair flat cables. The DMU's port data are stored, two hits with parity per word, in a 4k-word x 36-bit FIFO. Under the control of the Multiplexer Distributor Controller (MDC), the DMU FIFOs are multiplexed in turn to a common 32-bit bus with Front Panel Data Port (FPDP) protocol [9]. Data on this bus are received by a FPDP/Fiber Interface (FFI) module in the same crate; this full-duplex module serializes and transmits the data at 100 MB/s over an optical fiber to the counting room.

The MDC module provides the master function in a crate filled with DMU modules, and it prepares data (bias parameters for each of four ports in each FEC) for downloading to the front-end system. It fans out the L1, L2 triggers to the front-end controllers and handles their busy signals. It checks record length and parity for data on the FPDP bus and adds status information at the end of each record. The MDC's tasks are controlled by commands received over fiber from the DAQ system; this fiber occupies the second port of the full-duplex FFI module.

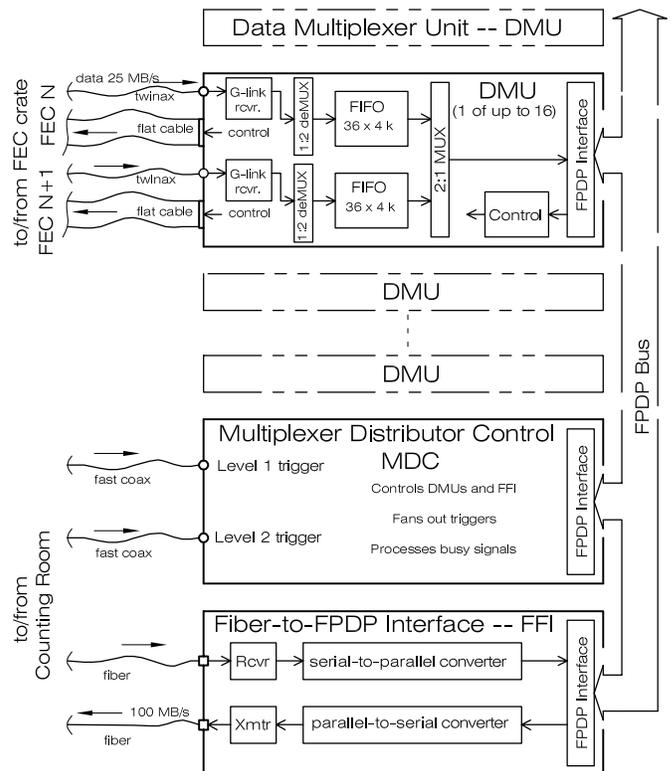


Fig. 6. Block diagram of modules in one crate of the Data Concentrator.

III. SYSTEM PERFORMANCE

A. Data Quality

A principal measure of the quality of the data from the front-end system is the channel signal-to-noise (S/N) ratio, defined here as the ratio of the MIP peak to the rms noise in the channel. Table I shows the S/N figure for various parts of the detector; the figures range from 15-to-1 in the Octagon portion of the multiplicity detector to 24-to-1 for the type 1 detector module used in the spectrometer. As expected, the figures correlate with the sensor channel's source capacitance which in turn is affected partly by the pad size. The S/N ratio everywhere in the detector exceeds the 12-to-1 minimum originally considered necessary for proper physics interpretation of the data.

TABLE I
SIGNAL-TO-NOISE FOR DIFFERENT PARTS OF THE DETECTOR

Subsystem Sensor	Signal-to-Noise	Sensor Pad Area, mm ²
Multiplicity -- octagon	15	23.6 (2.71 x 8.71)
Multiplicity -- rings	16	20 to 105 (pie-shaped)
Vertex -- inner	21	5.7 (0.473 x 12.0)
Vertex -- outer	21	11.4 (0.473 x 24.1)
Spectrometer -- Type 1	24	1.0 (1.00 x 1.00)
Spectrometer -- Type 2	21	2.6 (0.427 x 6.00)
Spectrometer -- Type 3	19	5.0 (0.667 x 7.50)
Spectrometer -- Type 4	19	10.0 (0.667 x 15.0)
Spectrometer -- Type 5	19	12.7 (0.667 x 19.0)

B. Reliability

Over three runs – the engineering run in 1999, the commissioning and first physics run in 2000, and the second physics run just drawing to a close in November 2001, the front-end system has performed flawlessly except for the failure of a cooling fan. But, despite its otherwise reliable performance over this period, the front-end system has recently sustained damage from errant beam in the machine; this is discussed in the following section.

C. Latch-up Protection Effectiveness

We retrofitted the power boards with latch-up protection in time for the year 2000 running period. During the commissioning period, we kept "sacrificial" silicon in place until stable machine operation was demonstrated. For the physics run which followed, we installed the complete multiplicity and vertex detectors and one spectrometer arm, in total about 324 sensors and 1,244 front-end chips. The beams – 2×10^{10} gold ions/beam at 65 GeV/nucleon – were well controlled. Under these conditions latch-up incidents, each involving 1 to 4 ports, occurred about 3 times/hour usually at the beginning and towards the end of each 4- to 6-hour beam store. With the latch-up protection installed, no front-end chips or wire bonds were lost; every incident was followed by complete recovery.

For the year 2001 physics run, we added the second spectrometer arm; the whole system now contains 496 sensors and 2,252 chips. In this run, RHIC achieved the design beam energy of 100 GeV/nucleon with 5×10^{10} gold ions/beam.

There has been good beam control for most of this run, during which latch-up incidents have occurred about 5 times/hour, again at the beginning and end of each 6- to 8-hour beam store. Unfortunately, in this present run, there have been 3 "errant beam" incidents in which the front-end has taken up to 0.5 rad/incident; in the most severe incident, latch-up occurred in 130 of the 152 active, installed ports. Although the protection system maintained the integrity of most of the front-end subjected to these beam incidents, we found 46 chips which suffered permanent damage; specifically, in a large number of channels in each of these chips, the calibration facility was damaged but fortunately the normal input from the sensor was left unaffected. We surmise that this failure is due to large current surges from the sensor: because of the absence of protection at the chip's input, these surges in turn lead to failure in the (near-) minimum-sized FET switch between the chip's internal calibration bus and the channel input (see Fig. 3).

IV. ACKNOWLEDGMENT

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