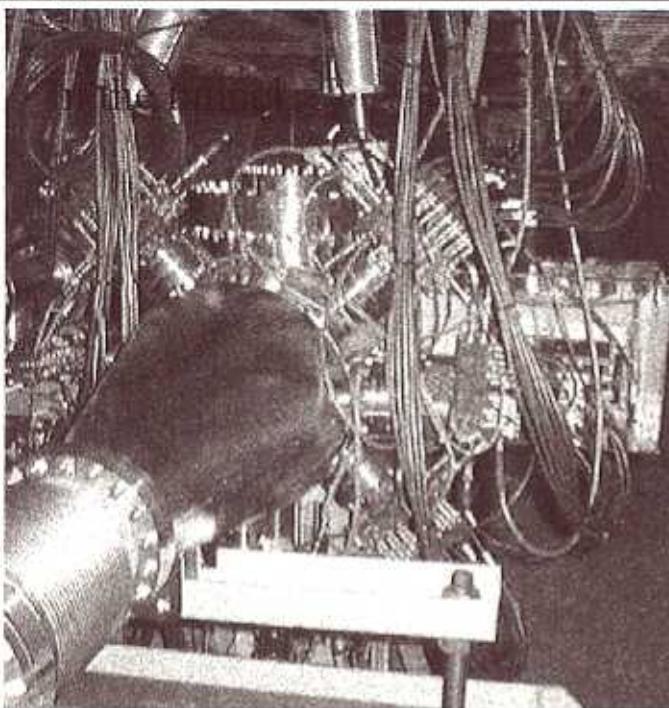


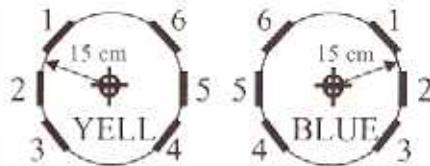
RHIC Polarimeter Updates

D. Svirida

RHIC Spin Collaboration Meeting
October 1, 2001
RIKEN BNL Research Center, Brookhaven National Laboratory



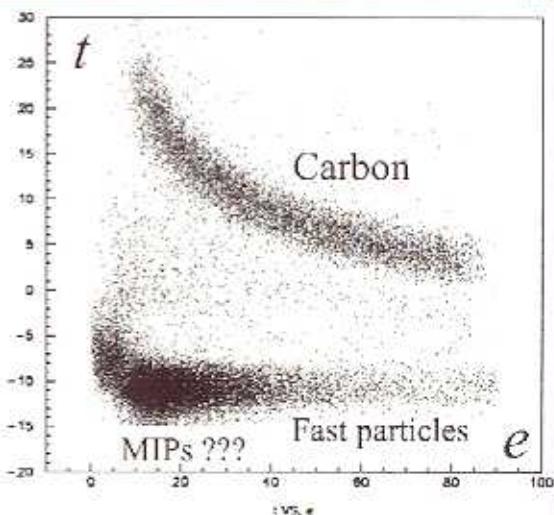
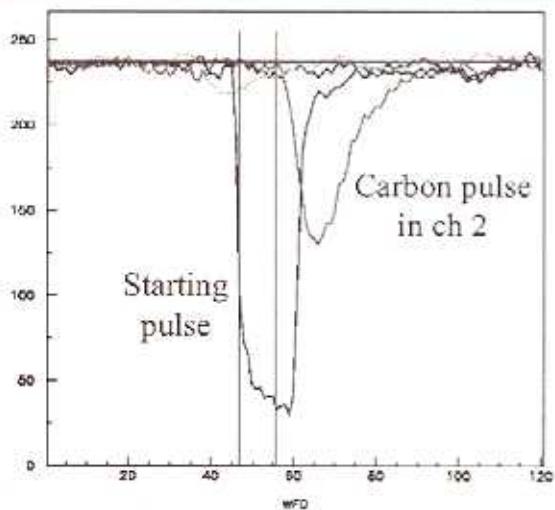
- WFD idea proved working during 2000 fall run (V1)
- 12 Si detectors mounted in the tunnel in both rings Apr 2001



- Cabling and preamps tested along with WFD V2 Apr 2001
- WFD configuration V5 developed and tested with pulser
- 6 WFD modules working, 2 assembled, 4 expect next week (new PCB version)
- Expect to have 48 channels this year

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Test of WFD idea



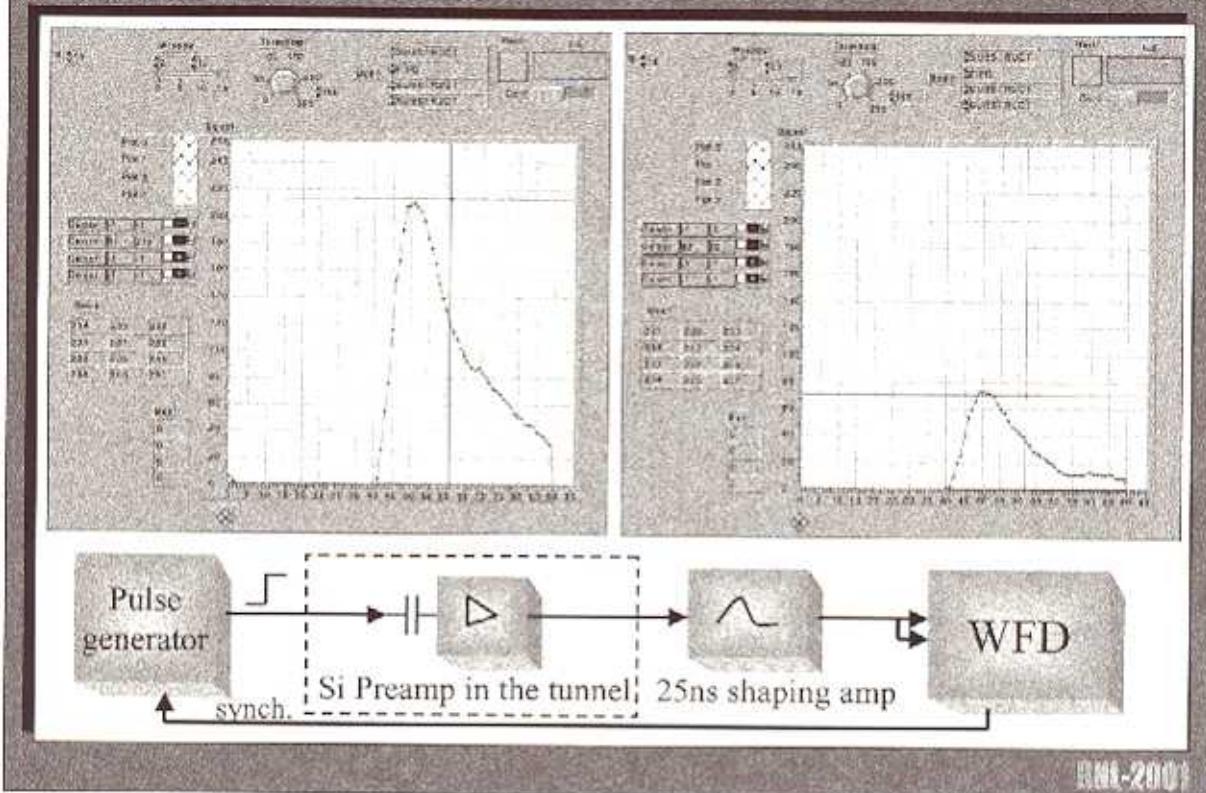
- 1 WFD module V1, 4 channels
- Common external trigger, 3 chans relative to reference pulse on ch. 4
- Waveforms read to PC

- Off-line event reconstruction

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Detector and WFD V2 test

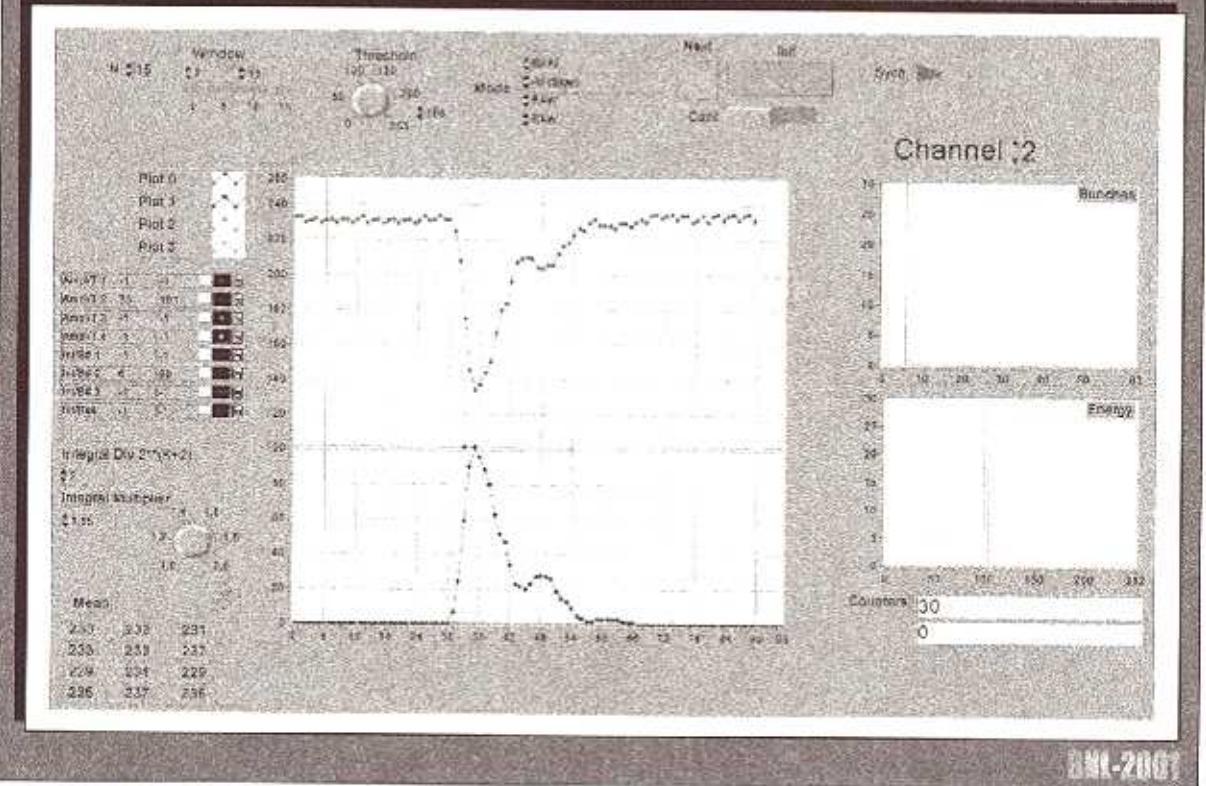
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WFD V5 test

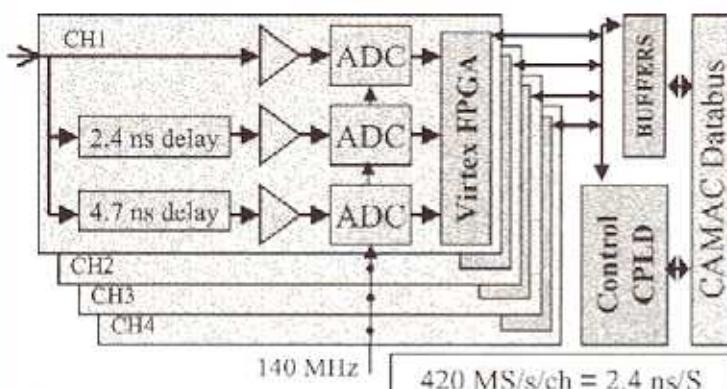
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WFD Block Diagram

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Mode	FIFO, ev	Bytes/ev	Max ev/s	Note
RAW	16	90	$3 \cdot 10^4$	Debug
WAVEFORM	16	90	$3 \cdot 10^4$	Debug
RESULT	256	4	$7 \cdot 10^5$	Test/Run
BOTH	1	92	$3 \cdot 10^4$	Test
SCALERS	-	0	:	Run

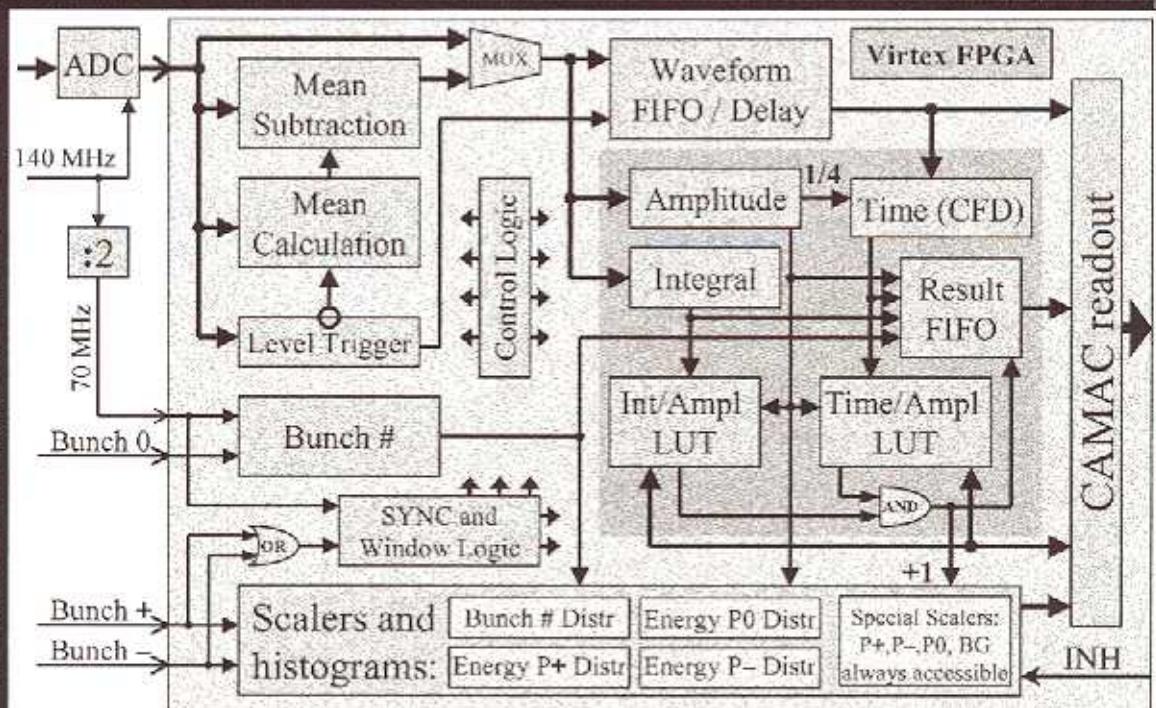
Expecting rate: 10^7

- ✓ 8-bit amplitude and integral
- ✓ 2.4 ns time resolution
- ✓ Bunch # information
- ✓ Windowed sensitivity
- ✓ Noise reduction
- ✓ Time/amplitude LUT
- ✓ Integral/ampl LUT
- ✓ LUTs programmable through CAMAC
- ✓ 5 always accessible scalers (P+, P-, P0, 2*BG)
- ✓ 60 ch bunch distribution
- ✓ 3*64 ch amplitude distributions for P+, P-, P0
- ✓ Crate INH stops scaling
- ✓ Zero deadtime
- ✓ Flexible FPGA configuration

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FPGA Block Diagram

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Commissioning

- With real carbon signals compare parameters calculated ON-BOARD with those calculated by various OFF-LINE methods using the waveforms ("BOTH" mode)
- Energy calibration

Run

- EITHER: Get some events with LUTs fully open to determine carbon cuts ("RESULT"), then program LUTs
- OR: Get some events with wide LUTs to get the luminosity information = "figure of quality" ("SCALERS")
- Get main statistics ON-BOARD ("SCALERS")
- Read out scalers/histograms
- Calculate average and bunch by bunch polarization:

$$\min S^2 = \min \sum_{i=1,M}^{j=1,L} \left(N_{ij} - \sigma_0 \cdot I_i \cdot C_j \cdot (1 + A_{pC} \cdot P_i \cdot \sin(\alpha_j - \varphi)) \right)^2, \text{ where:}$$

2·M+N
parameters
M·N
measurements

N_{ij} – count of j-th strip in i-th bunch;
 I_i, P_i – i-th bunch intensity and polarization;
 C_j, α_j – j-th strip acceptance and angle;
 φ – polarization vector angle.

To Do List

- Transfer the FPGA design to the new version of the PC board and test new modules
- Finish with *5 frequency multiplier and V124 signal fanouts
- Develop and debug the software for commissioning and running

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