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The implementation of Global Feature EXtractor (gFEX) - the ATLAS Calorimeter Level 1 Trigger system for LHC Run-3 upgrade

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Abstract: As part of the ATLAS Phase-I Upgrade, the global Feature EXtractor (gFEX) is one of several hardware modules designed to help maintain the ATLAS Level-1 trigger acceptance rate with the increasing Large Hadron Collider (LHC) luminosity and the increasing Pile-Up conditions. The gFEX is used to identify patterns of energy associated with the hadronic decays of high momentum Higgs, W & Z bosons, top quarks, and exotic particles in real time at the 40 MHz LHC bunch crossing rate. The board is required to receive coarse-granularity ($\Delta\eta \times \Delta\varphi = 0.2 \times 0.2$ gTower) information from the entire ATLAS calorimeters on 276 optical fibers. A prototype v1 with one Xilinx ZYNQ FPGA, and one Vertex-7 FPGA for technology validation has been designed and tested in 2015. With the lessons learned from the prototype v1, a prototype v2 with three Vertex UltraScale FPGAs and one ZYNQ FPGA has been implemented to verify full functionalities of gFEX in 2016. Based on the prototype v2 design, a prototype v3, the final gFEX prototype, is implemented, which is an ATCA module consisting of three Vertex UltraScale+ FPGAs, one ZYNQ UltraScale+ SoC, and 35 MiniPODs. This board receives up to 300 fiber optical links from calorimeters and transmits trigger data on 96 links to the to the ATLAS Level-1 Topological trigger (L1Topo [1]) at the speed up to 12.8 Gb/s. There are also 24 electrical links on board for communication between two FPGAs with the speed up to 25.6 Gb/s. The performance of three prototype boards have been tested and evaluated. For the prototype v3 board, the high-speed optical links are stable at 12.8 Gb/s with Bit Error Ratio (BER) $< 1 \times 10^{-15}$. The low-latency parallel GPIO (General Purpose I/O) buses between FPGAs are stable at 1.12 Gb/s. The peripheral components of ZYNQ UltraScale+ SoC, such as 16 GB DDR4 DIMM, UART, SPI flashes, and Ethernet, have also been verified. The test results of the prototype v3 board validate the gFEX technologies, architecture and full functionalities. Now the final production board is being produced.

Keywords: Trigger concepts and systems (hardware and software); Digital electronic circuits; Optical detector readout concepts

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1 Introduction

To increase the luminosity in the next ten years, a series of upgrades will be carried out on the LHC at CERN. The ATLAS [2] experiment will follow the same upgrade schedules. During the so-called Phase-I upgrade in 2019–2020, a global feature EXtractor (gFEX) will be installed within the Level-1 ATLAS calorimeter trigger (called L1Calo). It is one of serval new components designed to maintain the trigger acceptance with increasing instantaneous luminosity conditions. The gFEX is intended to identify large-radius jets [3], such as Lorentz-boosted objects, by means of wide-area jet algorithms refined by subjet information. The high-pT bosons and fermions are a key component of the ATLAS physics program. As shown in the figure 1, the current ATLAS Level-1 trigger system was designed for narrow jets with limited acceptance for large objects. The acceptance for large-radius jets will be greatly enhanced by the inclusion of the gFEX in the L1Calo system, shown as figure 2. The architecture of the gFEX permits event-by-event local pileup suppression for these large-R objects using baseline subtraction techniques [4].

The L1Calo system receives and processes signals from electromagnetic and hadronic calorimeters. As shown in the figure 3, the L1Calo system before Phase-I upgrade has three major subsystems (marked with green color): the Cluster Processor Subsystem (CP) consisted of Cluster Processor Modules (CPMs) [5] and Common Merger Extended Modules (CMXs) [6]; the Jet/Energy Processor Subsystem (JEP) comprising Jet/Energy Modules (JEMs) [7] and CMXs; and the Pre-Processor Subsystem with Pre-Processor Modules (PPM). There will be three new feature identification systems installed during the Phase-I upgrade: the Electron Feature Extractor (eFEX) [8], the Jet Feature Extractor (jFEX) [9], and the gFEX. The eFEX and jFEX will provide similar functionalities as the CPMs and JEMs respectively but benefiting from much finer granularity. Each system consists of multiple modules that operate on limited regions of the calorimeter. In contrast, the gFEX has the entire calorimeter data available in a single module and thus enables the use of full-scan algorithms. With these benefits, it will maximum the flexibility of the trigger, avoid the data duplication, and compute of global quantities without boundaries.

In LHC Run 3, the electromagnetic calorimeter will provide L1Calo with both analog signals (for the CP and JEP) and digitized data (for the FEXes). The hadronic calorimeter will continue to send analog signals which are digitized on the Pre-Processor and then transmitted to the FEXes through an optical patch-panel. The older analog subsystems will be decommissioned once the performance of the FEXes is validated.

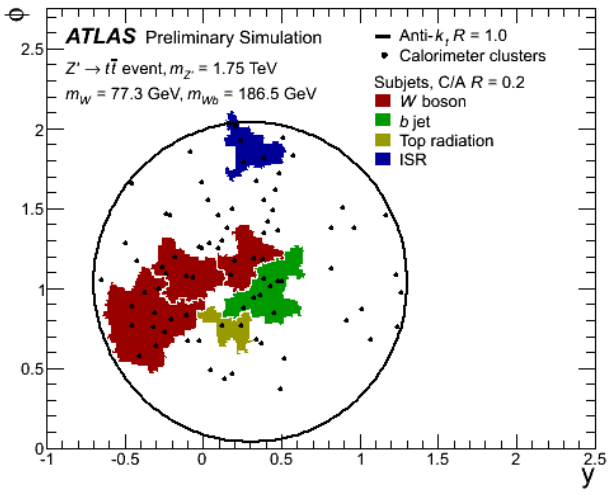

Figure 1. Effect of jet acceptance with gFEX, compared with current L1 algorithm [10]. The red circle area ($R < 1$) is the L1 narrow jet, and the black circle is the large-R jets with gFEX. Reproduced from [10]. © 2018 CERN for the benefit of the ATLAS Collaboration.

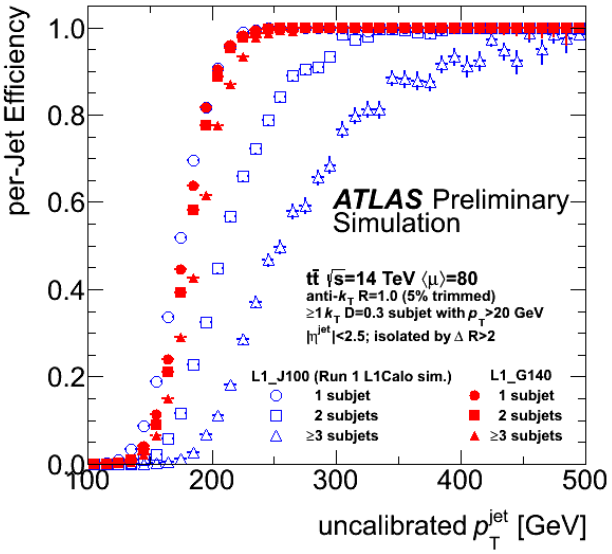

Figure 2. Acceptance gain for boosted top after adding gFEX [11]. The blue curves show the acceptance without gFEX. The 140 GeV gFEX trigger threshold is chosen to match the L1 J100 single subjet turn-on curve. After adding gFEX, the acceptance of two and more sub-jets is recovered and the resolution is nearly the same as that of one sub-jet. Reproduced from [11]. © 2018 CERN for the benefit of the ATLAS Collaboration.

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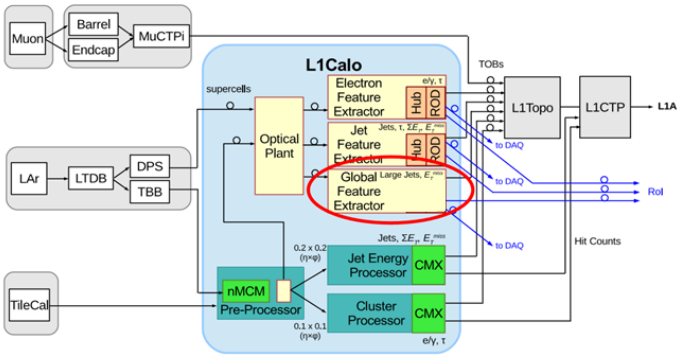

Figure 3. The L1Calo system block diagram after completion of the Phase-I upgrade; the eFEX, jFEX and gFEX are new hardware modules designed in the Phase-I upgrade.

2 Prototype hardware design of gFEX

The gFEX is a single customized Advanced Telecommunications Computing Architecture (ATCA) module based on the PICMG® 3.0 Revision 3.0 specification [12]. The board will receive coarse-granularity (0.2×0.2 gTower) information from the entire ATLAS calorimeters on 276 optical fibers. So several large Field-Programmable Gate Arrays (FPGAs) for data processing, a combined FPGA & CPU System-on-Chip (SoC) running embedded system for control and monitoring, and several Avago MiniPODs for data inputs and outputs are deployed in this board. A special feature of the gFEX is that it receives data from the entire calorimeter enabling the identification of large-radius jets and the calculation of whole-event observables. Each processor FPGA has 2π azimuthal (φ) coverage for a slice in pseudorapidity (η) and executes all feature identification algorithms. The processor FPGAs communicate with each other via low-latency GPIO links while input and output to the MiniPODs are via Multi-Gigabit Transceiver (MGTs). There are also on board electrical MGT links between processor FPGAs and SoC FPGA for data transmission and control. The gFEX module will be placed in a sparsely populated ATCA shelf so that it can occupy two slots if needed: one for the board and one for cooling (e.g., large heat sinks) and fiber routing, etc.

2.1 gFEX prototype v1

A first prototype was designed to verify all the functionalities of the chosen technologies, such as signal integrity, Megtron-6 material, PCB stack-up, back drill technology, power distribution and sequence, MGT link speed, high speed parallel GPIOs and ZYNQ interfaces.

To save cost and speed up the hardware development, only one SoC FPGA — ZYNQ and one processor FPGA are included on the prototype v1. There are also several MiniPODs, MicroPODs, power modules and high speed parallel GPIOs implemented for the technology validation.

This board was successfully tested and verified in the lab in 2015 [13]. All the 80 channels GTH transceivers of the Vertex-7 FPGA are running at 12.8 Gb/s with Bit Error Rate (BER) $< 1 \times 10^{-15}$. The 50-bit wide parallel GPIO data bus was tested at 960 Mb/s in 480 MHz DDR mode with very good margin ($> 65\%$). It was also used in the link-speed test between Liquid Argon Calorimeter (LAr) and L1Calo in January 2016 at CERN. The LAr-L1Calo link-speed test was aimed to choose the link speed between two systems in the Phase-I upgrade. The test results show that the links

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between the Liquid Argon Digital Processing Blade (LDPB) and gFEX are stable at 6.4 Gb/s, 9.6 Gb/s and 11.2 Gb/s without any error observed, except two links that have known issues at the LDPB TX side [14]. The link speed test between LDPB and eFEX was carried out in April 2016. Based on the successful LAr-L1Calo link speed test on both gFEX and eFEX, it was decided to use 11.2 Gb/s as the baseline link speed, with options of 9.6 Gb/s and 12.8 Gb/s.

2.2 gFEX prototype v2

The gFEX prototype v2 is a full functional prototype. As shown in figure 4, there are a total of four FPGAs implemented on the board. Three Virtex UltraScale FPGAs are used as processor FPGAs, and one ZYNQ FPGA is for TTC clock recovery and distribution as well as control and monitoring.

Three processor FPGAs process the data from the electromagnetic and hadronic calorimeter via fiber optical links and on board MiniPOD receivers. After processing, the real-time trigger data of each processor FPGA are sent to the L1Topo module through one 12-channel MiniPOD transmitter respectively. The processor FPGA-1 and FPGA-2 have identical functionalities; both receive 96 optical inputs. All the input data will be processed by the feature identification algorithms implemented in the FPGA, and the trigger information will also be sent to L1Topo at each processor FPGA directly. The processor FPGA-3 will only receive 84 optical links from calorimeter, which meets the design requirement of total 276 input optical links.

The FPGA-3 also functions as an aggregator, which receives data from the other two processor FPGAs, then sends all the trigger data to the FELIX (Front End LInk eXchange) [15]. The ZYNQ FPGA recovers the 40MHz TTC (Timing, Trigger and Control) clock through the FELIX link. The recovered TTC clock is the source clock of the high-performance clock generator (SI5345) with jitter-cleaning capability, which generates the reference clocks with required frequencies for the MGT links. The jitter cleaning function of SI5345 is crucial to guarantee the links running stably above 10 Gb/s.

The gFEX prototype v2 is a 26-layer board with 28 MiniPODs populated. It is designed and manufactured with low-loss material Megtron-6 as well. The back-drilling technology is adopted in the fabrication to minimize the influence of stubs on the high-speed link performance. Compared to the blind via technology, the back drilling is more cost effective and easier to produce.

The fully assembled board was tested in mid-2016 at BNL. The basic functionalities of all four FPGAs have been verified successfully, including the configuration, ZYNQ interfaces (SD card, DDR3, GbE and I2C slaves), clock generator configuration and distribution, and board health monitoring (voltage, current, and temperature). With 28 MiniPODs fully loaded on board, and all MGT links running at 12.8 Gb/s, the total power consumption is about 300W. Taking into account of the 90% efficiency of the DC/DC converter and power input module, the total power consumption of this board is about 333 W, which is less than the 400 W power limit of single slot in the ATCA chassis.

All the MGT links, including (optical links via MiniPODs and on board electrical traces), are running at 12.8 Gb/s stably without bit error. The on-board GTY electrical links have good eye diagram and are stable at 25.6 Gb/s without bit error [16]. The nine groups of 20-bit parallel GPIO data buses between two FPGAs have been tested running stably at 1.12 Gb/s in 560 MHz DDR mode with good margin (> 50%).

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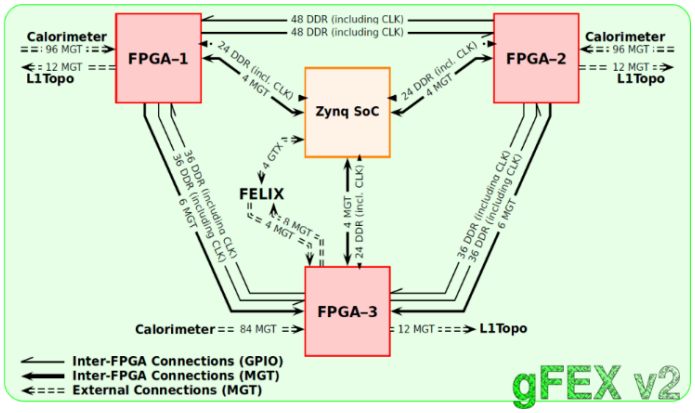

Figure 4. Architecture of gFEX prototype v2 board; the processor FPGA-1 and FPGA-2 both receive 96 optical inputs; the FPGA-3 receive 84 optical links from calorimeter; the ZYNQ is used to control and monitoring the board with embedded system on it.

After the functionalities and performance test, this board is used in the integration test with FELIX to prepare for the final design review of the gFEX. The integration test stand is shown in figure 5. The gFEX prototype v2 is on the test bench at the near end, while the FELIX is installed in the PC at the far end. The FELIX provides the TTC clock information to the gFEX via GBT mode link and receives the data from gFEX via FULL mode links. The ZYNQ on the gFEX recovers the TTC clock from GBT link, then sends to the jitter cleaning clock generator SI5345 to improve the clock quality and generates the reference clock for the FULL mode links to the FELIX. With this configuration, both the GBT mode link at 4.8 Gb/s and FULL mode link at 9.6 Gb/s are established between FELIX and gFEX successfully.

The prototype v2 board is also used as firmware development platform for the gFEX, so far it has been running as firmware test stand for about one year without power cycle.

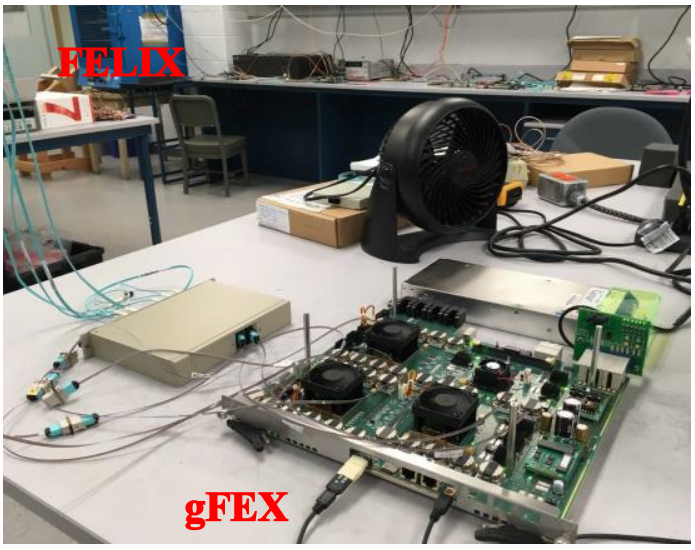

Figure 5. Test stand of the gFEX and FELIX integration test. The gFEX prototype v2 is on the test bench at the near end, while the FELIX is installed in the PC at the far end.

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2.3 gFEX prototype v3

Based on the experience of the previous gFEX prototype boards development, a prototype v3 has been designed and tested in 2017. The prototype v3 serves as the pre-production board, and it is the final prototype before the production and installation on detector. The architecture of the gFEX prototype v3 is shown in figure 6. Compared to the prototype v2, this board uses same Vertex UltraScale+ for the three processor FPGAs, and replaces the ZYNQ with a ZYNQ UltraScale+ FPGA. To take advantage of resources of ZYNQ UltraScale+, all the interfaces between processor FPGA-3 are moved to the ZYNQ UltraScale+. With the Vertex UltraScale+ FPGAs, all the transceivers are GTYs and there are much more 25.6 Gb/s links on-board. All three processor FPGAs send the trigger data to ZYNQ UltraScale+ via eight 25.6 Gb/s GTY links and twelve 12.8 Gb/s GTH links. Then the ZYNQ UltraScale+ transfers all these trigger data to the FELIX through 12 channels of MGT links. After removing the FELIX connection, the processor FPGA-3 can receive 100 optical links from calorimeter and transmit real-time data via 24 optical links to L1Topo as the other two processor FPGAs. With increased optical inputs and outputs, the total number of MiniPOD is increased from 28 to 35. These improvements will provide better compatibility for gFEX to be used in the High-Luminosity LHC (HL-LHC) which needs up to 24 output fiber links [17].

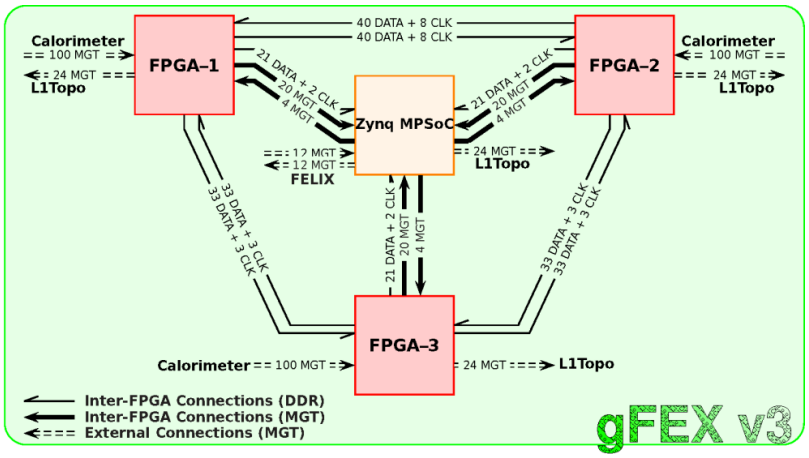

Figure 6. Architecture of gFEX prototype v3; all three processor FPGA-1 receive 100 optical links form calorimeter and transmit the real-data to L1Topo through 24 optical links; all the interface of FPGA-3 in the prototype v2 are moved to the ZYNQ UltraScale+ to simplify the hardware and firmware design.

With more MiniPODs and ZYNQ UltraScale+ FPGA, the board stack up has to be increased from 26 to 30 layers. The same PCB material and back drilling technology are used as previous prototypes. The estimate of power consumption is increased about 50 W, so a 500 W power input module and DC/DC convertor are used to replace 400W modules on the prototype v2 board.

The fully assembled gFEX prototype v3 shown in figure 7 was received in September 2017. The basic functionalities and performance test has been carried out at BNL. All four FPGAs can be configured via JTAG and QSPI flash successfully. For the ZYNQ UltraScale+ PS interfaces, GbE, I2C slaves, UART, 16GB DDR4 DIMM and voltage, current and temperature monitoring are verified successfully. However, the SD card is not connected to the dedicated ports which can be

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used as boot interface, this issue will be fixed in the production version. As shown in the figure 8, this board works well in the ATCA chassis with the IPMC module installed. The IPMC module on gFEX is used to control the power on and power off, which has been verified at shelf manage terminal successfully. The board can be powered cycle remotely as expected.

The IBERT test is carried out on this board to verify all the MGT links. All links are stable at 12.8 Gb/s without error detected. For 24 on board electrical GTY links from three processor FPGAs to ZYNQ UltraScale+, all of them are stable at 25.6 Gb/s. The typical eye diagram of optical link at 12.8 Gb/s is shown in figure 9. The typical eye diagrams for on board 8-inch electrical links are shown in figure 10 and figure 11. The figure 10 is for the 12.8 Gb/s and the figure 11 is for the 25.6 Gb/s links.

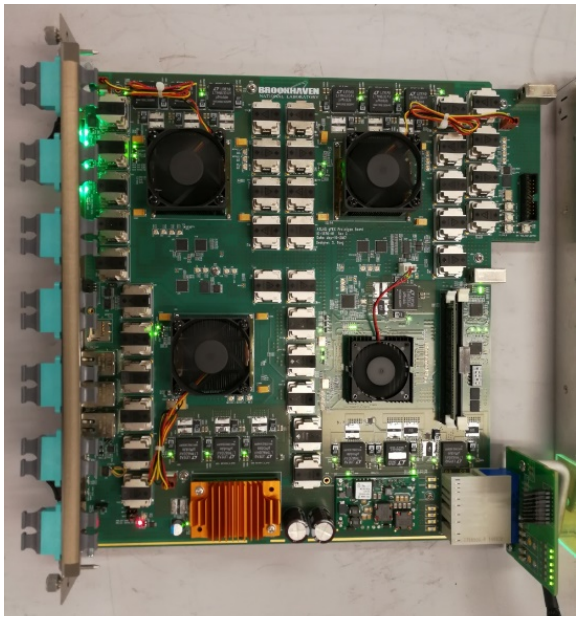

Figure 7. Fully assembled gFEX prototype v3 board. There are four large FPGAs and 35 MiniPODs, and it is a 2-slot module.

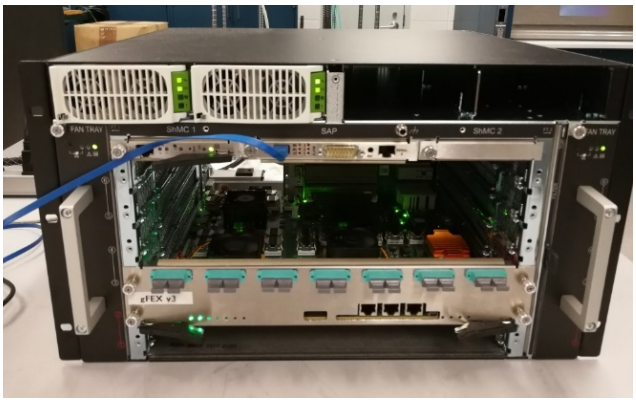

Figure 8. Fully assembled gFEX prototype v3 board in the ATCA chassis with IPMC card; the board can be remote power cycling through the ATCA shelf manager.

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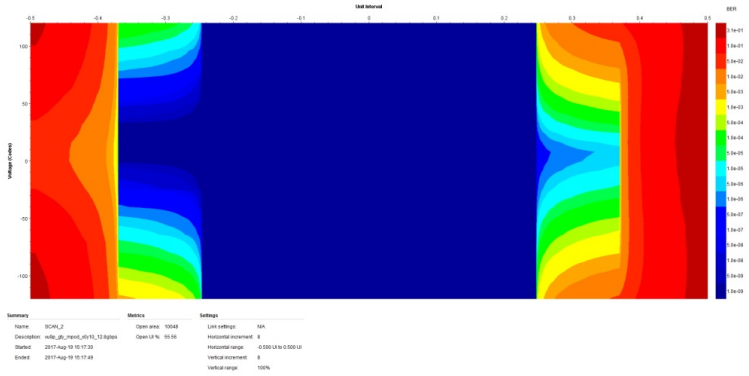

Figure 9. Eye diagram of the optical link from processor UltraScale+ FPGA GTY transmitter to GTY receiver going through MiniPODs and fibers. Open area is 10,048 at 12.8 Gb/s.

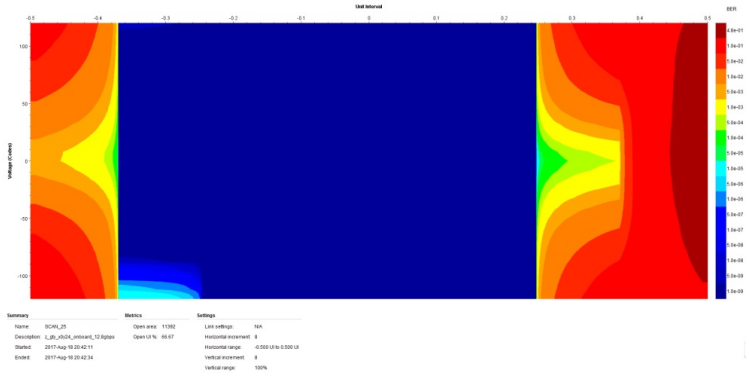

Figure 10. Eye diagram of the electrical link from processor UltraScale+ FPGA GTY transmitter to ZYNQ UltraScale+ GTY receiver. Open area is 13,922 at 12.8 Gb/s.

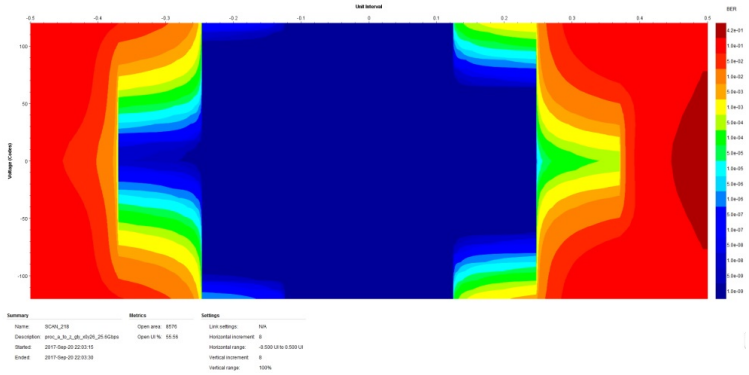

Figure 11. Eye diagram of the on-board electrical link from processor UltraScale+ FPGA GTY transmitter to ZYNQ UltraScale+ GTY receiver. Open area is 8,576 at 25.6 Gb/s.

The parallel GPIO buses between two FPGAs are also verified successfully at 1.12 Gb/s with good margin (> 50%). To estimate the power consumption of this board, all the transceivers of four FPGAs are turned on and running at 12.8 Gb/s with IBERT firmware. All 35 MiniPODs are in working status. The total power consumption is about 340W. Considering of the 95% efficiency of

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power input module and DC/DC into account, the total power consumption of this board is about 360 W, which is still within the 400W single slot limitation of ATCA chassis. Moreover, the gFEX board will sit in one chassis alone, the one slot power limit can be configured up to 600 W. In this test case, the temperature of the FPGAs is about 77°C and the hottest power module is about 85°C. Both are within the specified operating temperature range of the components.

3 gFEX production board

As mentioned above, there is a design issue of SD card interface on the prototype v3 board. A production board with design changes has been completed. It has been sent out for fabrication in the end of 2017.

4 Summary

The gFEX prototype v1 and v2 has been used to verify the challenging hardware technologies successfully, such as 12.8 Gb/s fiber optical links, 25.6 Gb/s on board electrical links, and 1.12 Gb/s on board parallel data buses. The gFEX prototype v1 has been used in the link speed test to determine the link speed between calorimeter and L1Calo systems. The gFEX prototype v2 board is used in the FELIX integration test and the firmware development. The fully assembled gFEX prototype v3 board has been tested, all functionalities and performance have been verified in the lab successfully. It will be used in the integration test at CERN in 2018. With successful development of prototypes, the production gFEX board design is moving forward for fabrication and test with good confidence. During the test of all the prototypes, the interface firmware and IBERT are used to verify the hardware performance. The algorithm firmware is under development, and the estimated latency for gFEX is around 270 ns which meets the requirement. The gFEX board is the FPGA based board, so it is flexible to be used as generic-processing engine in other parts of the ATLAS trigger chain.

References

[1] B. Bau et al., *ATLAS Level-1 Topological Processor Project Specifications*, v1.3, 11 September 2013, http://www.staff.uni-mainz.de/uschaefe/browsable/L1Calo/Topo/src/old/spx.pdf.

[2] ATLAS collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, 2008 *JINST* **3** S08003 [LHCC-I-020].

[3] ATLAS collaboration, *Search for new phenomena in final states with large jet multiplicities and missing transverse momentum using* $\sqrt{s}$ = 7 *TeV pp collisions with the ATLAS detector*, *JHEP* **11** (2011) 099 [arXiv:1110.2299].

[4] ATLAS collaboration, *Pile-up subtraction and suppression for jets in ATLAS*, ATLAS-CONF-2013-083 (2013).

[5] J. Bracinik et al., *ATLAS Level-1 Calorimeter Trigger Firmware Upgrade of Cluster Processor Module Project Specification*, v1.0.13, 01 August 2014, http://epweb2.ph.bham.ac.uk/user/bracinik/CPMPhase0/CPMPh0Spec.pdf.

[6] L1Calo CMX collaboration, *ATLAS Level-1 Calorimeter Trigger CMX Module Project Specification*, v1.0, 8 August 2011, http://www.pa.msu.edu/hep/atlas/l1calo/cmx/specification/1_preliminary_design_review/CMX_Project_Specification_v1.0_final.pdf.

2018 JINST 13 P07010

[7] U. Schäfer et al., *ATLAS Level-1 Calorimeter Trigger Jet/Energy Processor Module Project Specification*, v1.2d, 15 February 2008, http://hepwww.rl.ac.uk/Atlas-L1/Modules/JEM/JEMspec12d.pdf.

[8] W. Qian, *Design and test performance of the ATLAS Feature Extractor trigger boards for the Phase-1 Upgrade*, 2017 *JINST* **12** C01079.

[9] M. Weirich, B. Bauss, A. S. Brogna, V. BUESCHER, R. Degele, H. Herr et al., *Development of the jet feature EXtractor (jFEX) for the ATLAS level 1 calorimeter trigger upgrade at the LHC*, PoS(TWEPP-17)133.

[10] ATLAS collaboration, *Performance of shower deconstruction in ATLAS*, ATLAS-CONF-2014-003 (2014).

[11] ATLAS collaboration, *Global Feature Extraction (gFEX) Performance Plots*, ATL-COM-DAQ-2014-087, 21 August 2014, https://twiki.cern.ch/twiki/bin/view/AtlasPublic/JetTriggerPublicResults#Global_Feature_Extraction_gFEX_P.

[12] ATLAS collaboration, *Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment*, CERN-LHCC-2012-022 [LHCC-I-023];
AdvancedTCA ® Specification, http://www.picmg.org/openstandards/advancedtca.

[13] S. Tang, M. Begel, H. Chen, F. Lanni, H. Takai and W. Wu, *gFEX, the ATLAS calorimeter level-1 real time processor*, in proceedings of *Nuclear Science Symposium and Medical Imaging Conference*), San Diego, CA, 2015.

[14] W. Wu, M. Begel, H. Chen, K. Chen, F. Lanni, H. Takai et al., *The development of the global feature extractor for the LHC run-3 upgrade of the l1 calorimeter trigger system*, in proceedings of *Real Time Conference*, Padua, 2016.

[15] J. Anderson et al., *FELIX: a High-Throughput Network Approach for Interfacing to Front End Electronics for ATLAS Upgrades*, *J. Phys. Conf. Ser.* **664** (2015) 082050.

[16] H. Chen, M. Begel, K. Chen, F. Lanni, H. Takai, S. Tang et al., *The prototype design of gFEX — a component of the l1calo trigger for the ATLAS phase-i upgrade*, in proceedings of *Nuclear Science Symposium, Medical Imaging Conference and Room-Temperature Semiconductor Detector Workshop*, Strasbourg, 2016.

[17] ATLAS collaboration, *Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System*, CERN-LHCC-2017-020 [ATLAS-TDR-029].

2018 JINST 13 P07010