



Microelectronics Pilot Program

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"The research described herein is Fundamental Research as defined in EAR (15 CFR §734.8), or Part 810 (10 CFR §810.3), as applicable, and as described in the USD (AT&L) memoranda on Fundamental Research, dated May 24, 2010, and on Contracted Fundamental Research, dated June 26, 2008."

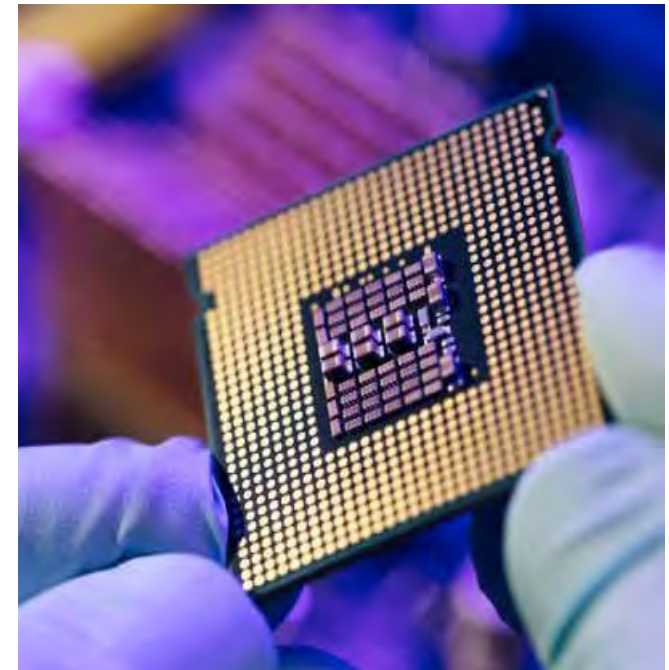
Microelectronics chips are ubiquitous

WHERE

Computers
Smart phones/tablets
Cars
Cameras
Refrigerators
Washing Machines
EVERYWHERE!

WHY ARE CHIPS USED?

Performance
Efficiency
Connectivity
Features



AMD RYZEN CHIP

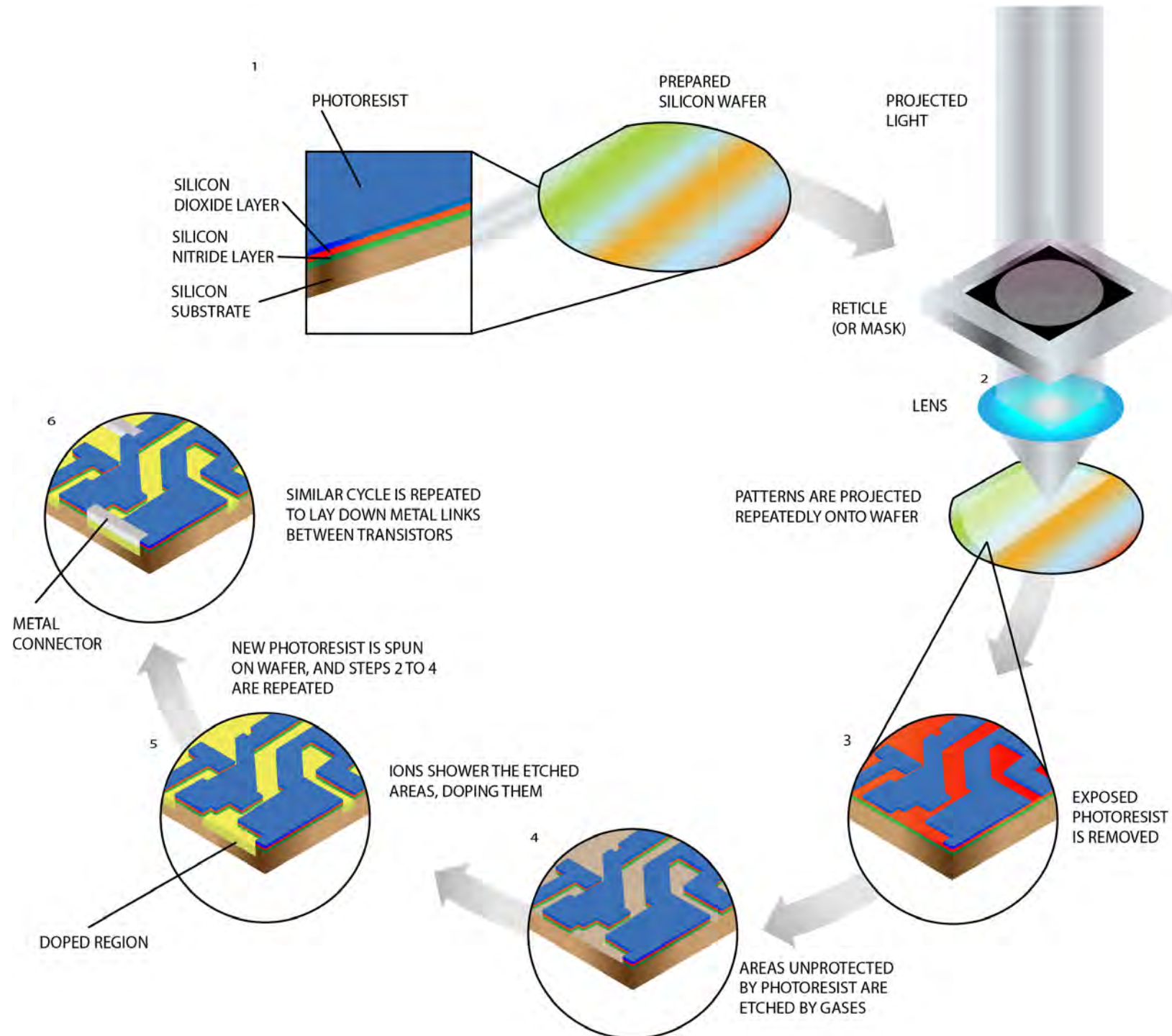
How are chips made?

Silicon Wafer

Lithography (to make small features)

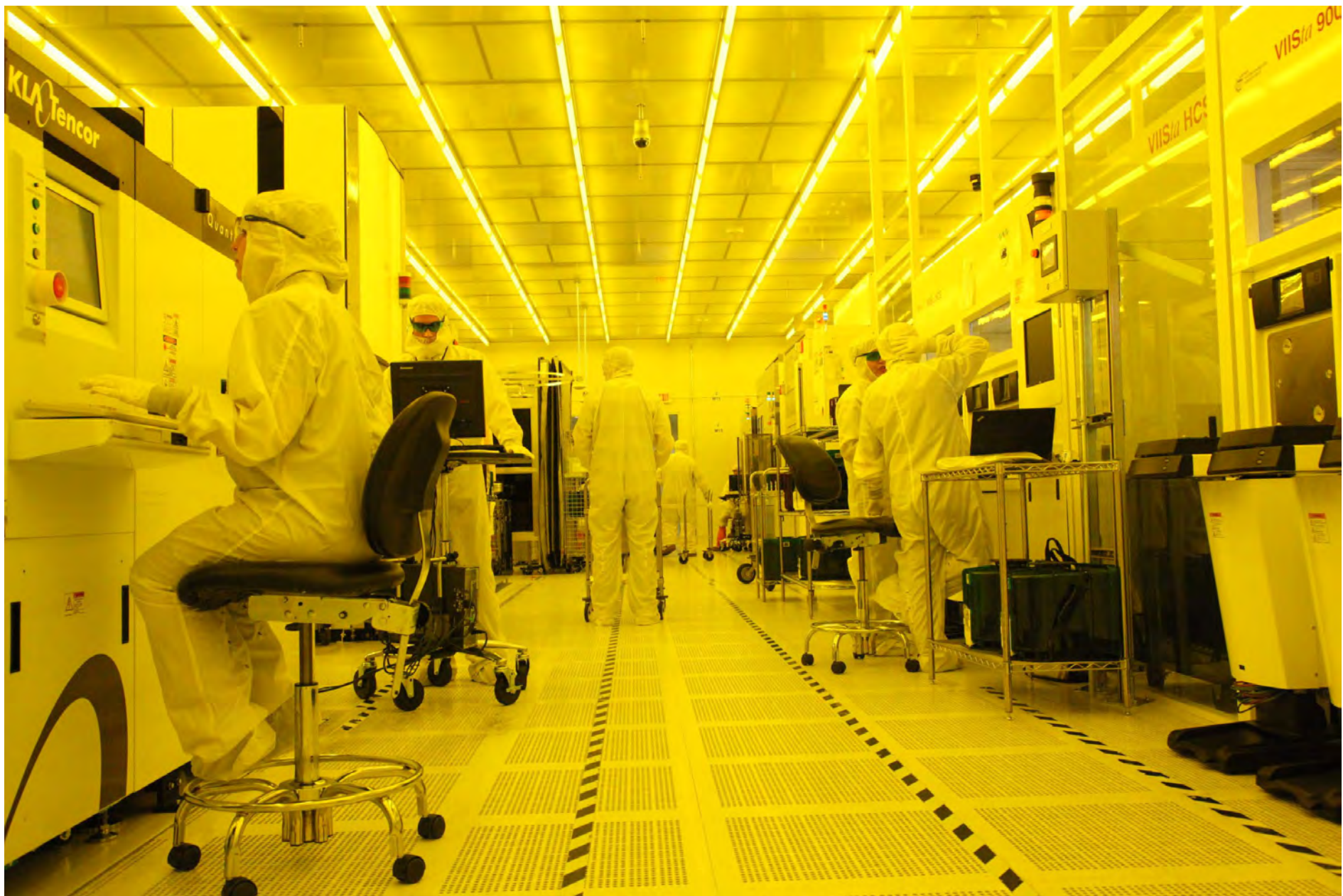
Materials deposition, etching...

Many layers!



NYCREATES Facility in Albany (>\$25B investment)



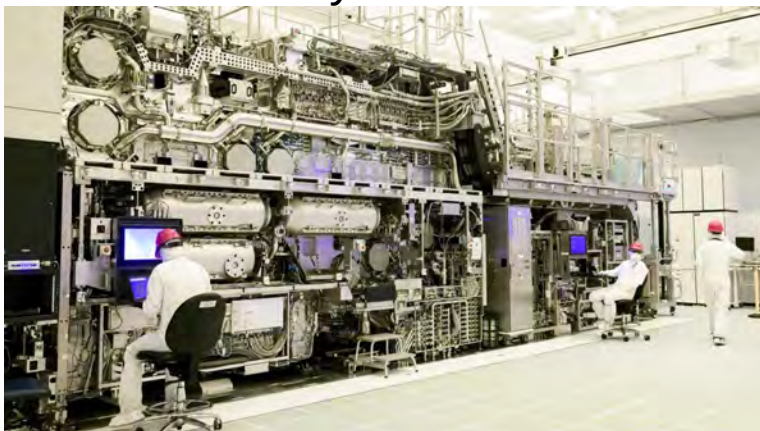




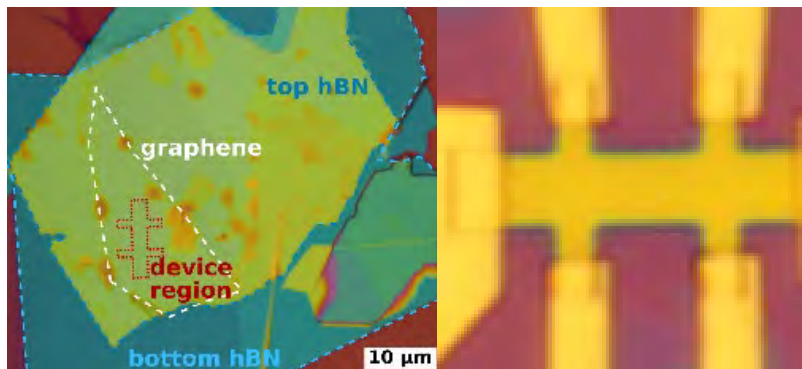
Partner Contributions

- Lithography

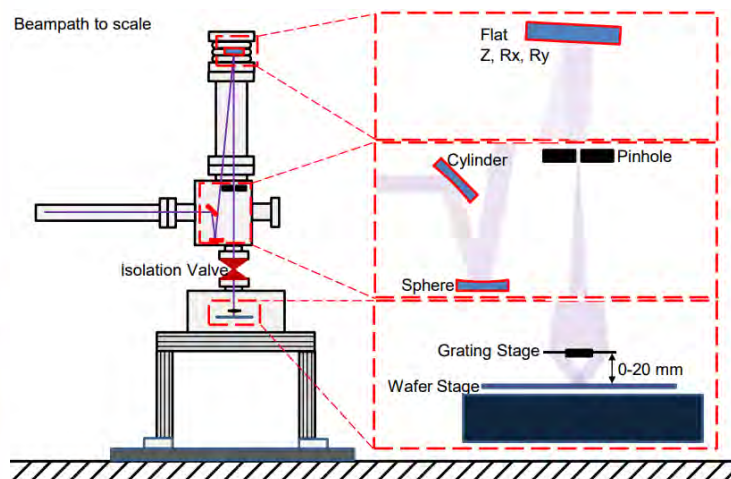
NYCREATES: ASML \$500M Tool
Production only!



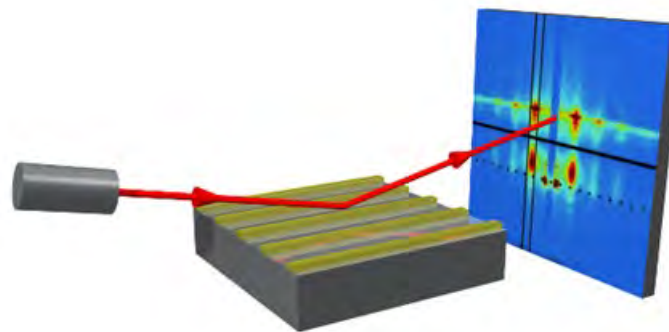
- Materials



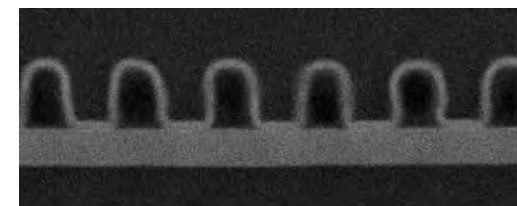
- Metrology



National Lab
Develop next
generation:



18 nm HP (half-pitch) EUV pattern



Courtesy of Dario Goldfarb, IBM Yorktown

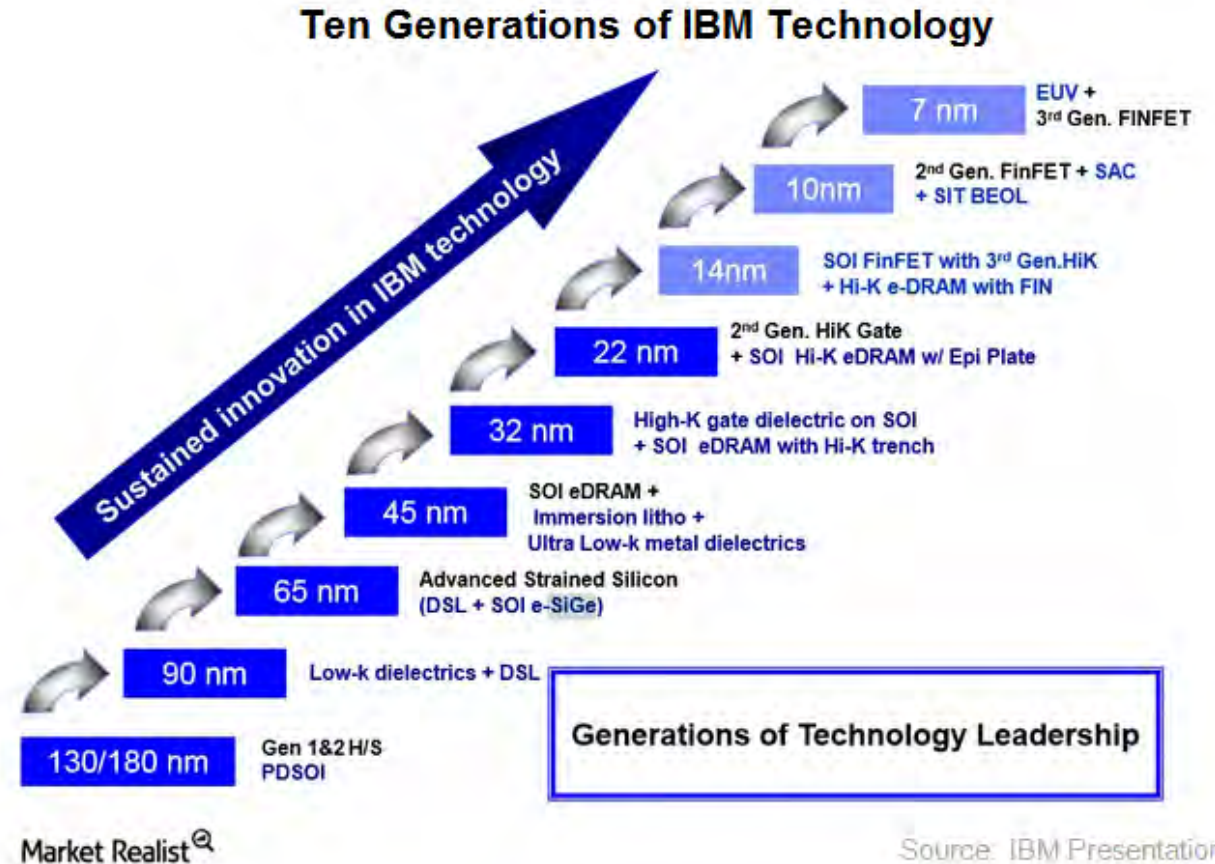
BNL and Microelectronics History

DOE Facilities play a crucial role in the national Microelectronics mission: Synchrotron impacts on CMOS: an IBM 30-year history!

Examples of device contact work using synchrotrons:

- Extended the usefulness of TiSi₂ as a contact material for generations beyond 0.25μm*
- Developed CoSi₂ as a replacement to TiSi₂ for the 130 and 90 nm technologies.
- By understanding defects in Ni/Ni silicides, helped the development of Ni-based contacts for 65, 45, 32 and 22nm planar technologies*
- With Samsung, IBM developed Ni-based contacts on III-V substrates for use in nFETs
- Ti-Si contacts optimized for use in 2nm node in FinFETs

Note: other areas of impact, BEOL metals, diffusion barriers, etc



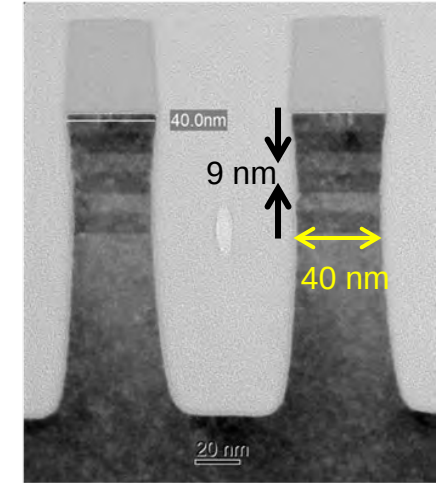
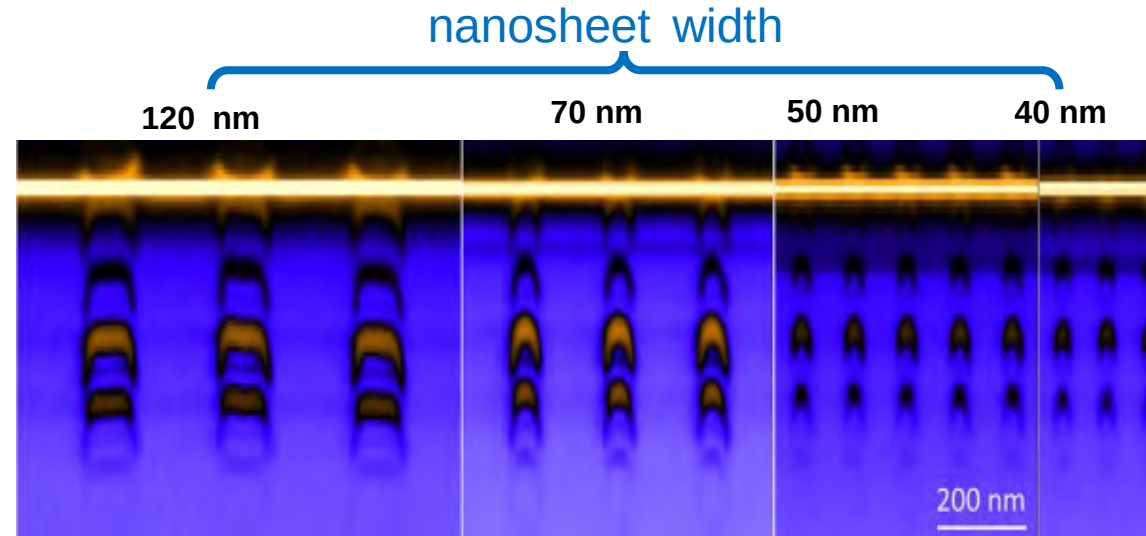
Over the decades IBM synchrotron material studies have helped maintain a competitive advantage as new generations of technologies are developed.

Nanoscale Scanning Imaging of FinFETs

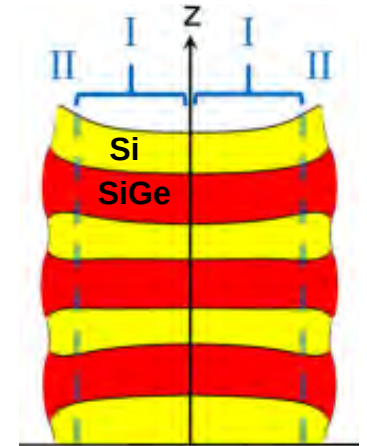
MOTIVATION: understanding the strain profile of nanosheet devices provides understanding of their performance

OPPORTUNITY: NSLS-II provides high intensity soft x-rays tools that were used to elucidate connections between microscopic material properties and qubit coherence

APPROACH: Scanning imaging using a focused x-ray beam (down to 10 nm) offers high-sensitivity multimodal imaging to study broad range of material properties (morphology, composition, oxidation state, crystalline phase and strain)



IMPACT: Strain in nanosheets was mapped out by nanobeam diffraction, providing empirical data need for developing a strain model for nanosheets Commun Eng, 1(1), 11 (2022)





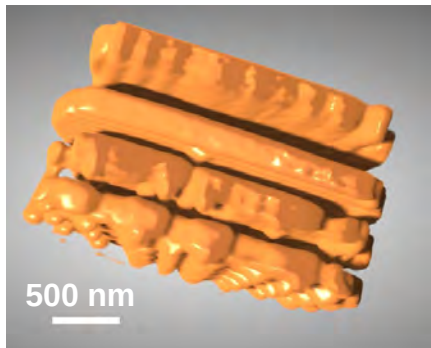
AI-enhanced Imaging of Microelectronics

- Full rotation 3D tomograms are time-intensive to collect and sometimes not even possible
- Adding AI into the analysis loop greatly reduces the amount of data needed to be collected

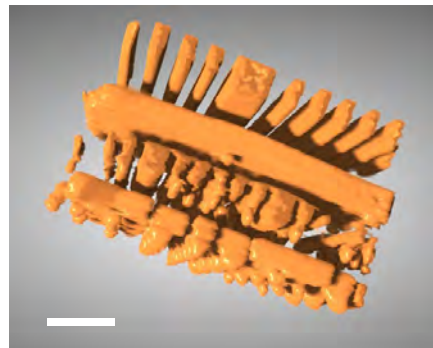
$$\hat{\mathbf{x}} = \underset{\mathbf{x}}{\operatorname{argmin}} \frac{1}{2} \|\mathbf{y} - \mathbf{A}\mathbf{x}\|_2^2 + \lambda R(\mathbf{x}) \quad 44 \text{ M parameter model}$$

- Dramatic increases in thru-put and applicability

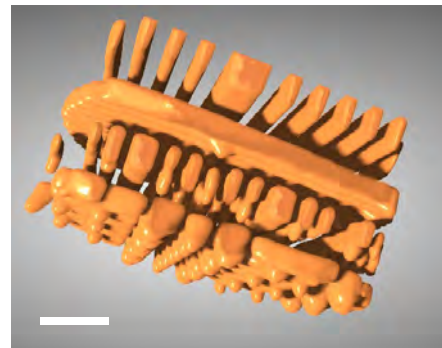
Conventional



AI-enabled

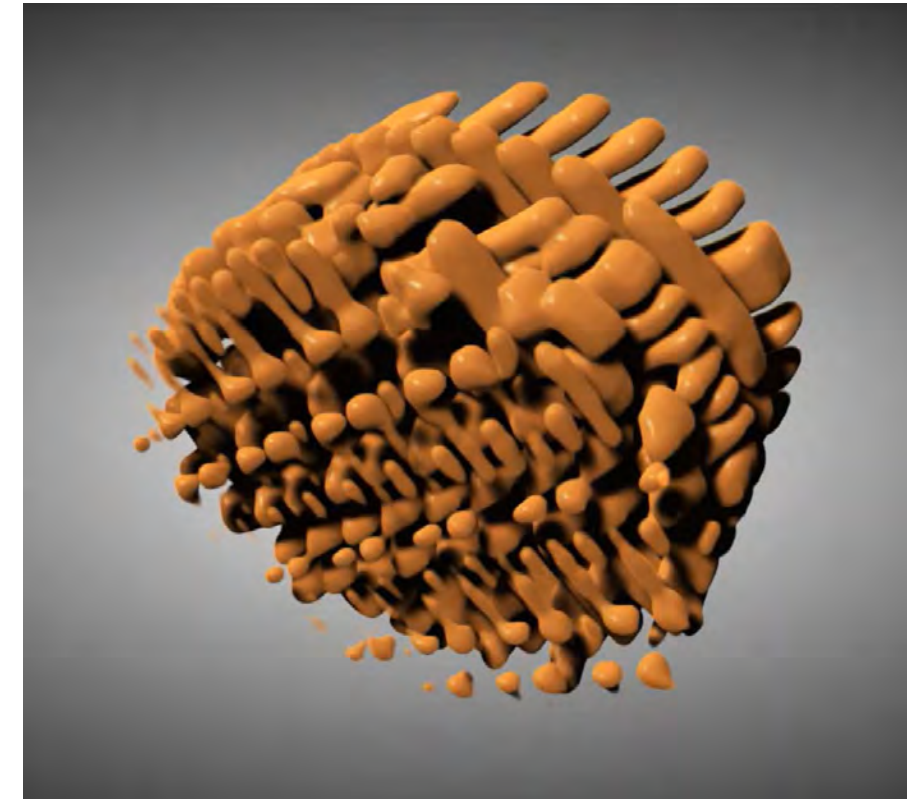


Ground-truth



Subset 84° data

Full 180° data



Cu interconnects in 3D - Legacy intel chip fabricated at 22 nm process node

NPJ Comput. Mater., 11, 240 (2025).

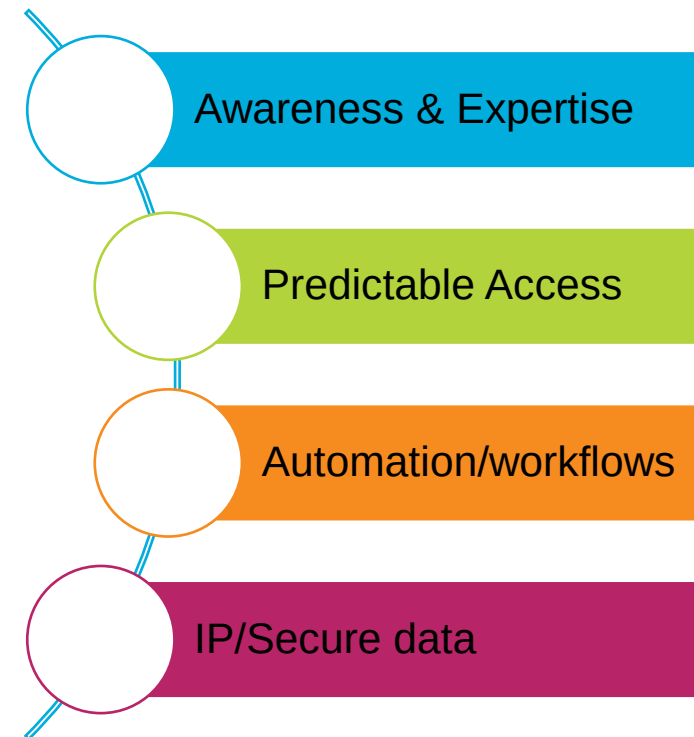
How can National Labs Impact Microelectronics?

Industry need

- Rapid, reliable feedback on materials properties, structures, interfaces, and process-induced changes
- Advanced X-ray and nanoscience capabilities can provide sensitive, non-destructive characterization of thin films, nanoscale features, and device-relevant structures

Opportunity

- Better connect microelectronics industry needs with unique capabilities and expertise at BNL and LBNL
- Explore both applied and fundamental research opportunities
- Build on engagement with NY Creates and industry partners



What the Pilot Will Explore

Engagement & Access

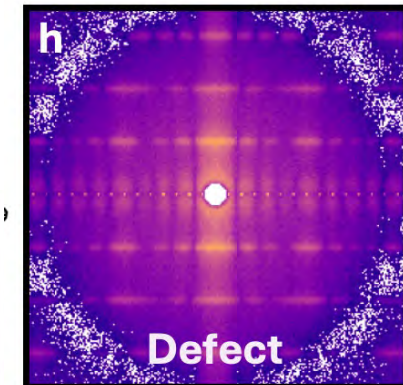
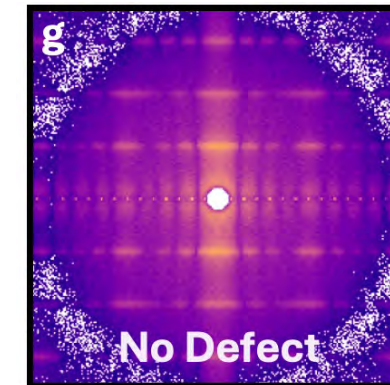
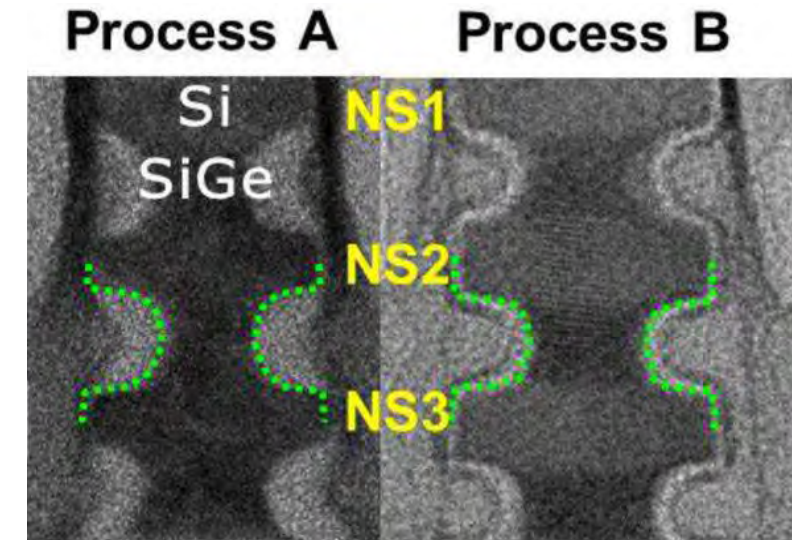
- Industry engagement and awareness
- Reliable and repeatable access pathways
- Streamlined onboarding and technique selection

Experiments & Capabilities

- Identify relevant facility capabilities and expertise
- Initial focus on microelectronics metrology and lithography
- Pilot experiments using selected capabilities

Data & Workflows

- More standardized and automation-friendly workflows
- Secure handling of proprietary information
- Pathways to AI/ML-ready datasets



Priority Actions

- Broaden engagement between the microelectronics industry and National Labs to identify high-priority areas of mutual interest and potential pilot activities.
- Support awareness of National Lab and user facility capabilities through industry meetings, technical exchanges, site visits, and other appropriate engagement.
- Assess the scientific expertise, facility capabilities, staffing and bridging functions, infrastructure, workflows, and automation that will be useful for industrially relevant experimentation.



Next Steps

- Continue technical exchanges with NY CREATES and industry stakeholders to identify high-priority pilot opportunities, relevant facility capabilities, reliable access pathways, staffing and coordination needs, and enabling tools and workflows.
- Use these discussions and initial projects to refine the scope, governance, access model, workflows, and longer-term partnership model.



Initial Technical Focus Areas

Lithography

Next-Generation Lithography

Next-Generation EUV & Beyond EUV (BEUV) Interference Lithography Capability

Project Description

- Extend the BNL's 13.5 nm EUV Grating Interference Lithography (EGIL) platform to (a) high & hyper-NA EUV and (b) to 3.1 nm BEUV in partnership with LBNL/CXRO
- Design EUV gratings for variable high- and hyper-NA exposures
- Design a 3.1 nm illuminator for BEUV interference lithography
- Develop and optimize BEUV multilayer optics/coatings
- Integrate into EGIL & demo the variable NA and BEUV IL capability
- Prepare for the ALS validation and preliminary industry user access at LBNL (Phase II) & final installation and full industry user operation at BNL (Phase III)

Importance to Industry

- Enable R&D for high- & hyper-NA EUV and BEUV lithography at 3.1 nm for future nodes
- Support development and evaluation of EUV patterning under high & hyper NA as well as BEUV optics, photoresists, and patterning processes
- Complement the ASML high-NA EUV and the planned xLight free-electron laser (FEL) at Albany NanoTech by providing a BEUV research platform
- Strengthen partnerships among BNL, LBNL/CXRO, IBM, and NY CREATES for accelerating future EUV & BEUV technologies

EGIL
Extreme Ultraviolet Grating Interference Lithography



Schematic of BNL EGIL platform being developed in partnership with LBNL/CXRO (the system to be completed by Jan 2027)

Logos: Brookhaven, BERKELEY LAB, creates, IBM

Metrology

Advanced 3D Metrology

X-ray Metrology on EUV Lithography Structures

Project Schedule

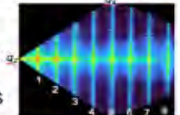
- Fabrication of lithography structures at NY CREATES and ALS (2-8 months)
- Development of analysis pipeline, integrating data simulation, data acquisition, data analysis and visualization (0-6 months)

Milestones:

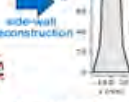
- Completion of robust analysis pipeline for CD-SAXS with the side-wall reconstruction.
- Establishment of workflow for GISAXS and resonance scattering.

Staffing and Materials

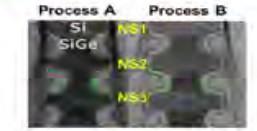
- 1 postdoc for supporting data collection and data analysis
- 20% staffing for piolet project, 20% staffing at CMS, 20% staffing at SMI, 10% staffing at CFN
- 10% staffing at NY CREATES 10% staffing at IBM
- ~\$200k for miscellaneous materials and travel



Side wall reconstruction from CD-SAXS



Process A Process B



Visualizing the "Half-moon" defect in nanosheet is one of the problems.
Stefan, Schoëche, IBM

Logos: Brookhaven, creates, IBM, ALS



U.S. DEPARTMENT
of **ENERGY**



Blue-X

