Development of CoRDIA: an imager for Diffraction-Limited Synchrotron Rings and Continuous-Wave Free Electron Lasers

on behalf of the *CoRDIA* collaboration

*CoRDIA*ASIC

BONN

DESY.

Acknowledgements

- the team (A. Klujev, S. Lange, T. Laurus, D. Pennicard, U. Trunk, C.B. Wunderer, H. Krueger and H. Graafsma)
- NIKHEF (particularly V. Gromov and A. Vitkovskiy), for allowing us to use a version of the PCS-GWT circuit
- CERN and the RD53 collaboration, for allowing us the reuse of CMOS IO pads and SOFIC ESD structures in our design
- Europractice, IMEC and CERN for their MPW and design tool support
- the Caribou collaboration, for providing us with a versatile system for prototype testing

Outline

- Motivation
- Overall architecture
- Development plan
- Prototypes
- Test results
- Summary

current imager types in photon science

CoRDIA ASIC

imager example for SR: LAMBDA

- Up to 10 megapixel (55 µm pixel size)
- 2 kHz frame rate (continuous)

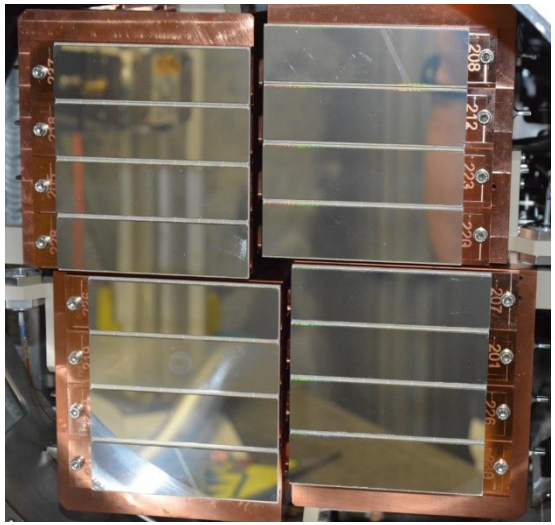
or MM-PAD-1 → 2.1

- 1.1kHz →10 kHz (continuous)

or CITIUS

- 17.4 kHz (continuous)

for high-repetition rate FEL: AGIPD



- 1 megapixel (200µm pixels), 4 megapixel in development
- 4.5 MHz burst imaging (internal storage: 352 images)

or LPD (500µm, 500img)
or DSSC (hexag, Ø≈230µm, 800img)

- 4.5 MHz burst imaging (internal storage) 4

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SR: 3rd → 4th gen (diffraction limited)

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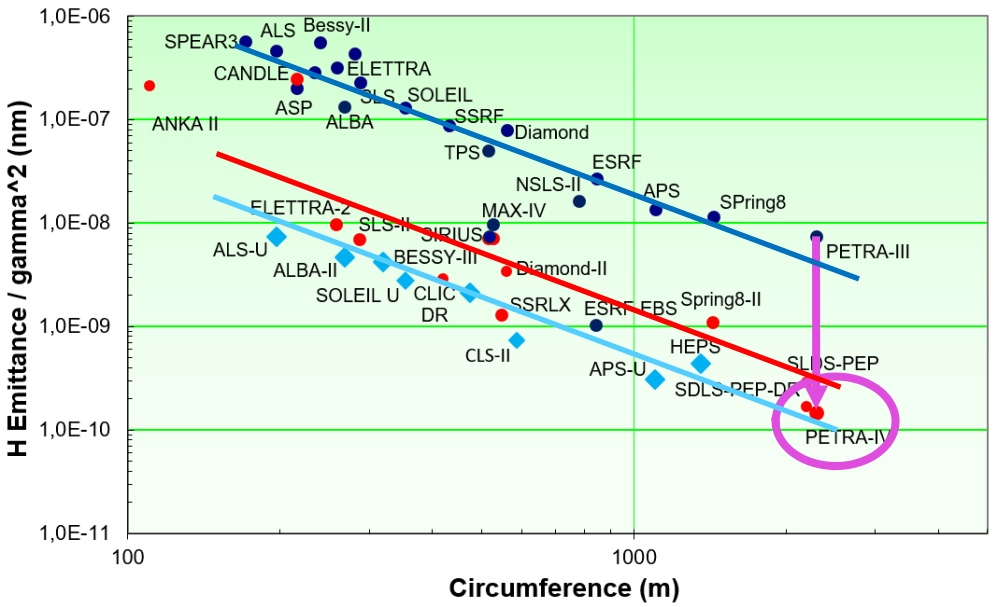
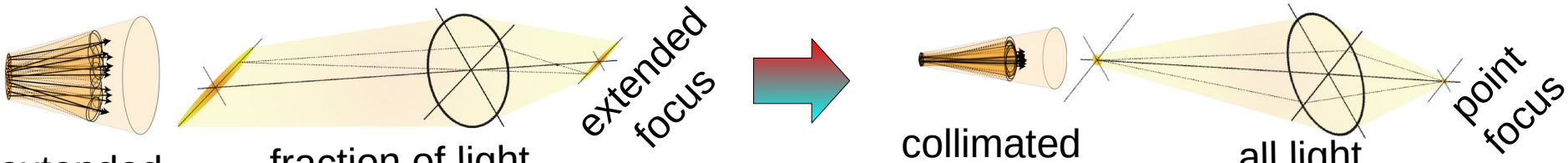


Multibend-achromat technology

On-axis inj. +technology

→ more collimated beam



extended source

fraction of light hits optics

collimated beam

all light hits optics

→ more ph/s on the detector
Frame rate requirements in experiments increase from kHz to >100 kHz

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FEL: reducing gaps / elongating trains

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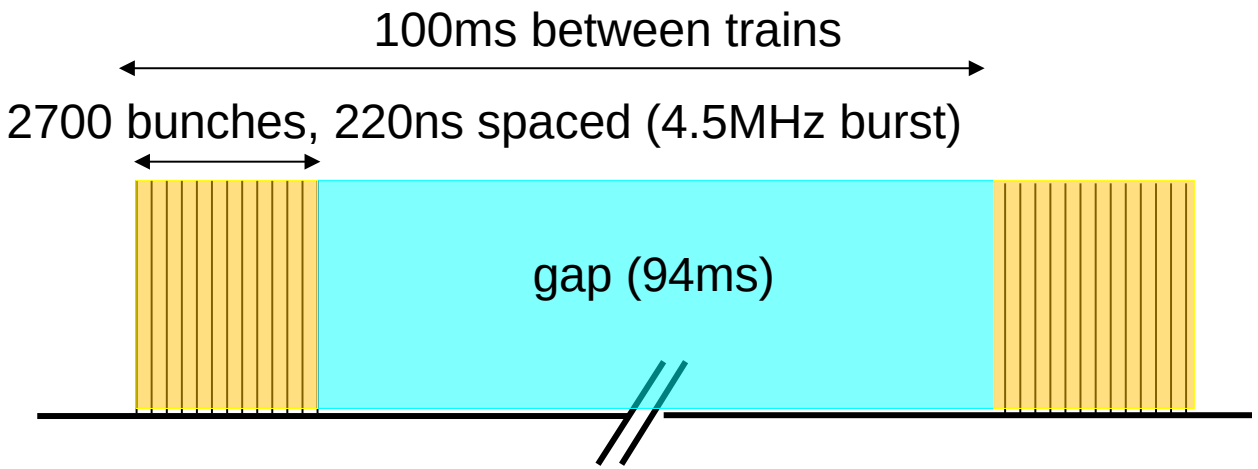
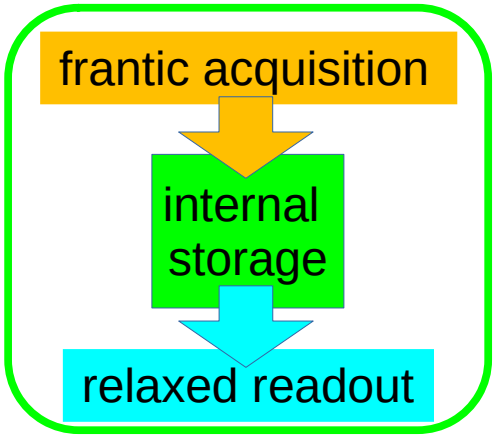
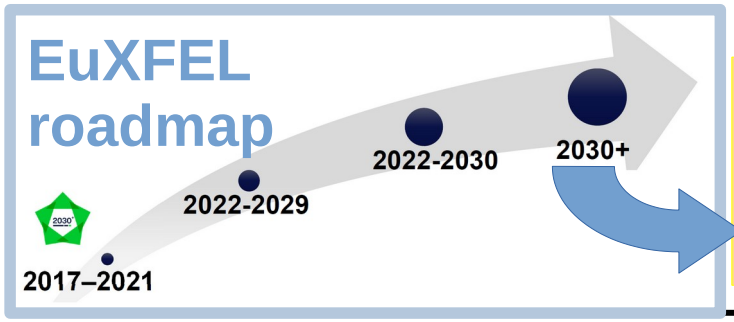
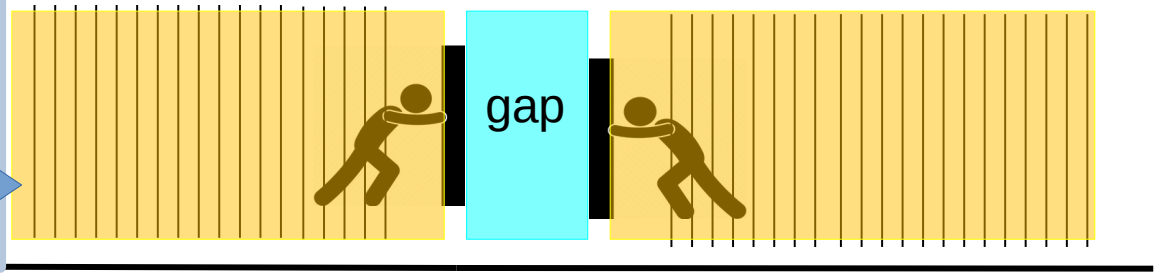








"many more" bunches in "much longer" trains at "slightly reduced" rate

"much smaller" gaps (ideally, full CW)

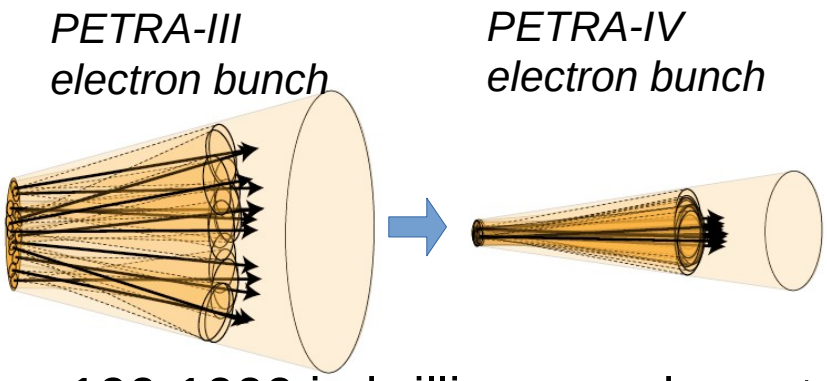
What we can interpret: **bunches spaced 1us** to 100us, **most of the time**

→ frantic acq/relaxed readout no longer an option (no space for large internal memory anyway)

BONN DESY.

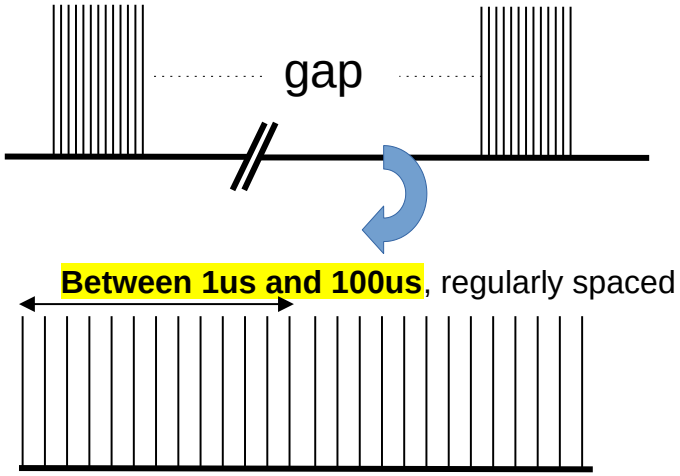
coming source upgrades

PETRA-IV: Upgrade to diffraction limited ring (~2030)



- x100-1000 in brilliance, coherent flux
- Frame rate req. in experiments: from kHz to >100 kHz (continuous) readout

European XFEL: CW mode operation (20??)



many more [O(1)] bunches per second
no gap for burst-readout of internal storage

common need for:
- continuous readout
- > 100kHz frame rate

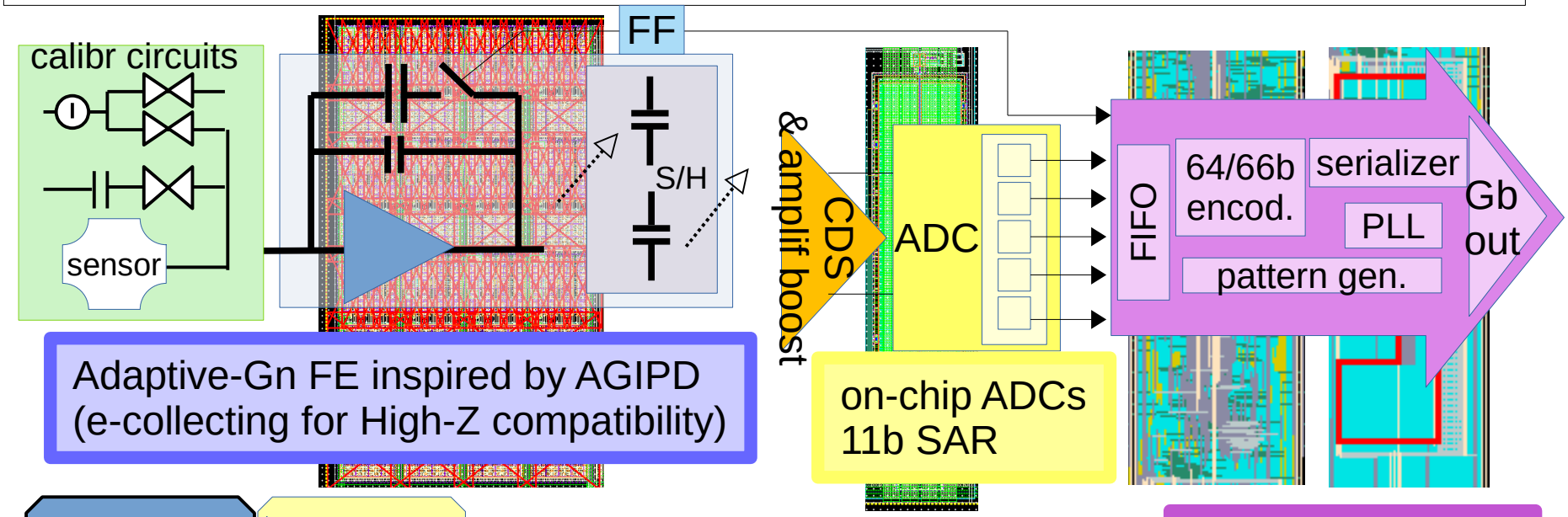
(pro-term)

COntinuous Readout Digitising Imager Array

CoRDIA ASIC

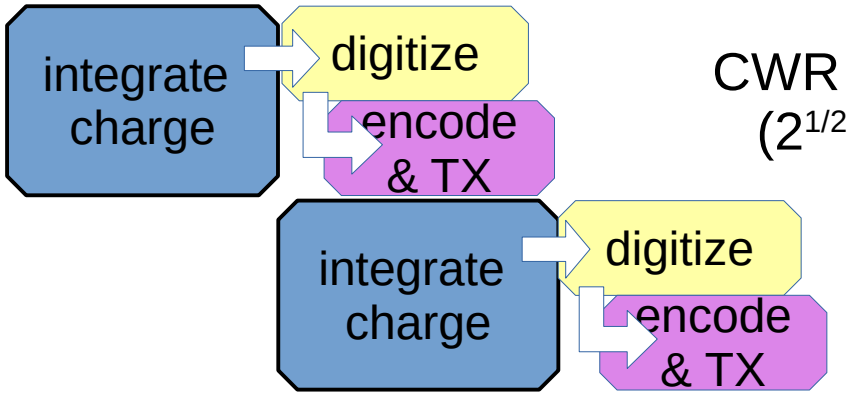
our goals

- 150 kHz, continuous
- ~110 µm pixel size
- 1-photon sens. 12 keV
- charge-integrating (FEL-compatible)
- a-few-k ph/pix/img (aiming 10k, not there yet)
- compatible with High-Z



Adaptive-Gn FE inspired by AGIPD
(e-collecting for High-Z compatibility)

on-chip ADCs
11b SAR



CWR scheme
($2^{1/2}$ stages pipeline)

(PCS +) GWT
devel. by Nikhef
for Timepix4

TSMC 65nm

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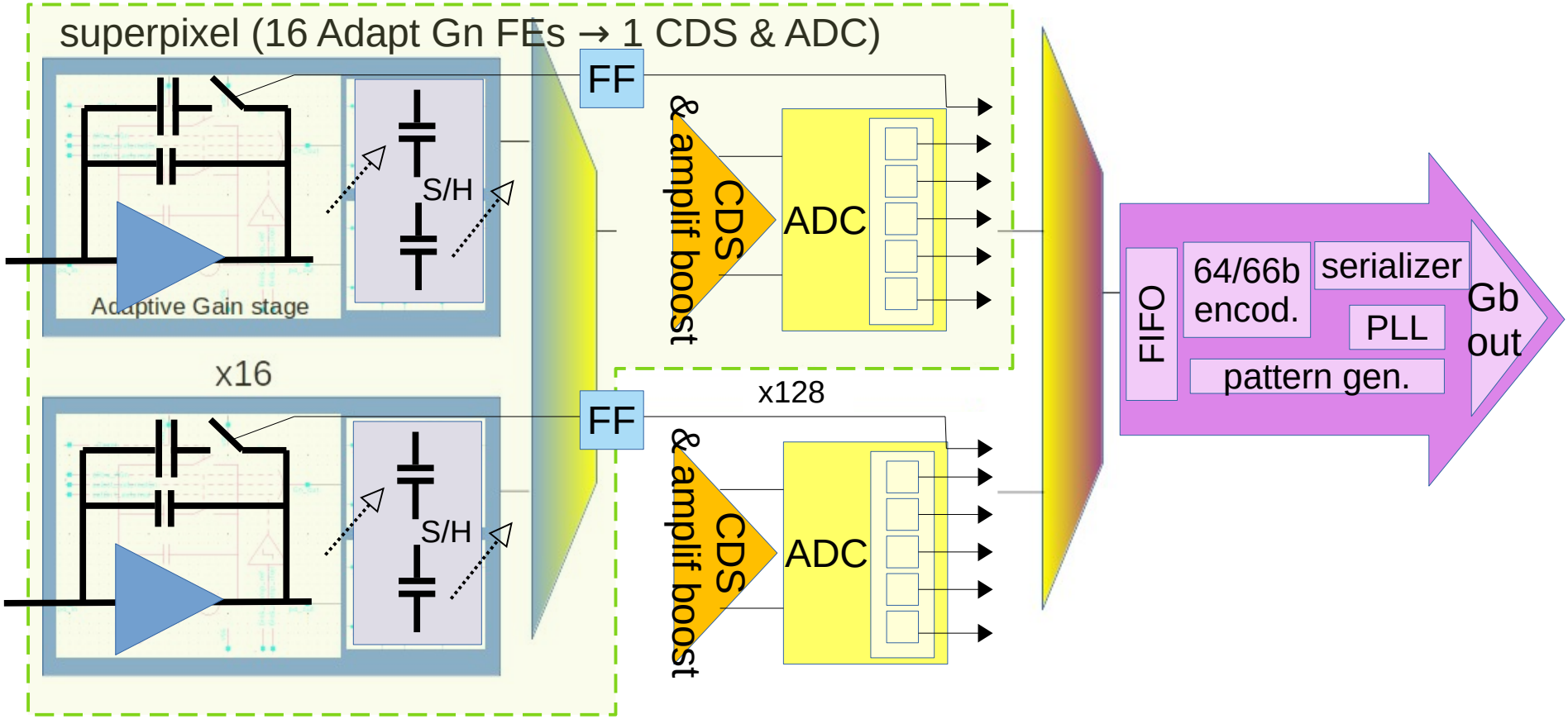
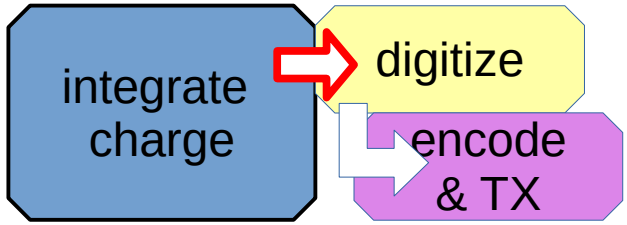
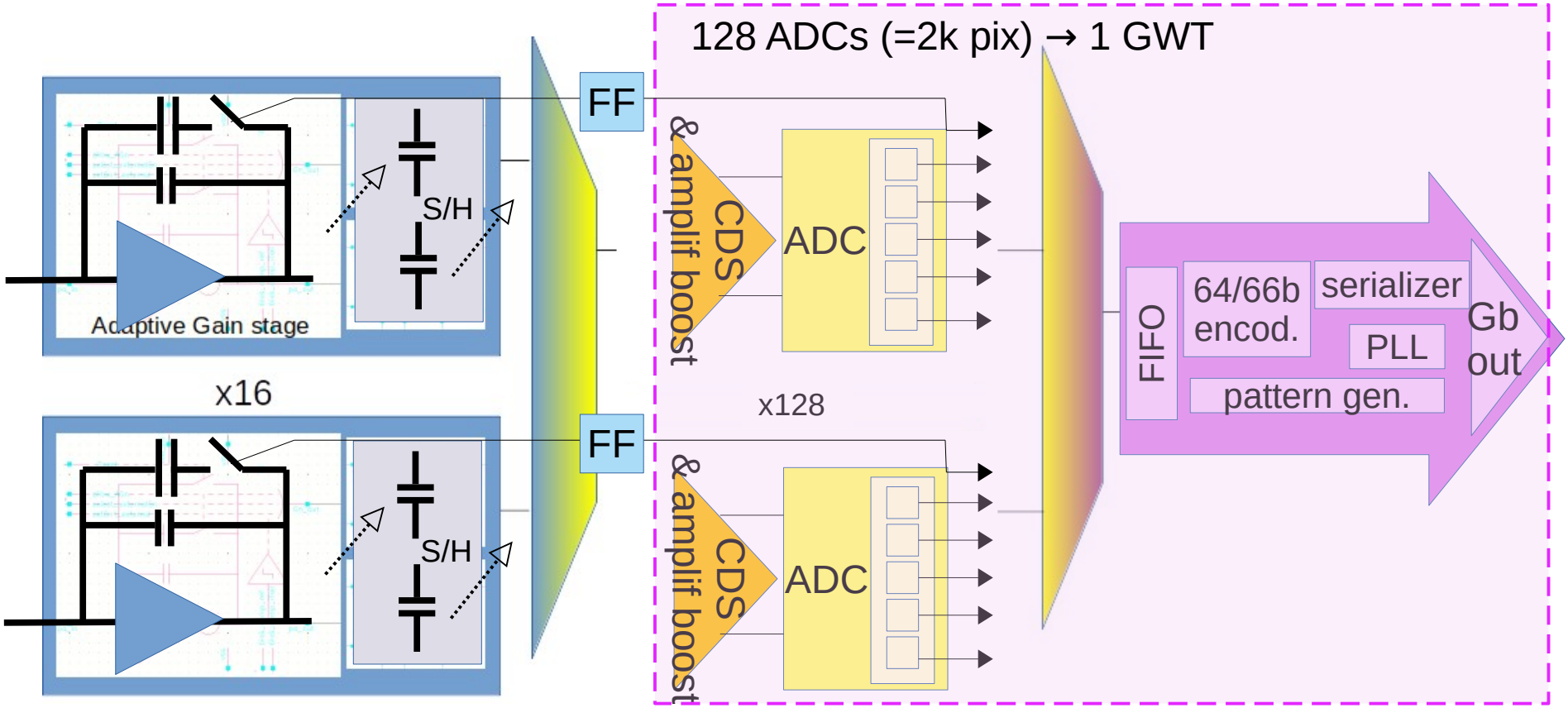
CoRDIA$_{ASIC}$ structure

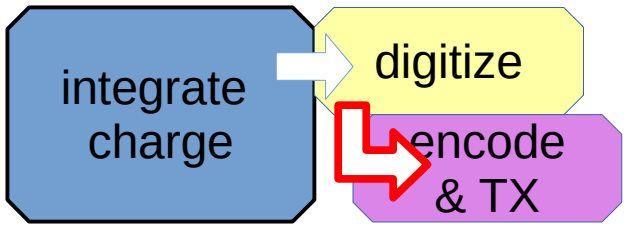




sequential digitization (11b) + Gn bit of the former image per 16 pixels (charge stored in S/H cells)

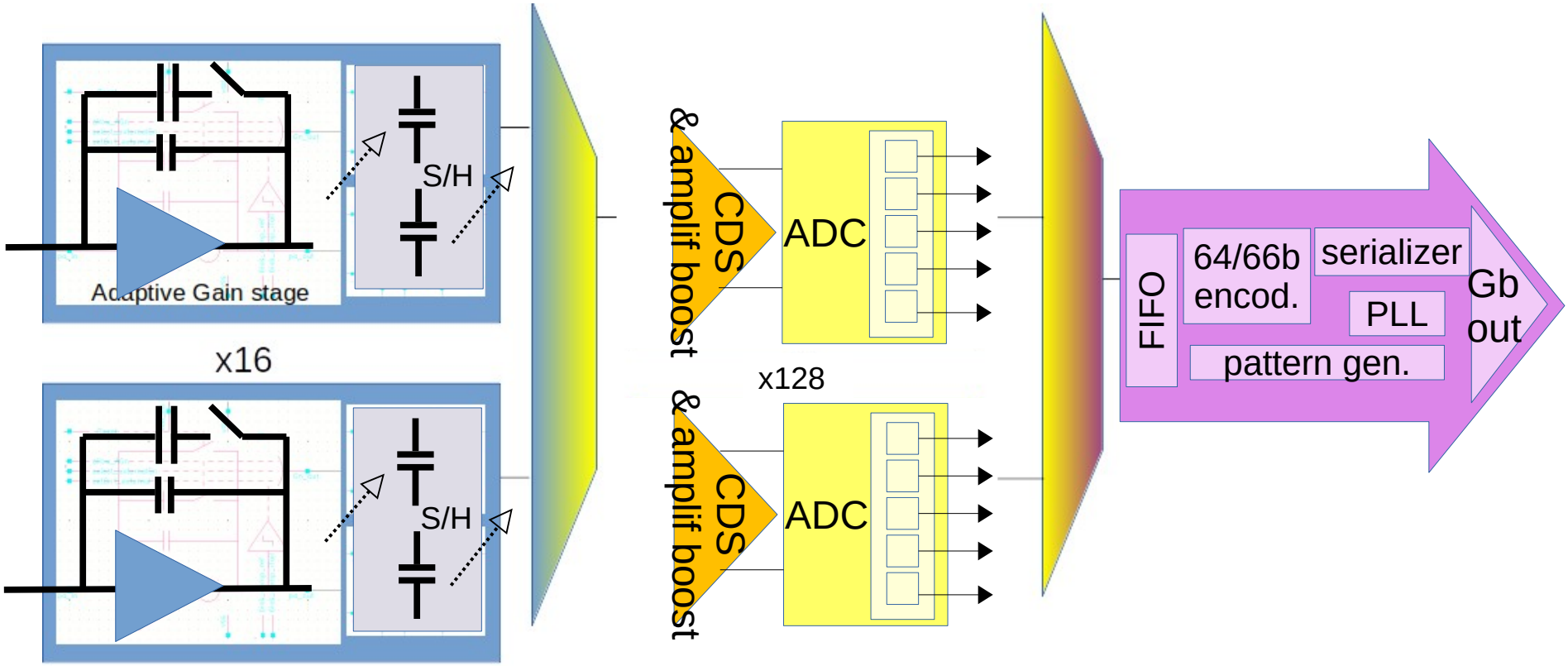
CoRDIA$_{ASIC}$ structure

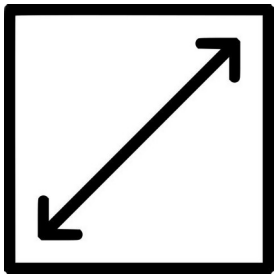




128b from superpixels (2kpix) → 64-66 encod → bit stremout @ 5.12GHz

CoRDIA$_{ASIC}$ structure





56kpixels (256 x 224)
29.96mm x 24.7mm
near (but within) recticle limit

→ 28 GWT/chip

contingency plan
16kpixels (128 x 128)
15mm x 15mm

→ 8 GWT/chip

our plan

CoRDIA ASIC

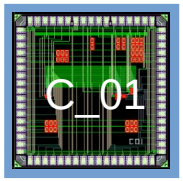
validation of individual circuit blocks

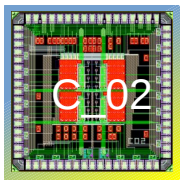
validation of circuit chain as a pixel array

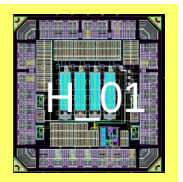
validation as a component of the overall detector system

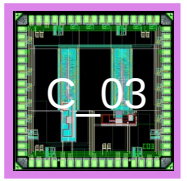
exploratory MPWs (TSMC65)

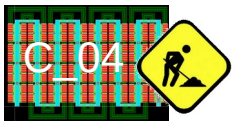
MPWs











performance improvement study

expansion to full-scale ASIC

1st gen ASIC

target pixel pitch, readout 150kHz

1st xrays @ P-IV start-of-op (expected ~2030)

performance improved ASIC

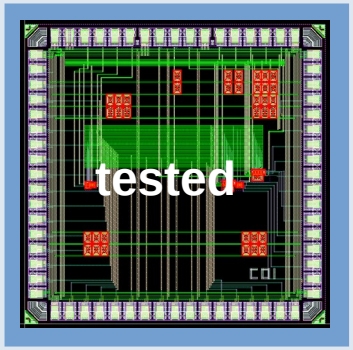
2nd gen ASIC

aim at:
fix bugs (if any),
ext. dyn range,
min. blind areas

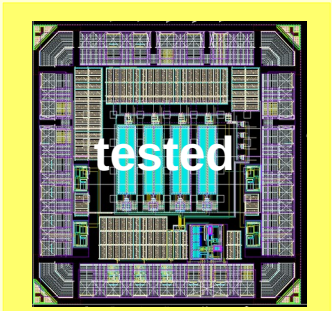
BONN

DESY.

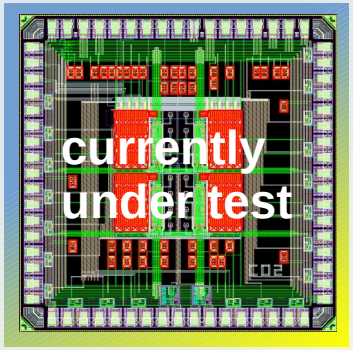
MPWs



2021: CoRDIA_01
Designed, produced, tested.
Used to validate analog circuit blocks as at the expected frame rate

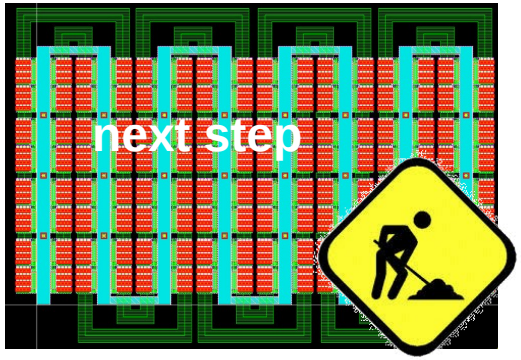


2021: HSI_ADC01
Designed, produced, tested.
Used to confirm image sampling capability at the expected frame rate



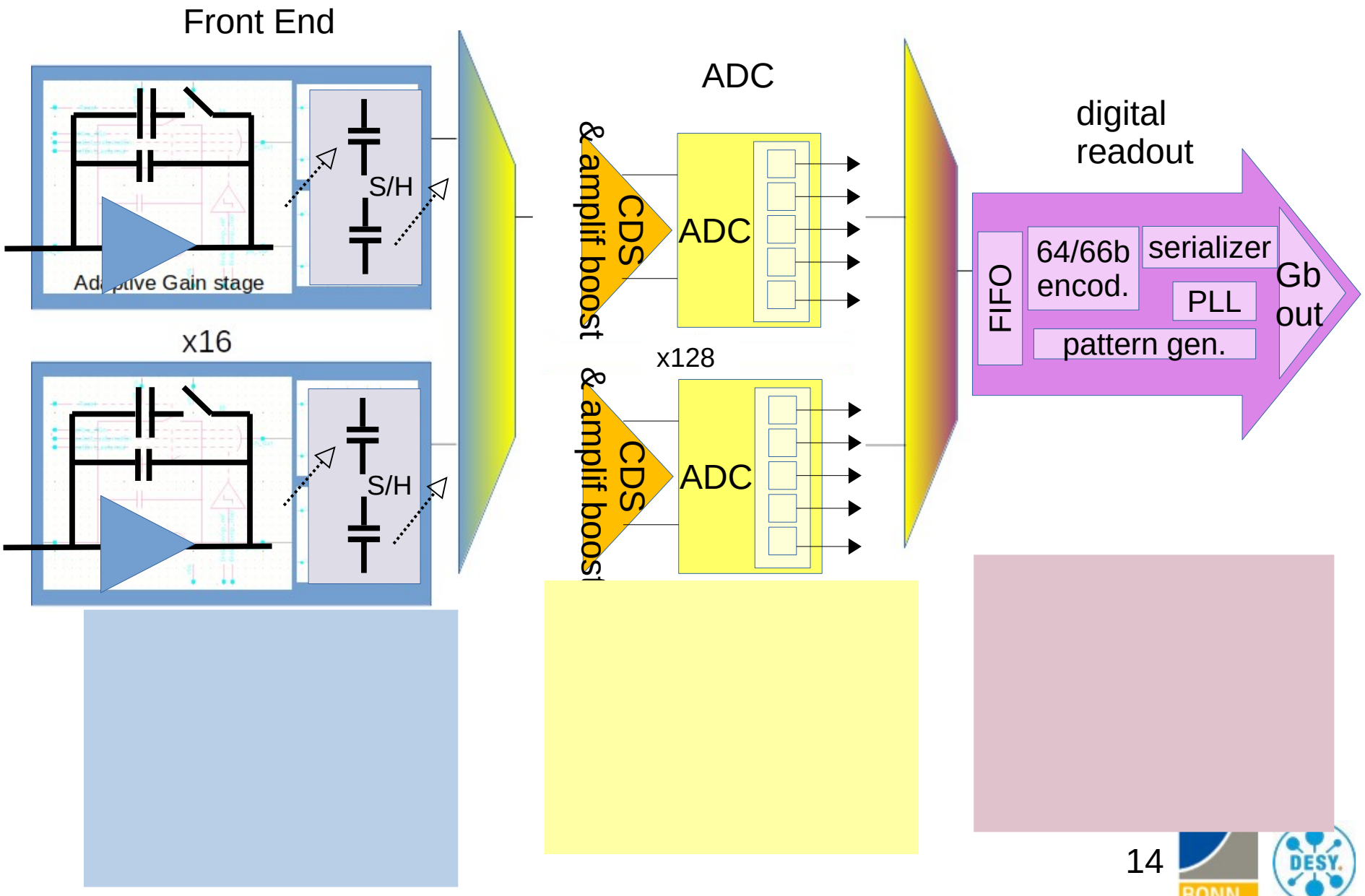
2022-2023: CoRDIA_02
Designed, produced.
Currently under test.
Used to validate pipeline signal-processing and evaluate performances.

2023: CoRDIA_03
Designed, produced, being wire-bonded now
Test expected summer.
Will be used to validate the PCS+GWT circuit, optimized to CoRDIA.



CoRDIA_04 prototype-to-come: small-sized pixel array (~2kpixels, design in progress, expected after C03 test) floorplanning as a meandering structure to emulate full-size chip size “column” (to estimate eventual drops before full-size chip engineering run)

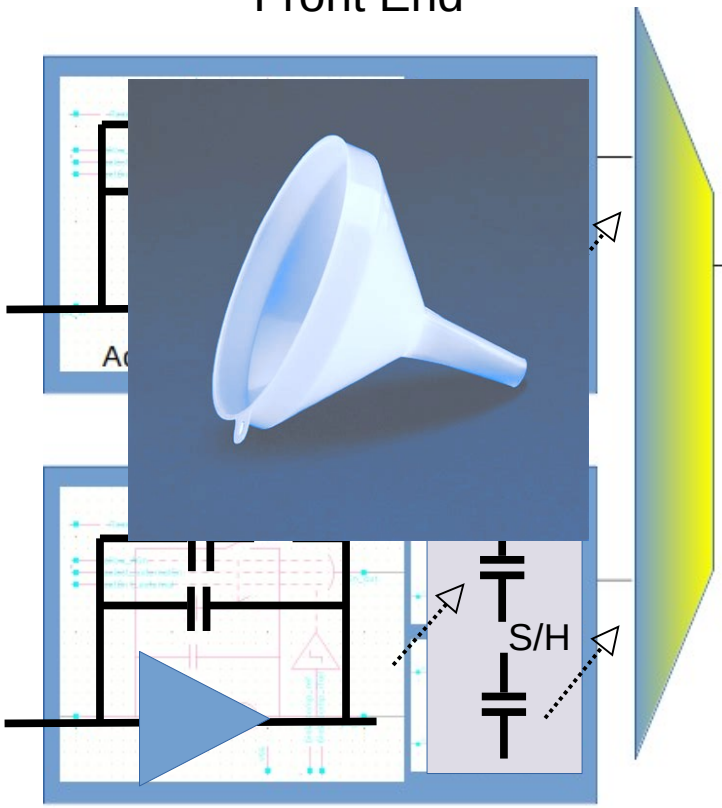
CoRDIA$_{ASIC}$ expectations



CoRDIA$_{ASIC}$ expectations

CoRDIA$_{ASIC}$

Front End

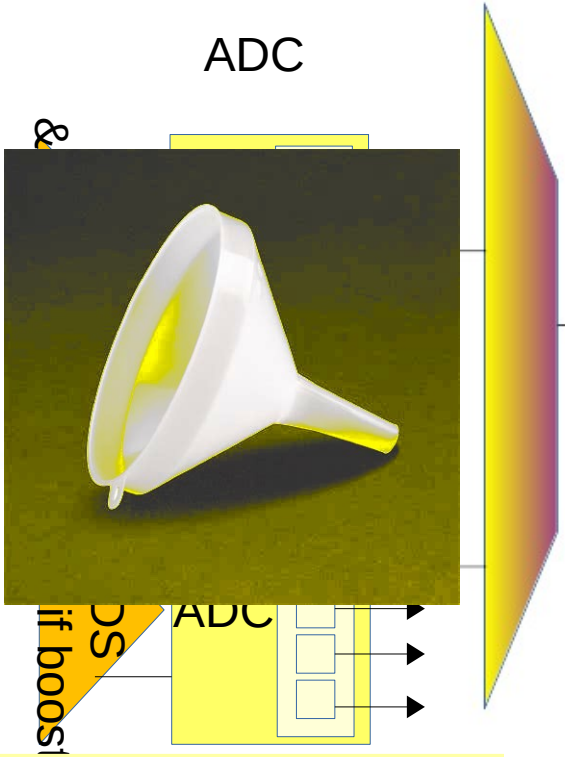


Original spec >100kHz
PetraIV revol. rate 133kHz
Users are greedy kids

→ FE design, tested (DESY)

$$>150\ kframe/s$$

ADC



1 ADC serves 16 FEs, so it needs to operate at least at 150k x 16= 2.4MS/s

→ ADC tested (UniBonn)

$$\frac{2.5\ MS/s}{16\ FE} > 150\ kframe/s$$

digital readout

11 bits, + Gn bit
→ < 2Bytes/pix
*16*128= 2kpixel / GWT*
64-to-66bit encoding

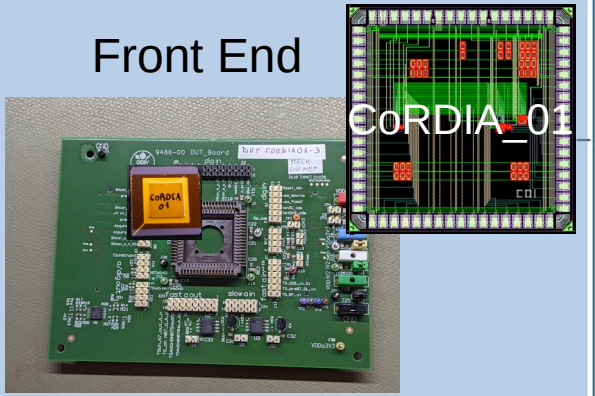
→ GWT tested (NIKHEF)

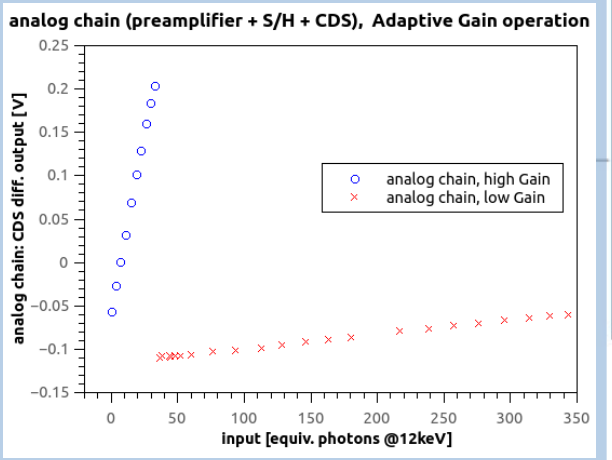
$$\frac{5.12\ Gb/s}{12\sim16b * 2k\ pixels * 66/64} > 150\ kframe/s$$

checking the puzzle pieces...

CoRDIA ASIC

Front End





Adaptive Gain circuit tested by calibr. source (pulsed capacitor) @ expected frame rate

ADC

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→ ADC tested (UniBonn)

$$\frac{2.5\,MS/s}{16\,FE} > 150\,kframe/s$$

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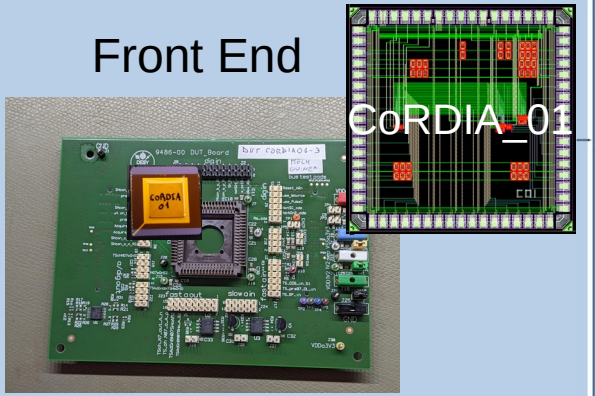
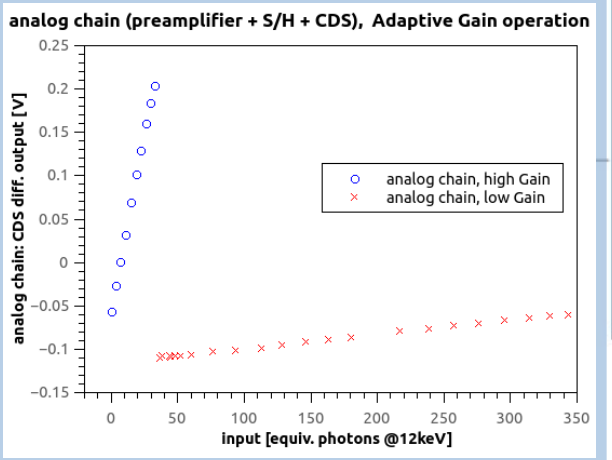
CoRDIA ASIC

Front End





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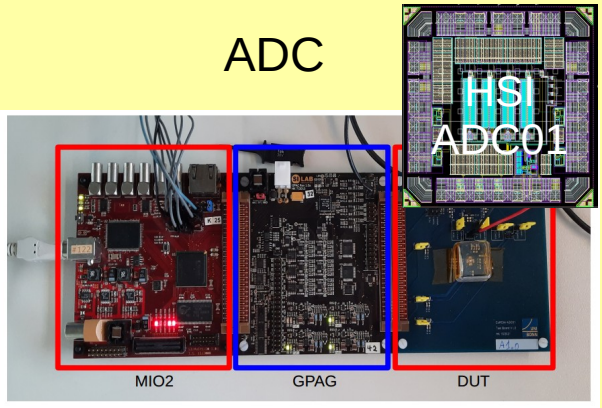
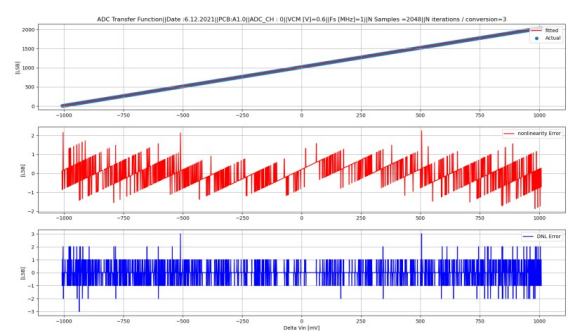
ADC





11-bit SAR developed, tested by UniBonn. DNL , INL test suggests >10ENOBs @ expected frame rate

digital readout

11 bits, + Gn bit
→ *< 2Bytes/pix*
*16*128= 2kpixel / GWT*
64-to-66bit encoding
→ GWT tested (NIKHEF)

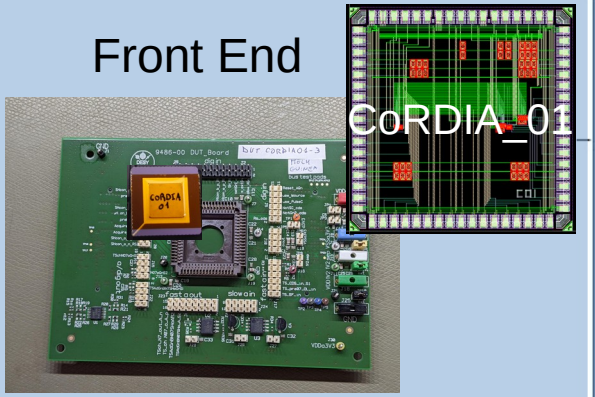
$$\frac{5.12\ Gb/s}{12\sim16b * 2k\ pixels * 66/64}$$

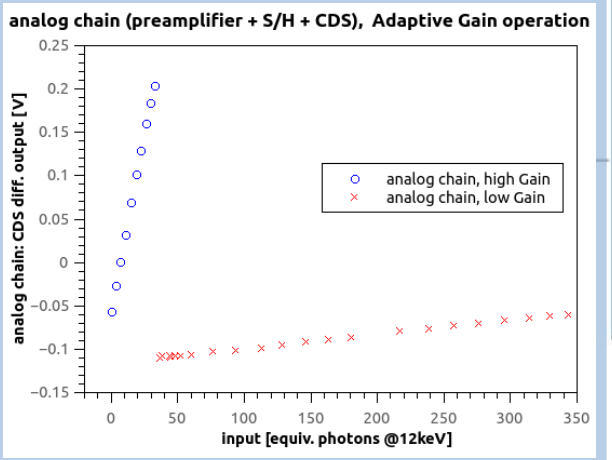
$$>150\ kframe/s$$

checking the puzzle pieces...

CoRDIA ASIC

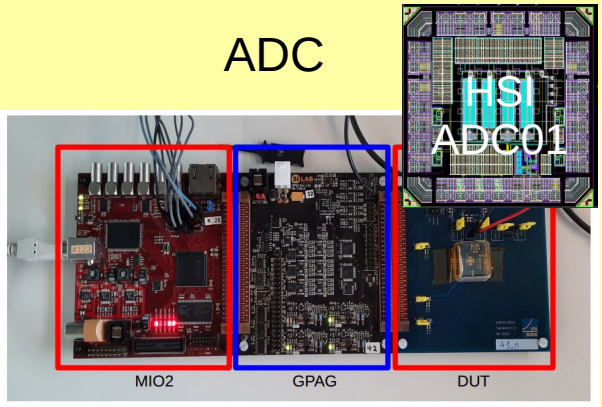
Front End

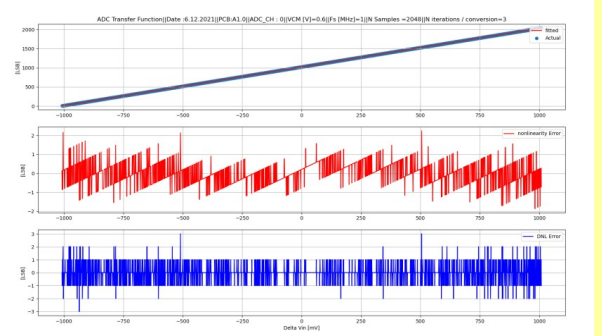




Adaptive Gain circuit tested by calibr. source (pulsed capacitor) @ expected frame rate

ADC

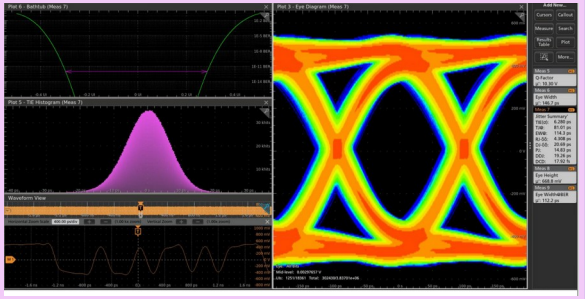




11-bit SAR developed, tested by UniBonn. DNL , INL test suggests >10ENOBs @ expected frame rate

PCS+GWT

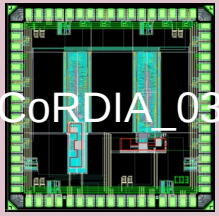
lazy-person approach: reuse Timepix4 solution



X. Llopart on behalf of the Medipix4 collaboration
11 Feb 2022, CERN seminar

prelim: NIKHEF & Medipix collab.: good eye diagram @ 5.12 Gb/s.

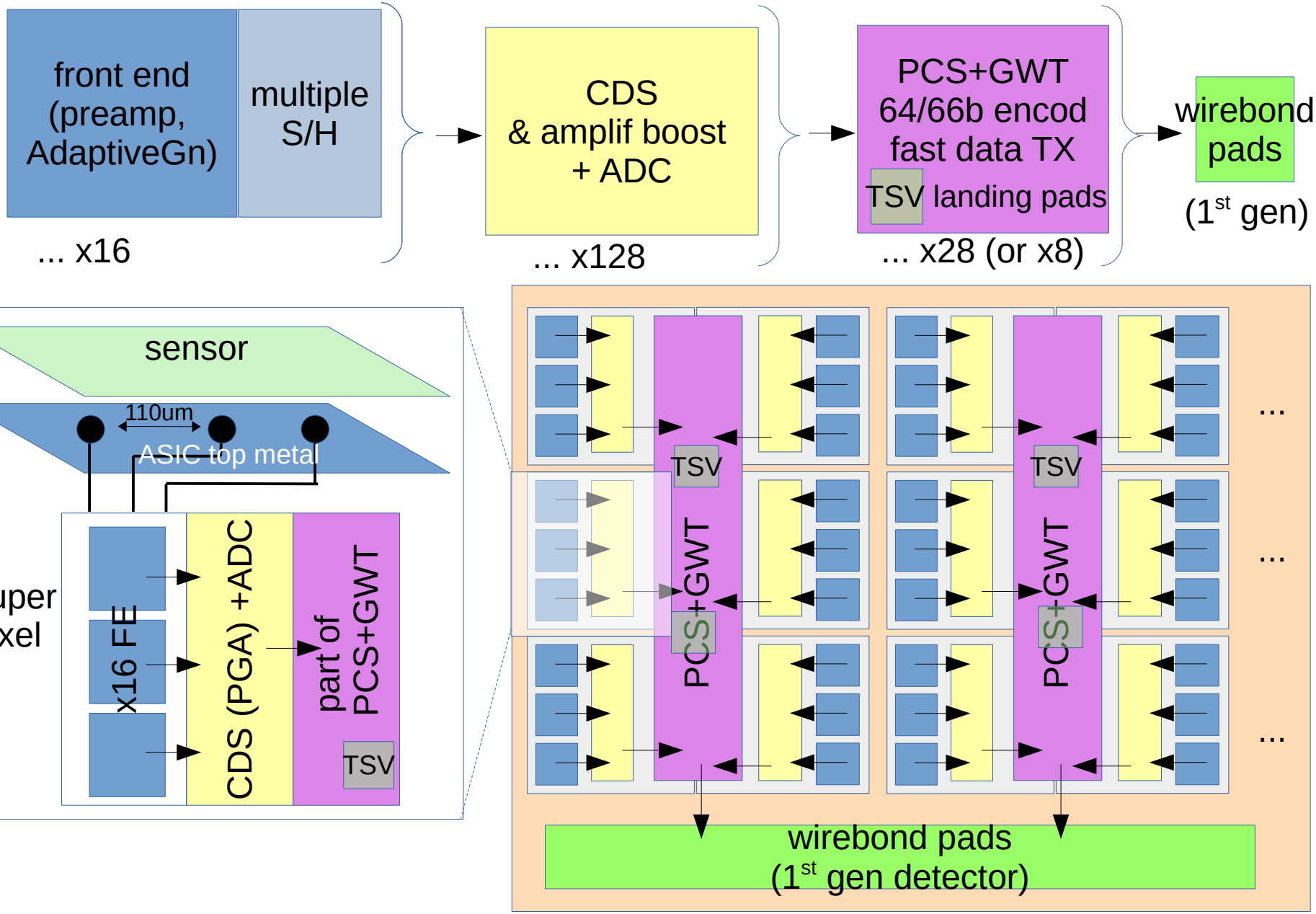
adapted circuit perform.



to be confirmed on CoRDIA prototype (being wirebonded)

...looking at the picture on the box...

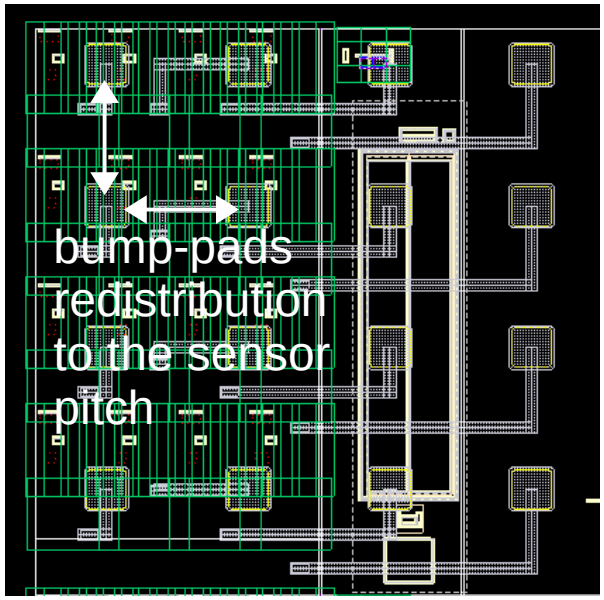
CoRDIA ASIC

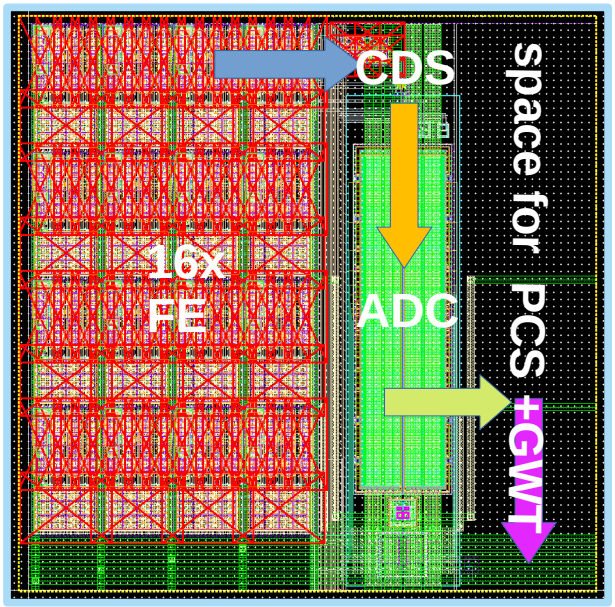


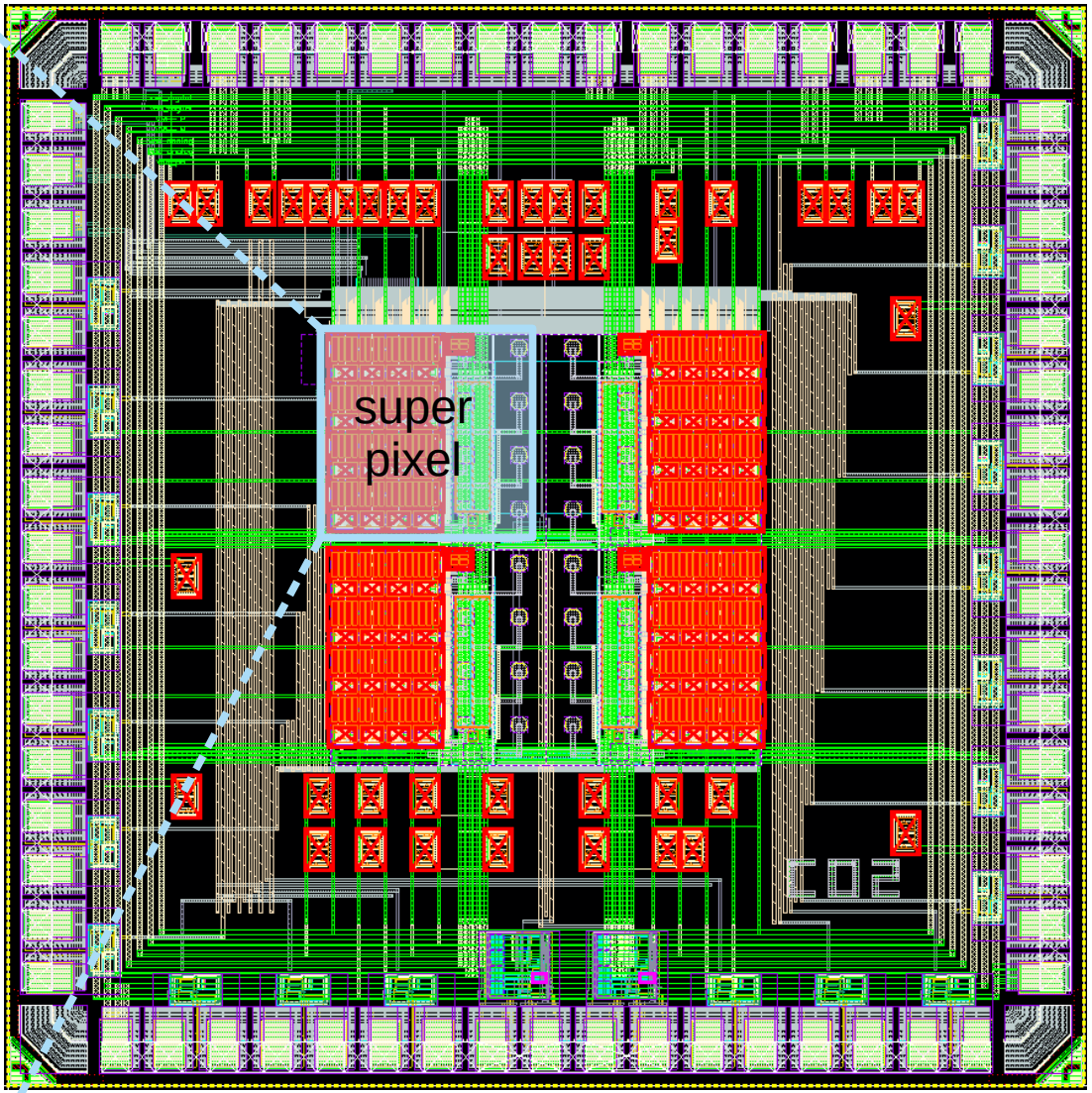
… combining (some of) the puzzle pieces

CoRDIA ASIC

pad redistrib on top metal



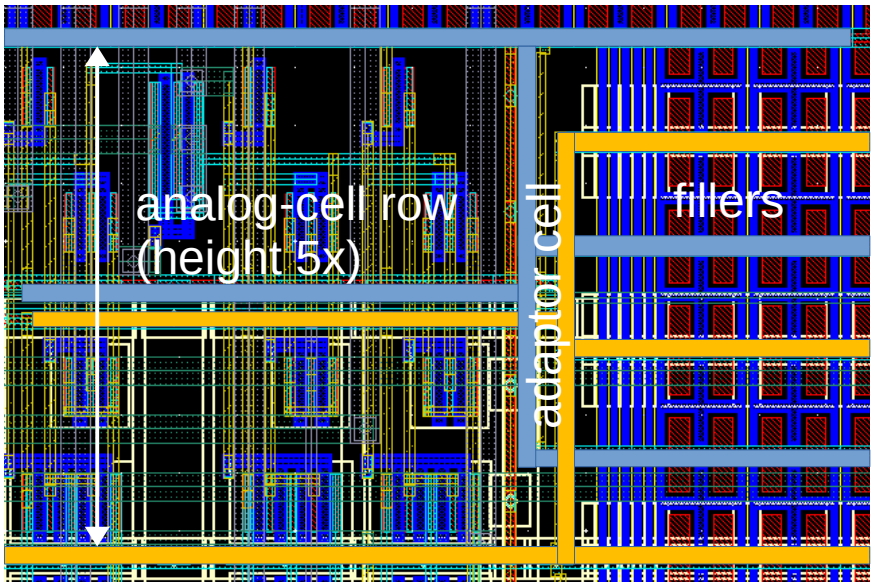


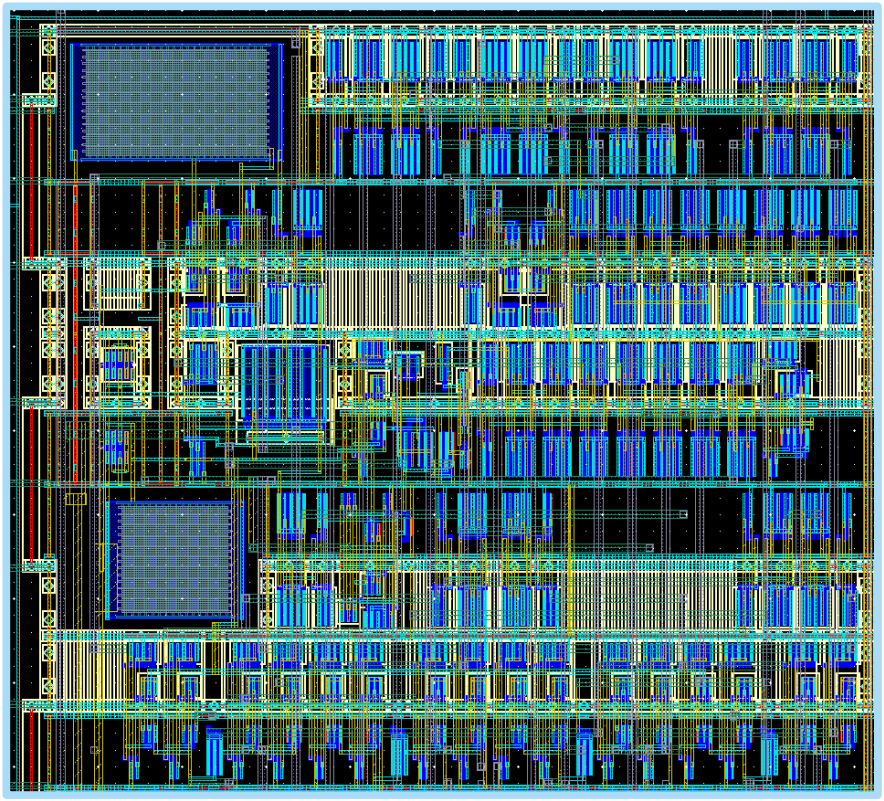


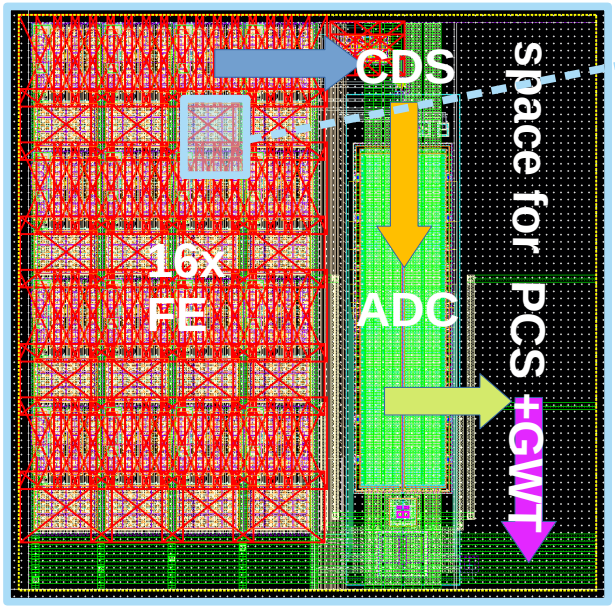
BONN DESY.

… made of smaller puzzle pieces

CoRDIA ASIC





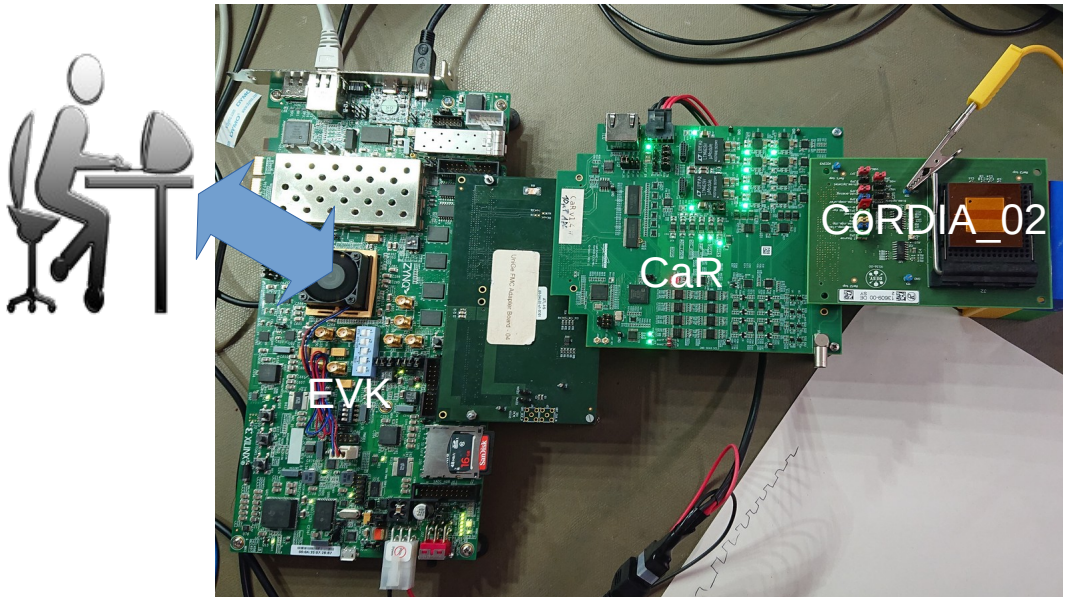


effort to design analog blocks in a standard-cell fashion for ease of placement and reuse and compatibility to existing cells (e.g. fillers)

BONN DESY.

do they fit together?

CoRDIA ASIC

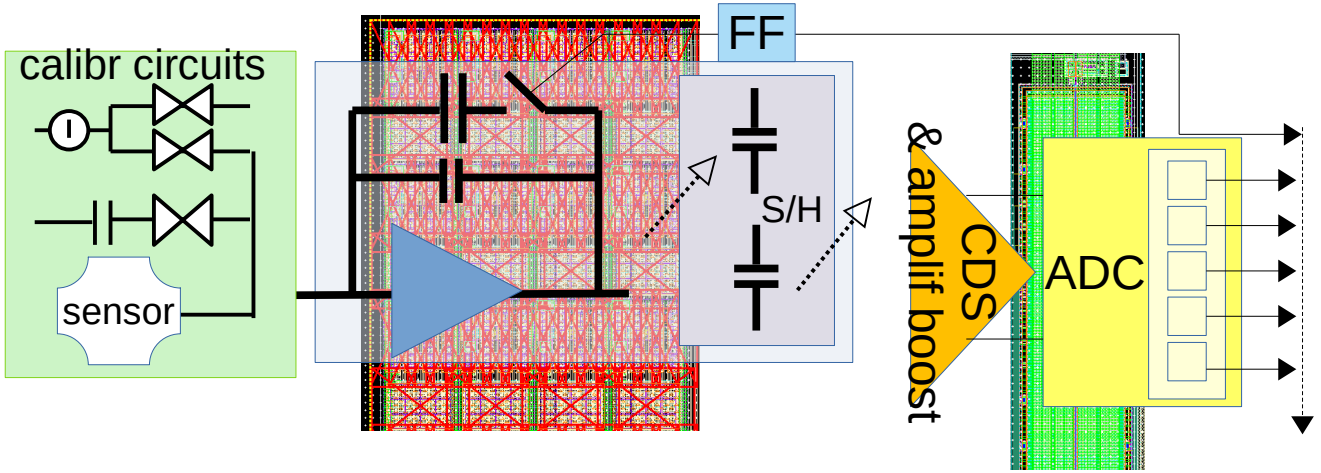


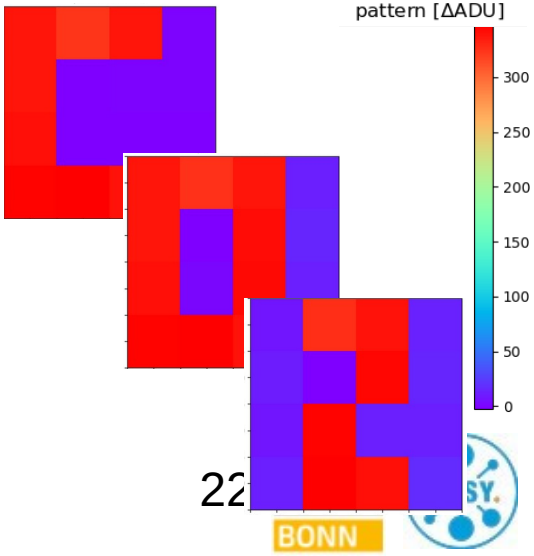
test using Caribou setup

versatile testbox system,
providing cntrl, bias & DAQ

see: T. Vanat et al.
PoS TWEPP2019 (2020) 100

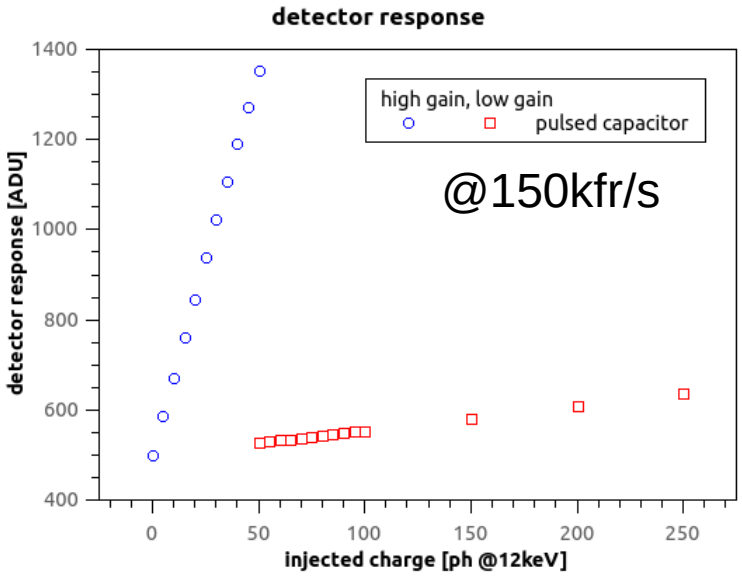
charge injection in selected pixels using calibration circuits (pulsed-C, Isource)
image acquisition @ operational speed (150kfr/s)
slow readout @ 40MHz (no GWT, 1 superpix. rather than 128)

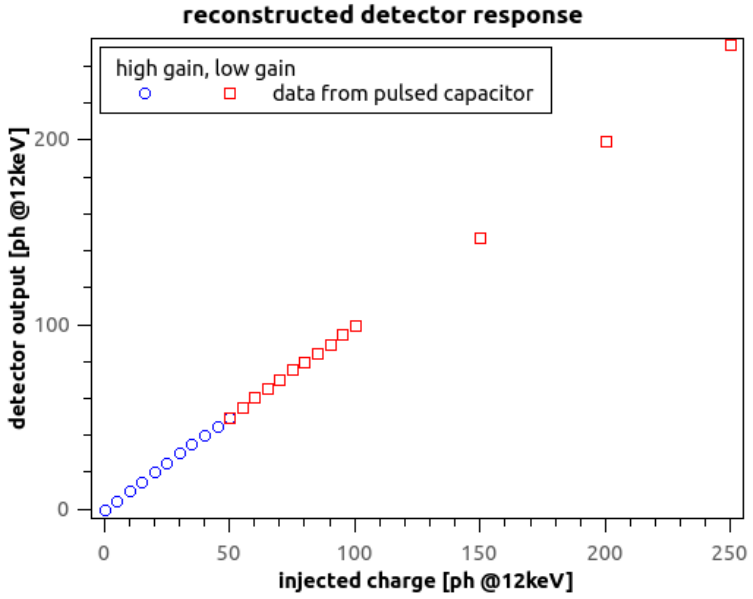


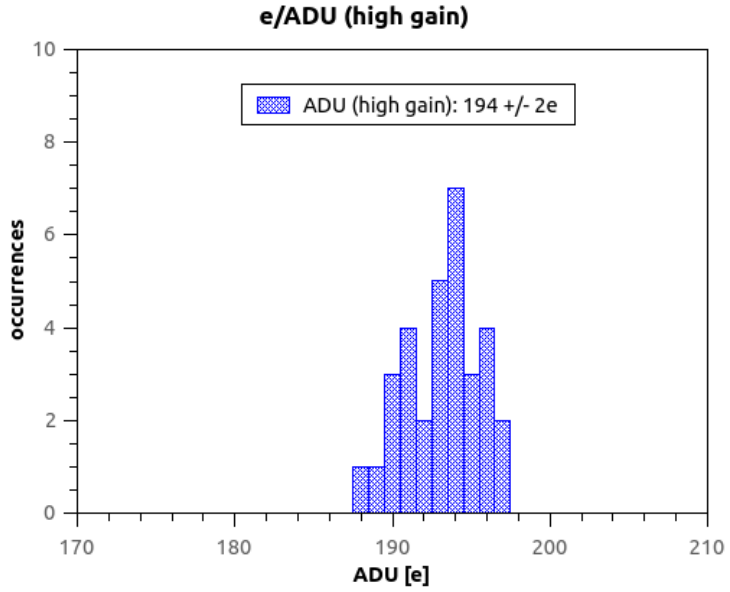


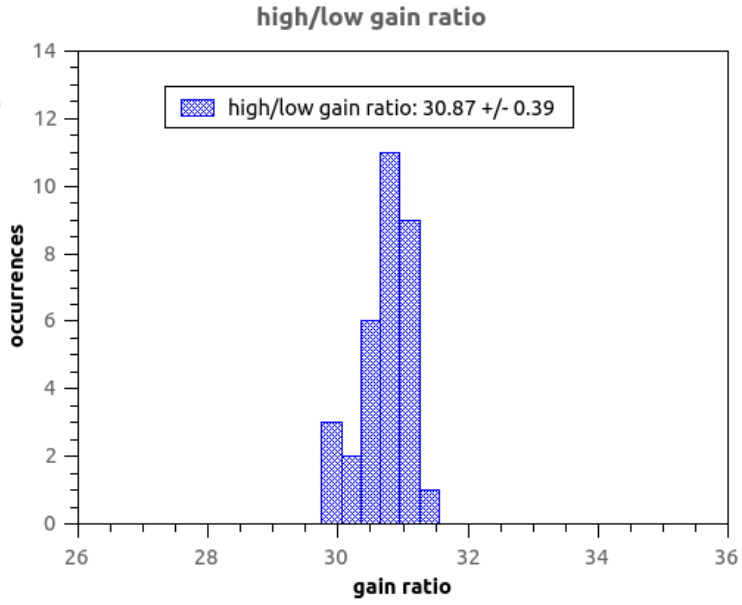
pulsed-C → Ad-Gn reconstruction, e/ADU est.

CoRDIA ASIC



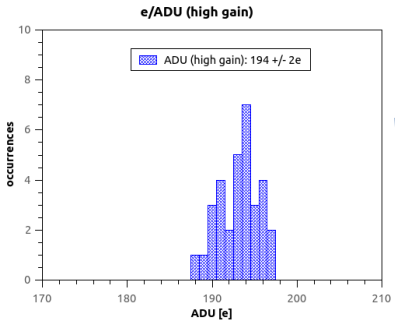


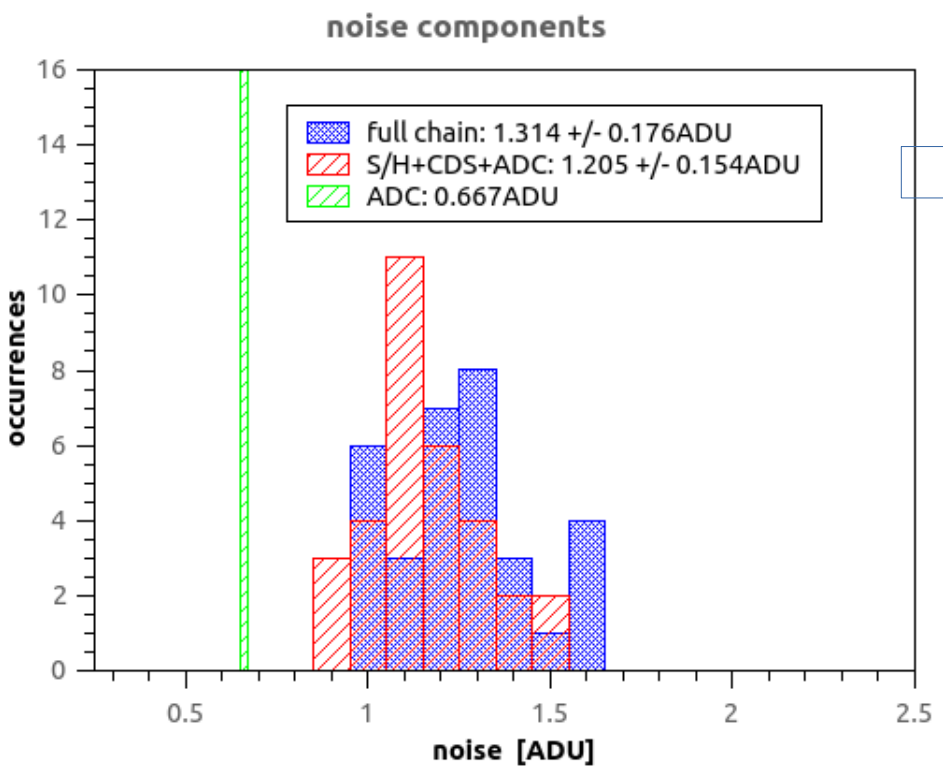


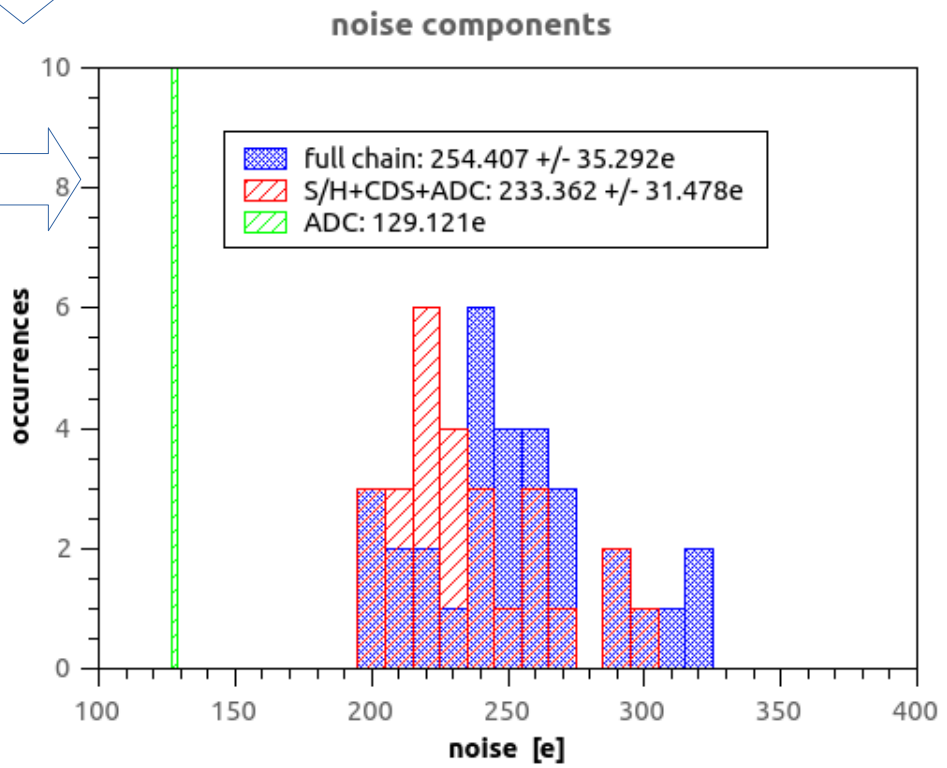


dark noise estimation

CoRDIA ASIC



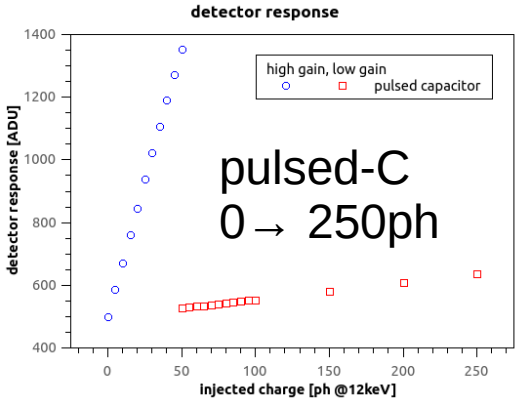


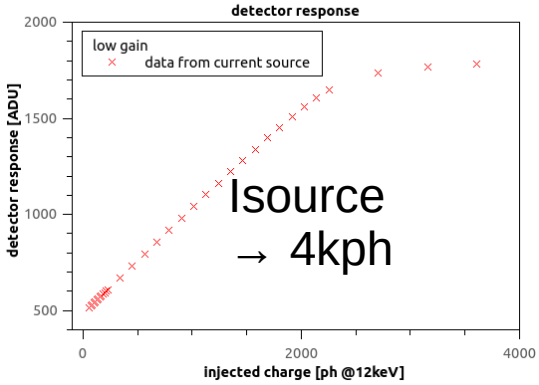


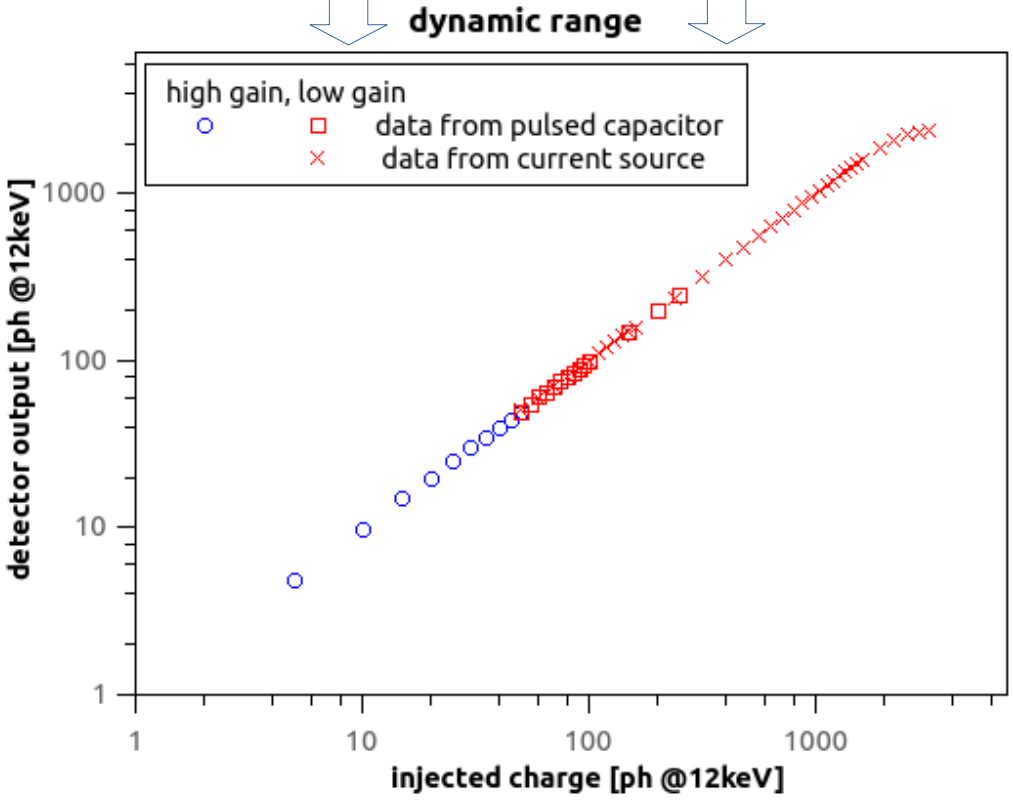
BONN DESY

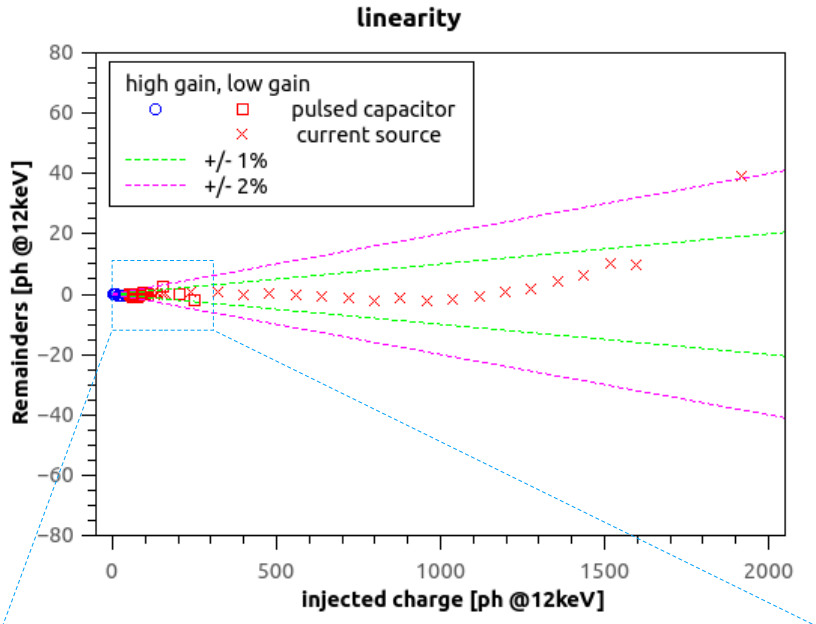
dynamic range estimation

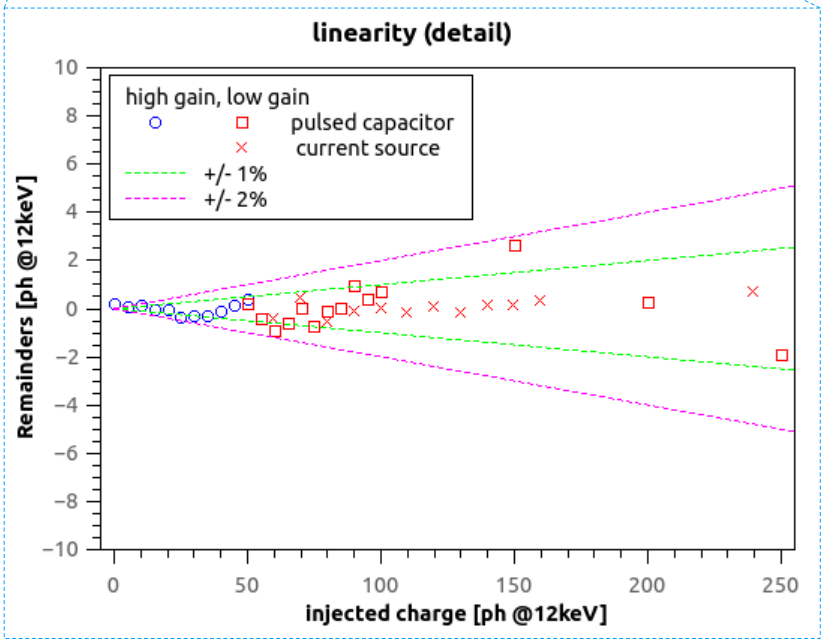
CoRDIA ASIC





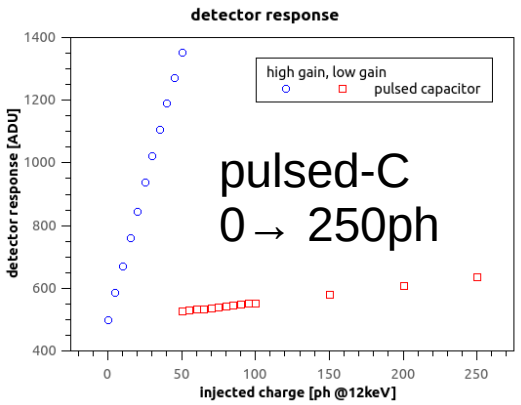




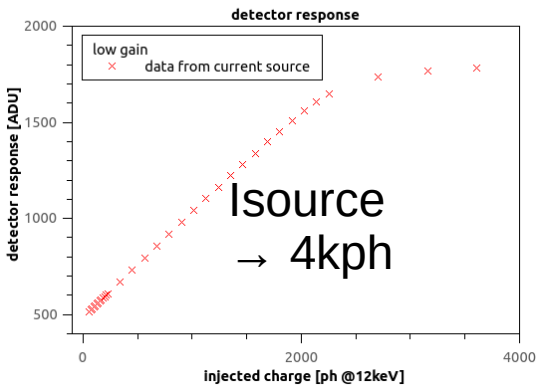


noise vs. poisson

CoRDIA ASIC

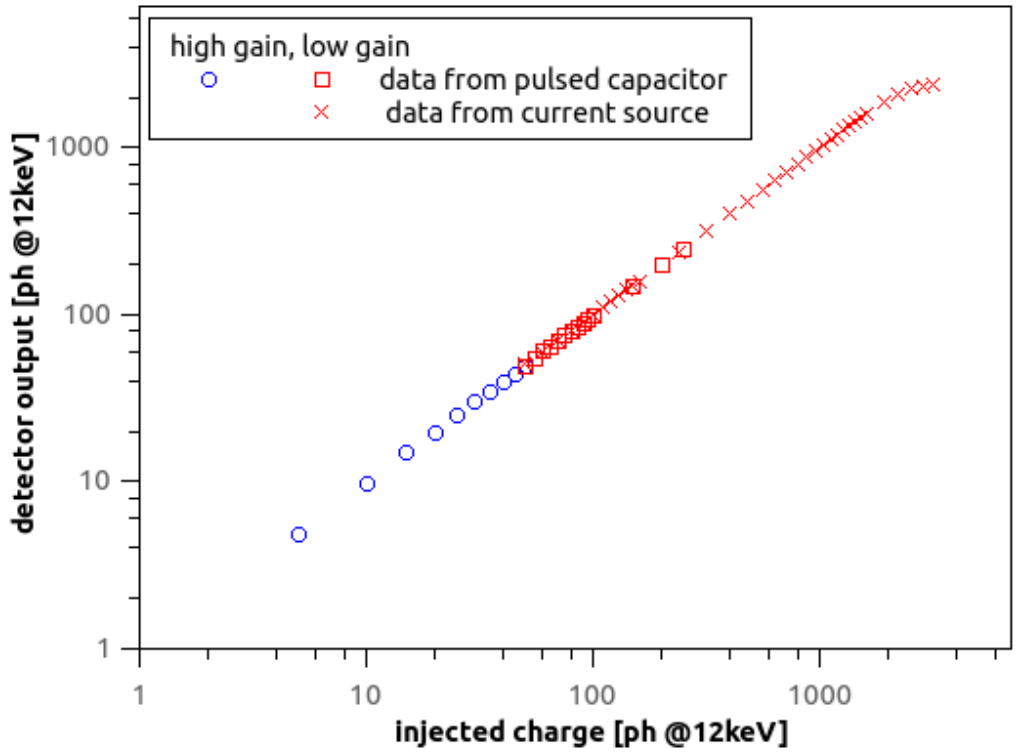


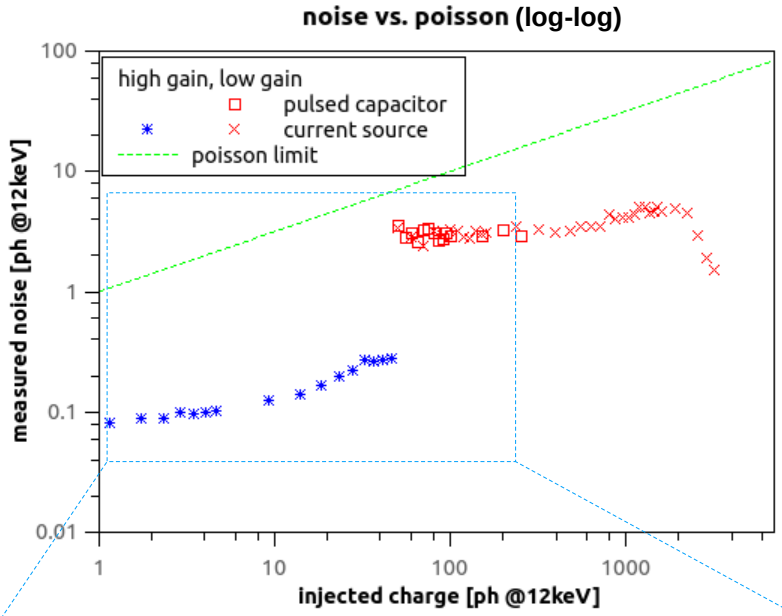
pulsed-C
0→ 250ph

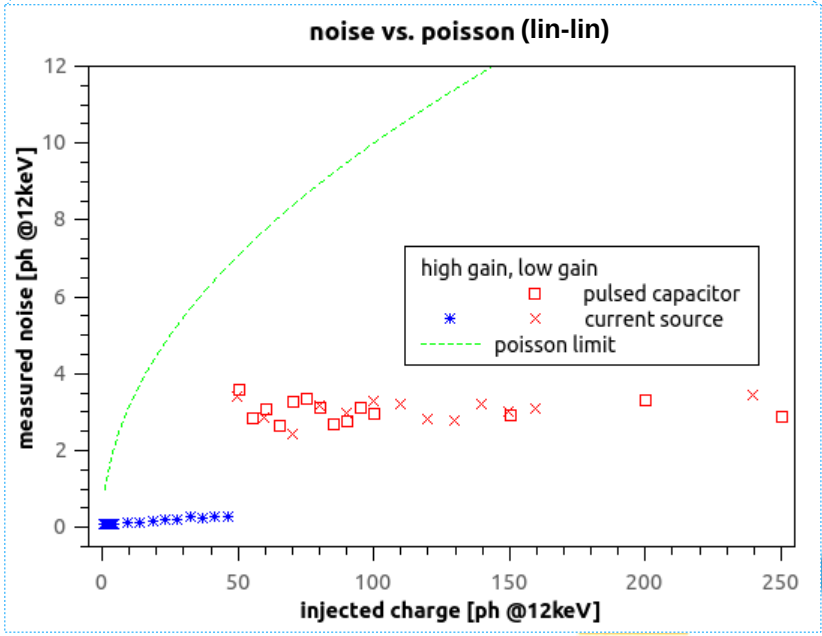


Isource
→ 4kph

dynamic range

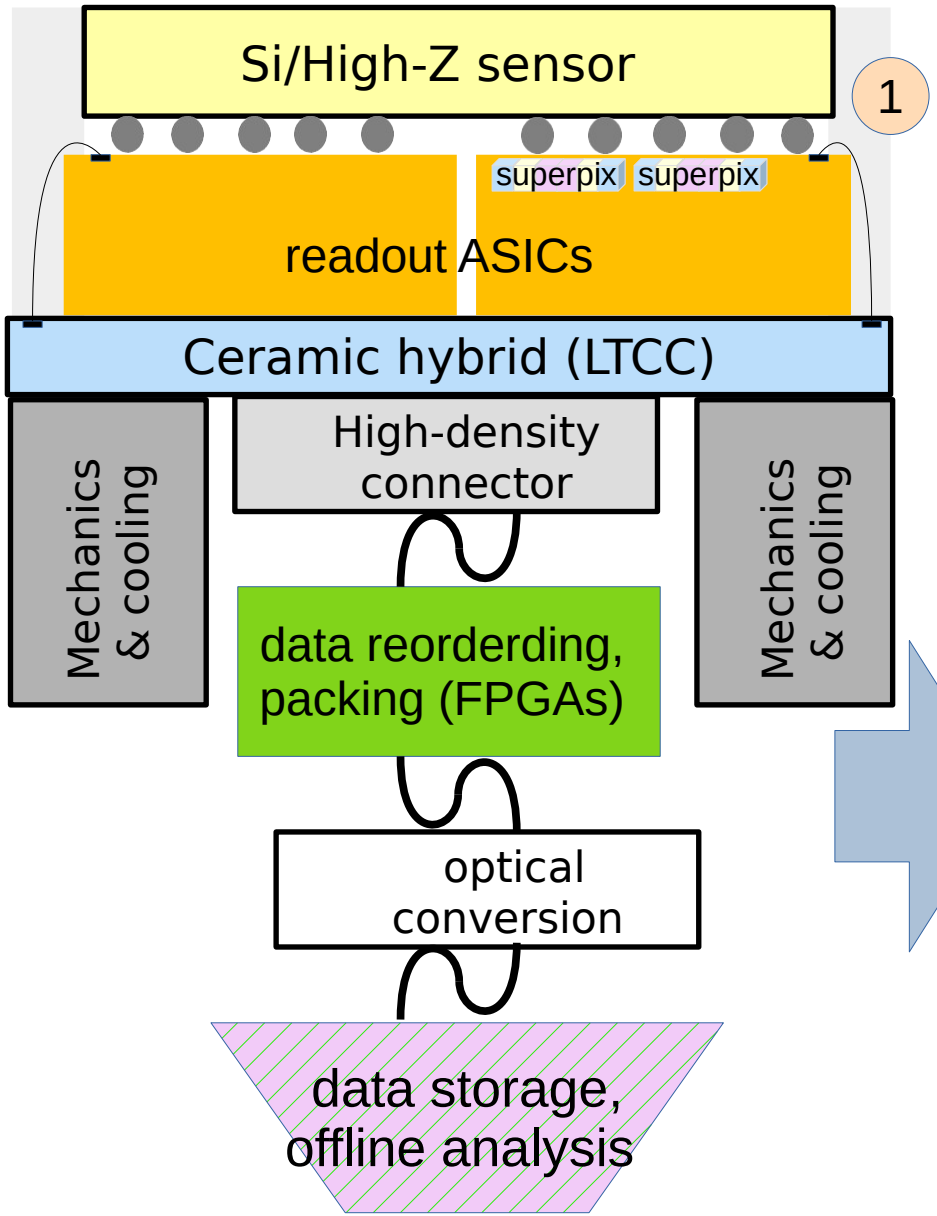


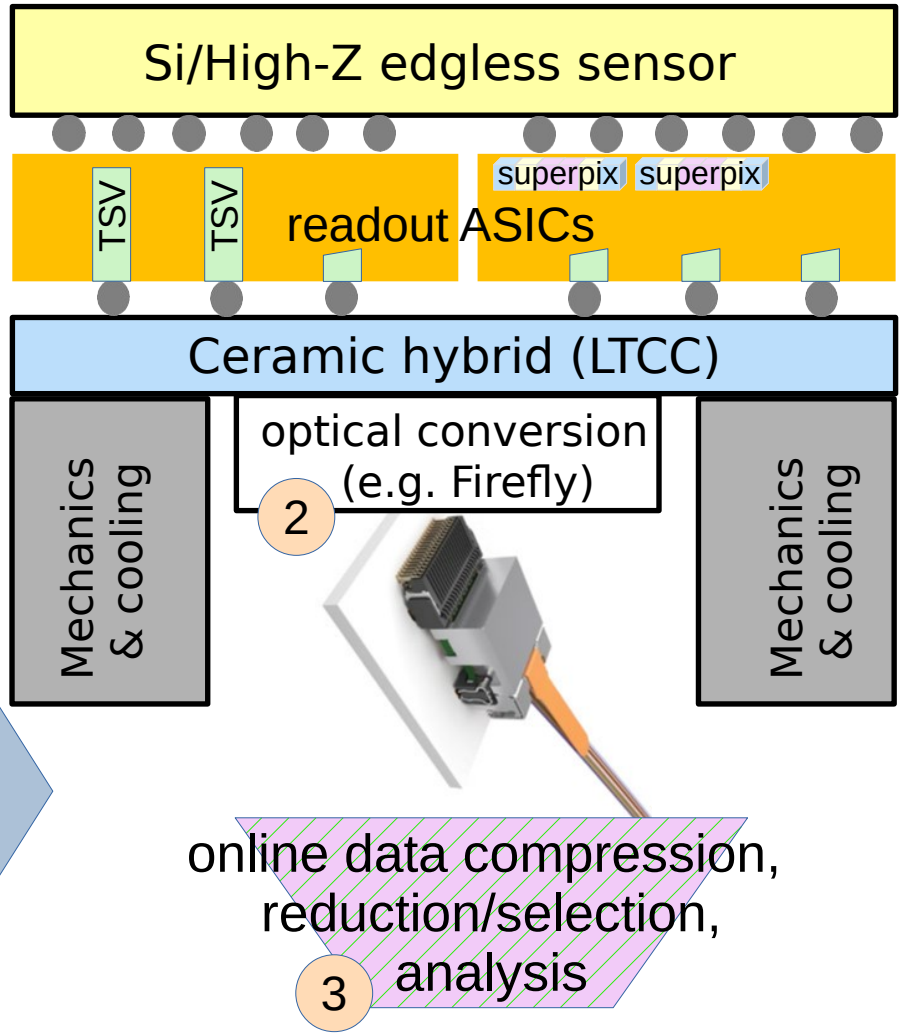




a glimpse of the bigger picture

CoRDIA





but beware of the ...

CoRDIA

DatApocalypse

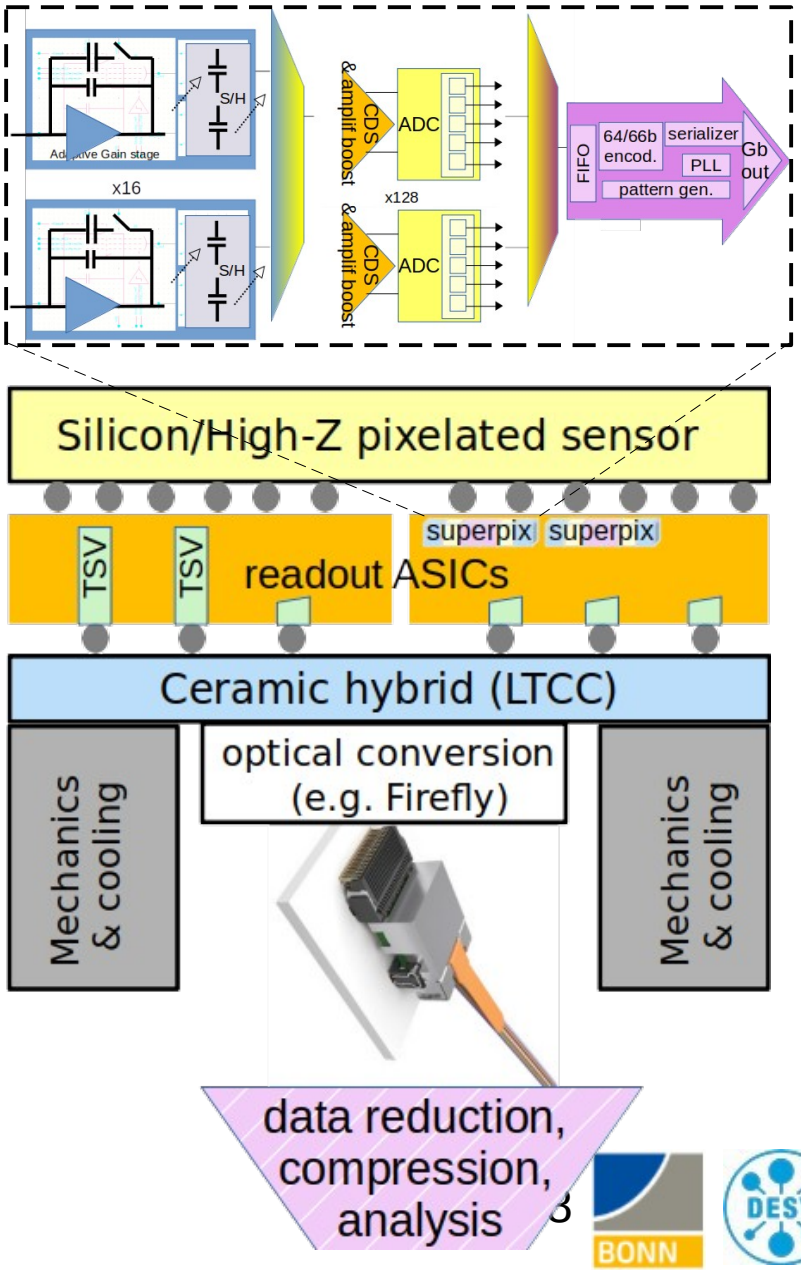
Even when used at reduced speed, produces a considerable data output:

1Mpix (min. size palatable by users)
x 12bit/pix (min discr. 11bit ADC + Gn)
x 133kframe/s (PetraIV bunch rate)
x 66/64 (encoding for GWT)

> 200GBytes/s (>1.6Tb/s)

addressed on silicon:
pipelined architecture, on-chip ADCs, high-speed drivers

out-of-Silicon: considering Xilinx Alveo acceleration cards

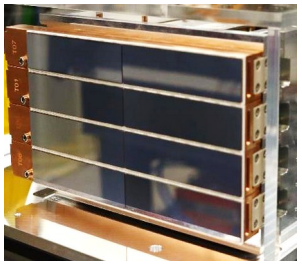


Data reduction

CoRDIA

- Goal – use accelerator cards with built-in network links to receive, buffer and process detector data
  - Experimented with Xilinx Alveo FPGA card with 2x100 GBE
  - Compared performance for bad image rejection between CPU, GPU and FPGA

Detector module e.g. CoRDIA

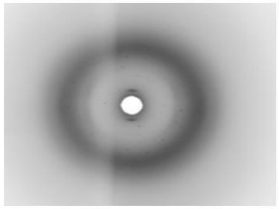


Detector PC layer with accelerator cards

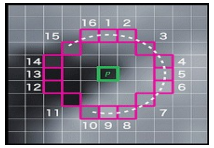
Facility central computing and storage

- Developed machine-learning-based methods for rejecting bad images in serial crystallography
  - E.g. extracting features from images with computer vision techniques, then classifying with neural network (MLP)

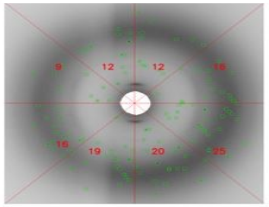
Input image



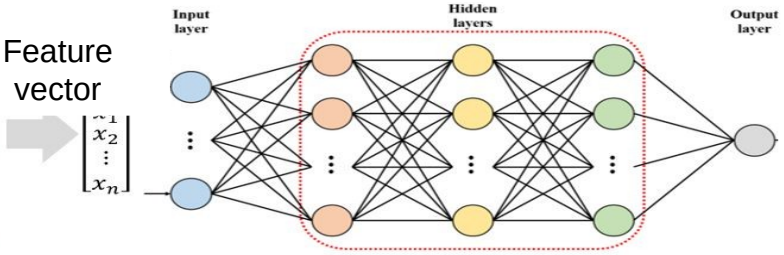
Keypoint finding



Feature extraction



Fully-connected NN



multilayer perceptron, a feedforward artificial neural network

BONN DESY

CoRDIA in a nutshell

CoRDIA ASIC

Ph source upgrades

need for imagers:
> 100kHz frame rate
continuous readout

goal

- 150 kHz, continuous
- 110 µm pixel size
- 1-photon sensitive 12 keV
- charge integr. (FEL-compatible)
- a-few-k ph/pix/img
- e-collect. (compatible w. HiZ)

approach

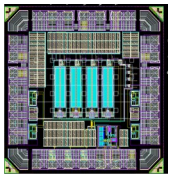
Adapt.-Gn FE → ADCs 11b SAR → T.pix4 GWT devel. Nikhef

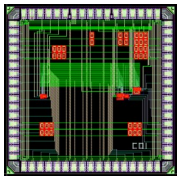
integrate charge → digitize → encode & RO

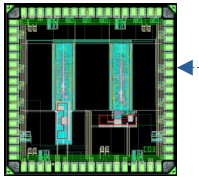
integrate charge → digitize → encode & RO

pipelinelined architecture

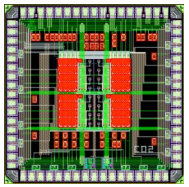
analog FE, ADC, GWT as blocks

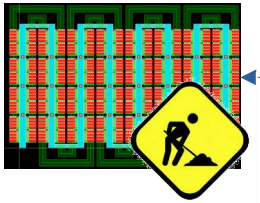






superpixel, small array





timeline

validation of individual circuit blocks → validation of circuit chain as a pixel array → validation as a component of the overall detector system

validation by MPWs (TSMC65)

performance improvement study ← expansion to full-scale ASIC → 1st gen ASIC

by start of Petra IV (~2030) will target pixel pitch, CWR, 150KHz

performance improved ASIC → 2nd gen ASIC

extend dyn rng, min. blind areas

BONN DESY.