IFDEPS 2024 – March 17-20

Detector development activities : X-ray detector family for LCLS-II

Dionisio Doering, Angelo Dragone

*on behalf of SLAC X-ray Detector R&D Program

SLAC NATIONAL ACCELERATOR LABORATORY

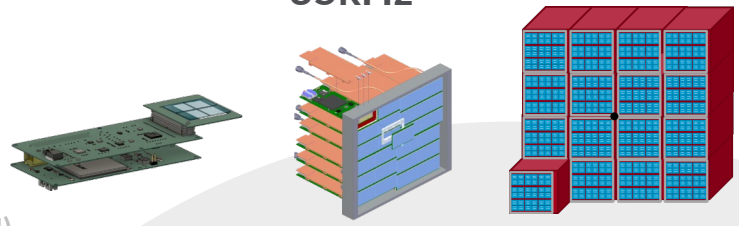
Stanford University | U.S. DEPARTMENT OF ENERGY

SLAC X-ray detectors families

Bigger, Faster, Higher resolution and Higher Energies

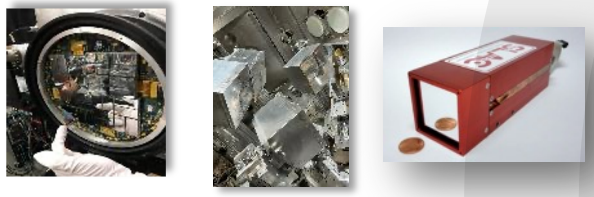
With goals built into projects progressively meeting science priorities and requirements

ePixUHR$_{35kHz}$ (2019-2027)



ePixHR$_{5kHz}$ (2016-2024)

ePix (2013-2018)



ePixUHR (2019-2029)

- Full frame 100kHz-1MHz

SparkPix (2020-2027)

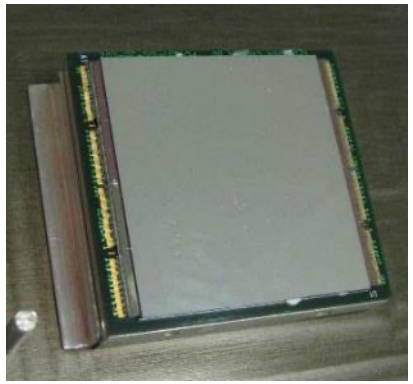
- In addition
- SparkPix-T, RT,…

ePixHR Detector Concept

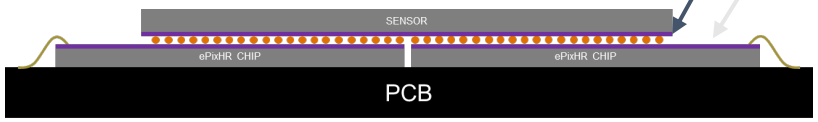
Standard modular hybrid approach (same as ePix)

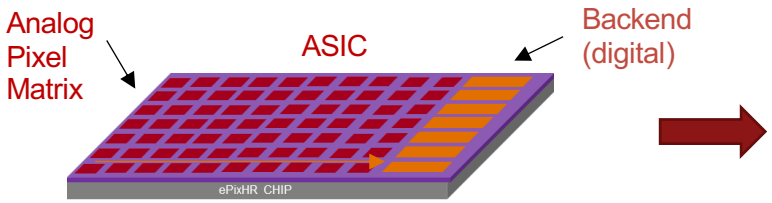
Core module architecture 5kHz version:

Sensor-ASIC assembly



Sensor-ASIC assembly cross-section





Fully depleted Si Sensor (or HiZ)

- Same Si or Thick –Si sensors used for ePix10k (demonstrated)

Standard micro-bumps

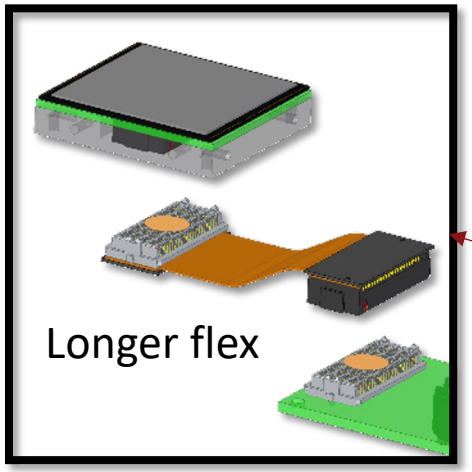
Readout ASIC (ePixHR)

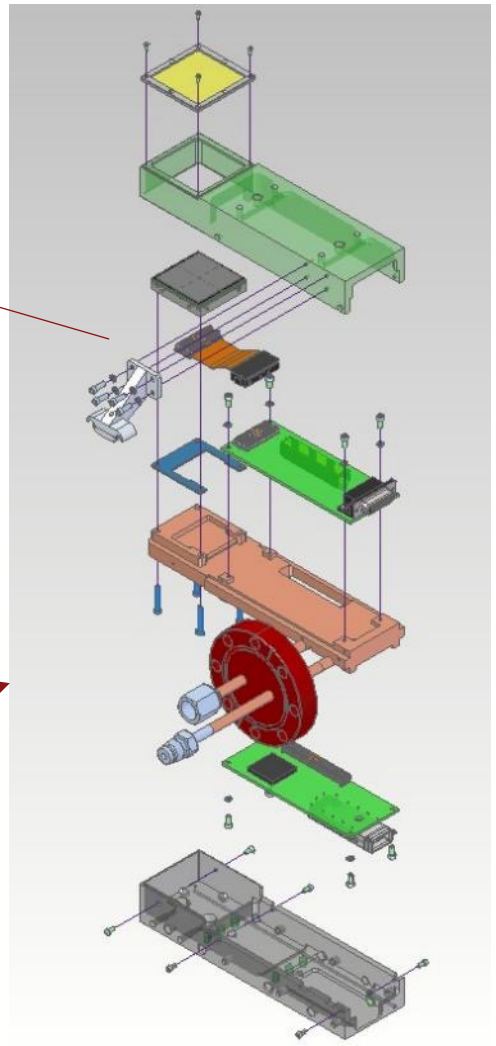
- Variant of ePix10k
  - 4th prototype @5kHz (ASIC standalone demonstrated 2023)
  - Science grade module are in fabrication
  - ASIC compatible with Hi-Z sensors (inverted polarity also available)

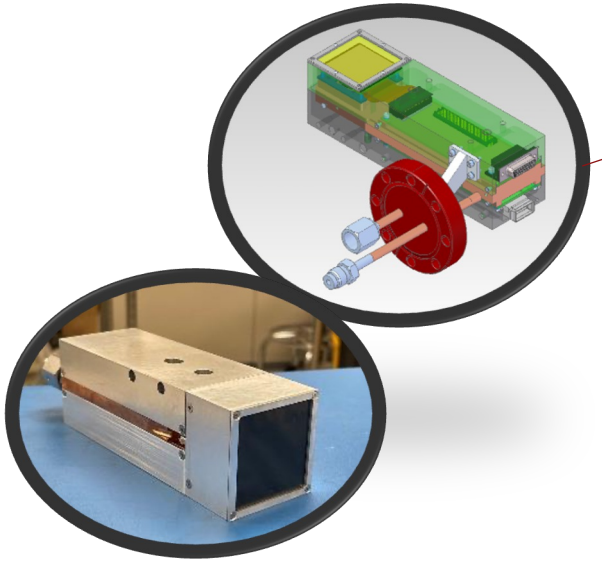
	ePix	ePixHR
Type of backend	Analog	Digital
Architecture	Analog Mux	1MSPS ADC/column + Digital Mux
Rate	1kHz	5kHz

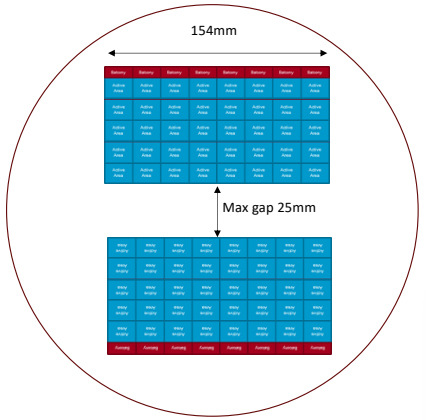
Detector development aiming LCLS-II TXI beamline

- 140kPix front or side entrance and 2Mpix variants

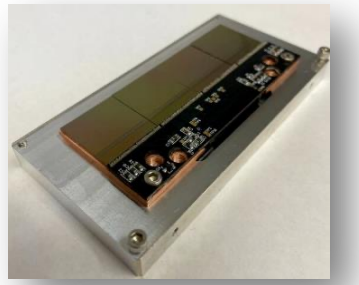


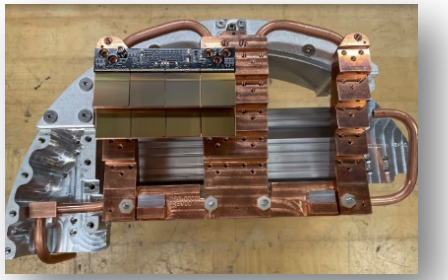


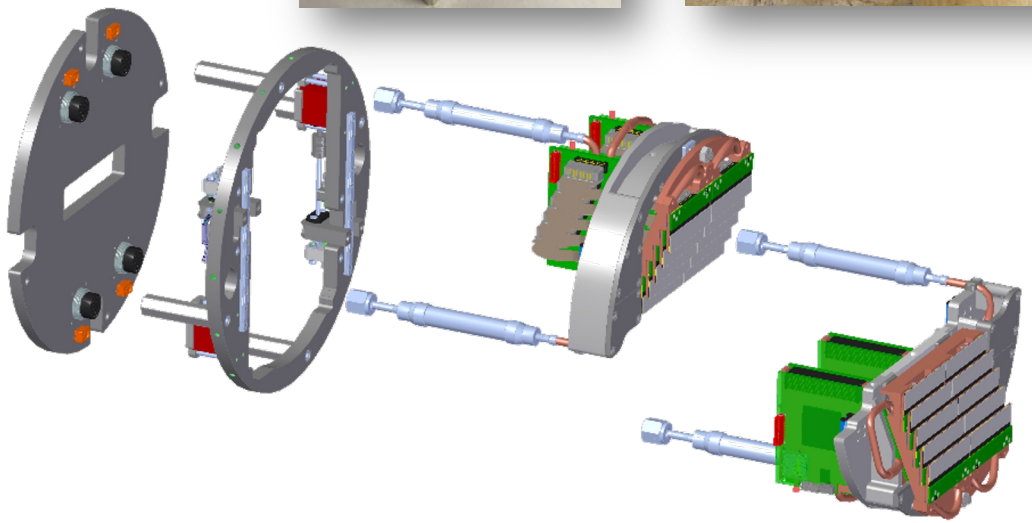




144*192 pixels * 4 ASICs = 110kpix

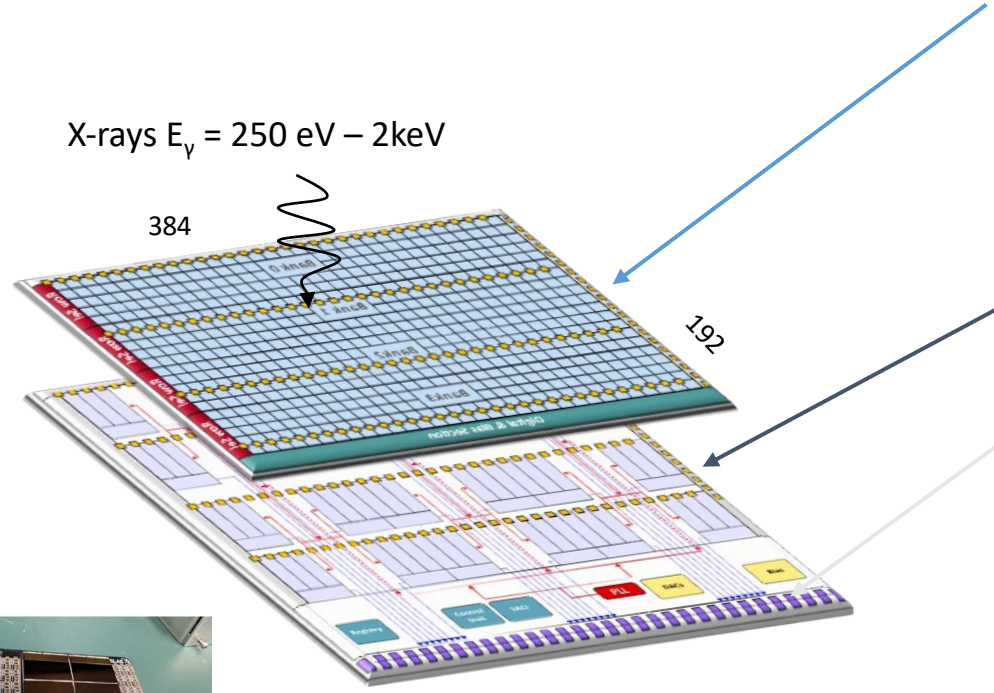


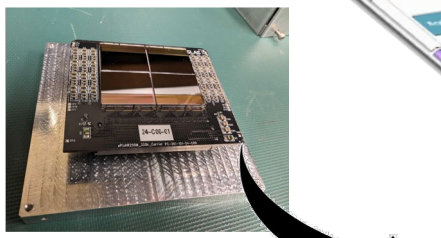


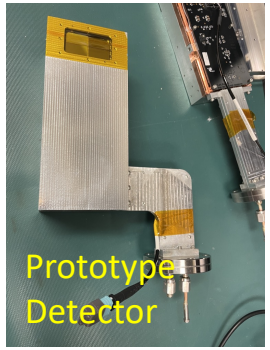


Detector Concept

Standard modular hybrid approach







ePixM
90 degree
at qRIXS
model

ePixM Monolithic Active Pixel Sensor (MAPS)

- On-sensors amplifier reduces noise → **demonstrated**
- Fully-depleted and back-illuminated → **demonstrated**
- Entrance window optimized for soft X-rays → **demonstrated**

Standard micro-bumps

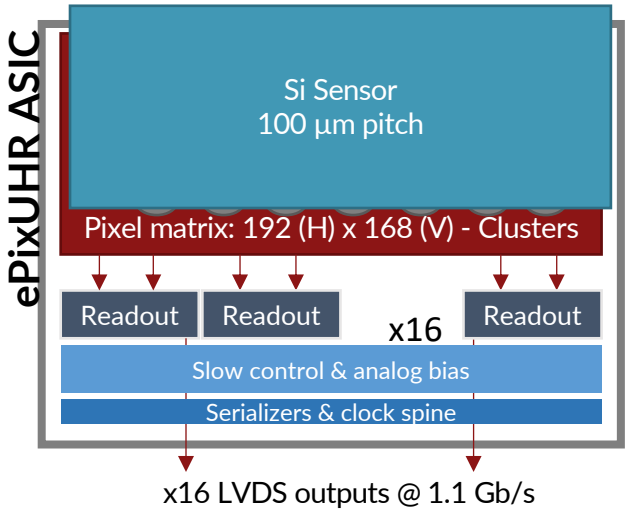
ePixHR-M Readout ASIC (ROIC)

- 4 arrays of 192 ADCs
- Each array is a copy of the ePixHR back-end → **demonstrated**

Parameter	Threshold	Objective	0.3 Mpix ePixM
Pixel pitch [um]	50	50	50
Read noise [e^- rms]	15	10	12
Well depth [Number of 530eV photons]	1000	3000	>1000
Quantum efficiency [%, 275eV-1500eV]	70	90	~84
Frame-rate [kHz]	5	10	7.5

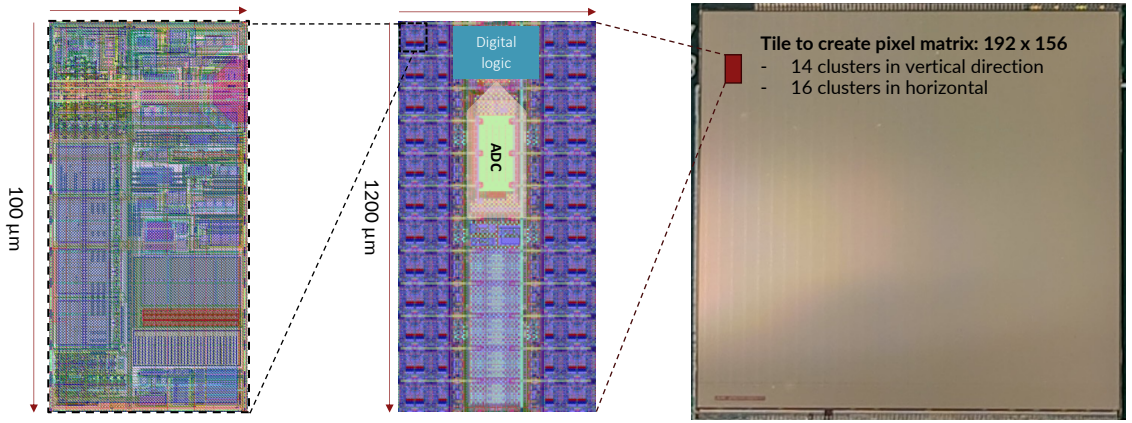
ASIC Architecture

- **Full frame 35kHz for HE first light**
- Sensors for hard X-rays
- 4MPix detector design for HE



Detector	ePixUHR	
Mode	35 kHz	100 kHz
Pixel Pitch [um]	100	
Frame rate [kHz]	35	100
Matrix size	192 x 168	
Read Noise [e^- rms]	100	
Well depth [4keV photons]	10^4	
Power consumption [W/cm^2]	1.2	
Data rate [Gb/s]	16	44
CMOS tech node	TSMC 130 nm	

Demonstrated 1st prototype Goal 2nd prototype



Pixel

- Operates at 35 kHz – 1 MHz
- Si sensor: 100x100 µm^2
- ASIC: 50x100 µm^2

Cluster

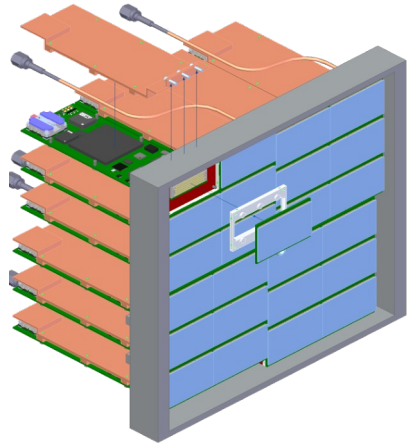
- 72 pixels → 1 ADC @ 8 MSPS
- Digital logic for pixel configuration and readout

ASIC

- 72 pixels → 1 ADC @ 8 MSPS
- Digital logic for pixel configuration and readout

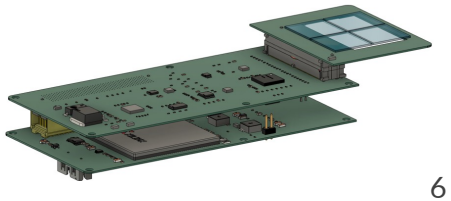
Data

- Pixel matrix test-pattern obtained at a clock frequency of 35 kfps



4MPix ePixUHR 35kfps

130kPix ePixUHR 35kfps

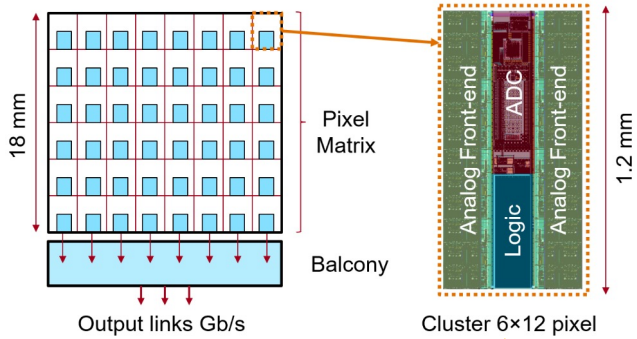


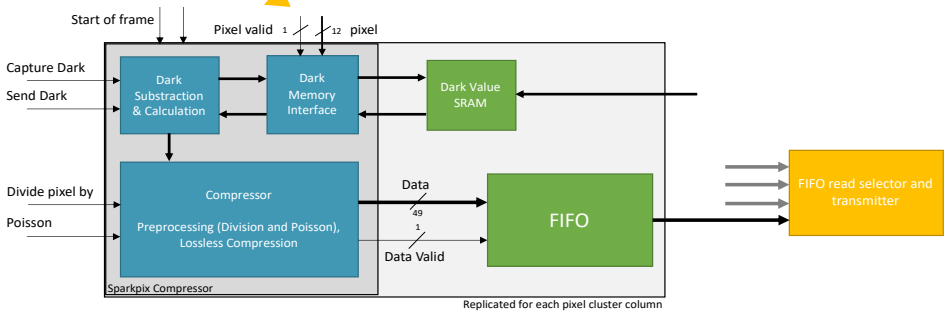
SparkPix-{RT, SR}

SparkPix-RT detector taken as reference for initial prototype specifications:

- Compression algorithm
  - Expand edge processing to the ASIC
  - Implemented in the balcony
  - Reduce data-rates

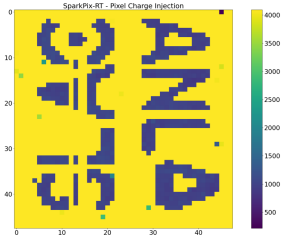
Goals of this R&D:
Solve data transmission bottleneck by finding compression algorithm solutions therefore expanding edge computing into the ASIC





SparkPix-SR (Super Resolution):

- Future development
  - Mega Hz frame rate operation
  - 25□m pixel pitch
  - Charge sharing enables sub-pixel position information extraction
  - Real time energy and position processing
  - Sparse data readout
  - BCDI and XPCS types of experiments

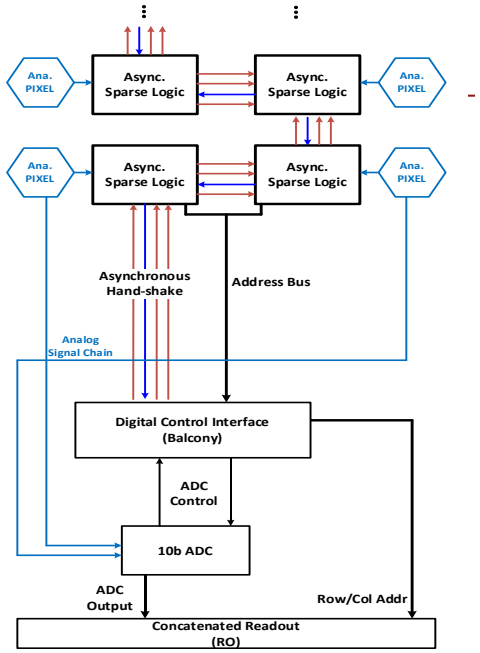


SparkPix-{S, T}

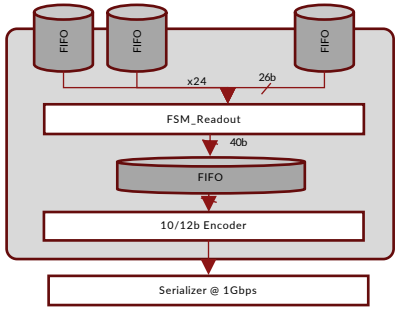
***See Lorenzo's talk on Beyond ePixUHR 100,000 fps: on-chip data reduction with the Sparkpix detector family**

- **SparkPix-S**
  - Implemented sparsification in the analog domain
  - In-pixel discriminator with local threshold
  - ADC is shared among a cluster of pixels and digitizes only pixels containing a "hit"
  - Power & area efficient
  - Digital readout builds on SparkPix-T

Pixel (50x50um²)

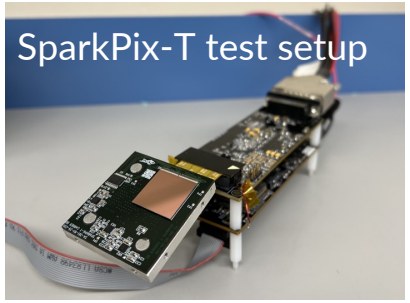


Sparse digital readout (every 24 columns): can be tailored to different ASICs

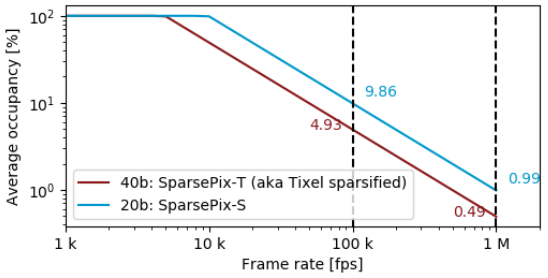


Two levels of FIFOs act as local buffers, allowing for higher "single-hit" occupancy without losing information.

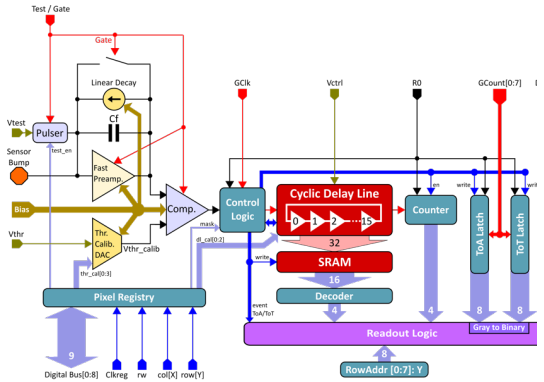
- **SparkPix-T**
  - Time of Arrival (+ ToT)
  - 100 ps time resolution
  - 6.5□s time depth
  - 100□m pixel pitch
  - 49MHits/s/cm²



Simulated avg occupancy/frame



Pixel (100x100um²)



SNL's Role In The DRP

SNL/ML Inference at the sensor (eFPGA / in memory compute)

x5 ASICs carriers

ASIC
ASIC
ASIC
ASIC

ASIC
ASIC
ASIC
ASIC

⋮

ASIC
ASIC
ASIC
ASIC

8.5Gbps/carrier

SNL/ML Inference on the detector (readout FPGA)

FPGA

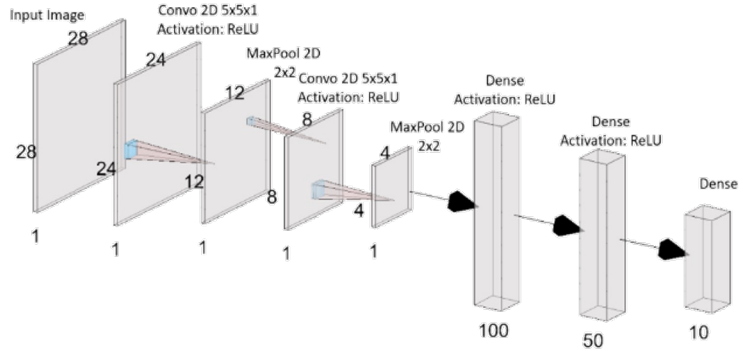
Image Proc. algorithms

Commercial Co-Processors

SNL/ML as a resource to DRP. Larger networks and full images. (Commercial coprocessors are best deployed here)

- As the SNL/ML deployment gets farther from the sensor, the compute resources increase but so do the network sizes.
- Commercial solutions become more viable
- Closer to the sensor allows for smaller networks and earlier data reduction.

SNL/ML Inference at the boundary to the DRP



DRP

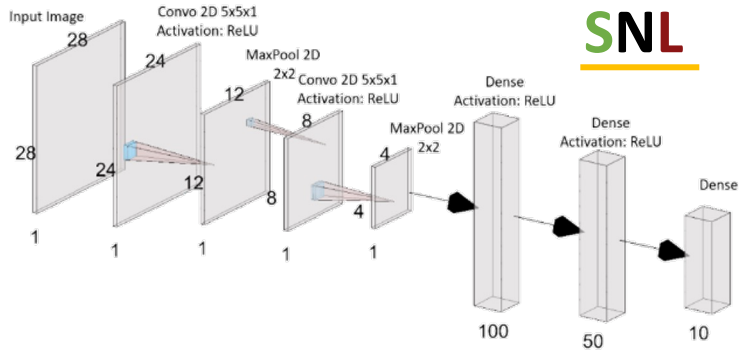
***See Jana's talk on LCLS-II Online Processing, Data Reduction, and Future Opportunities in Data Science**

SLAC X-ray detectors families

***See Conny's talk on Commissioning and Operational detector experience at LCLS**

Bigger, Faster, Higher resolution and Higher Energies

With goals built into projects progressively meeting science priorities and requirements



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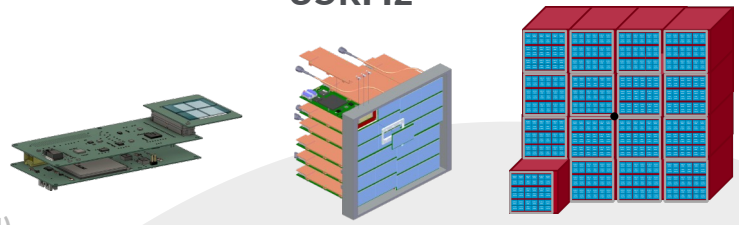

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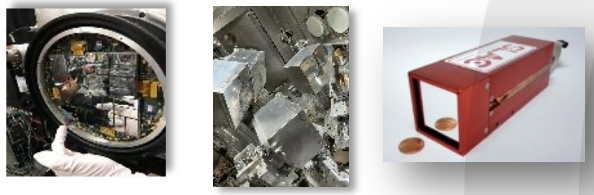
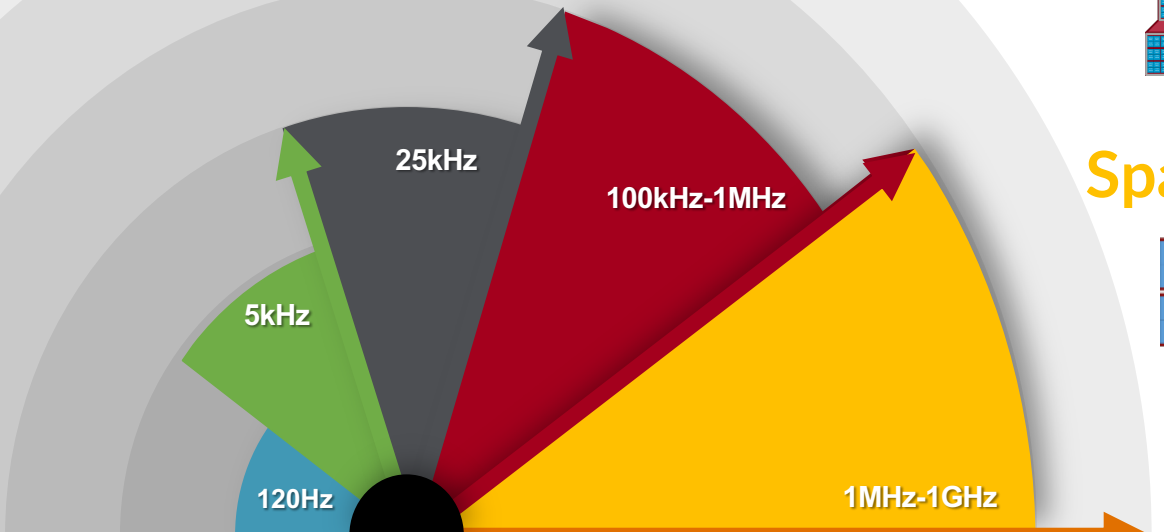
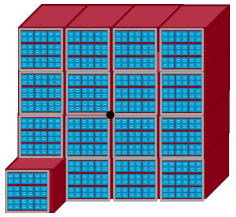


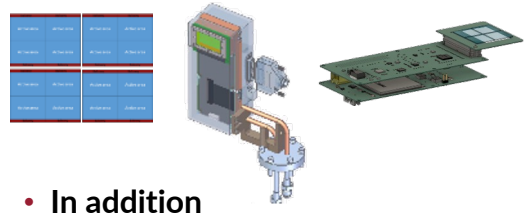


ePixUHR (2019-2029)

- **Full frame 100kHz-1MHz**



SparkPix (2020-2027)



- **In addition**
- **SparkPix-T, S, RT, SR, ED,…**