XIDyn

A high dynamic range and timing resolution hard X-ray detector for 4th generation synchrotrons

Matt Wilson (STFC)

On behalf of the XIDyn Collaboration

IFDEPS 2024

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Content

- Motivations to Requirements
- Challenge and Choices
- DynamiX and XIDer
- XIDyn ASIC
- XIDyn demonstrator
- Summary

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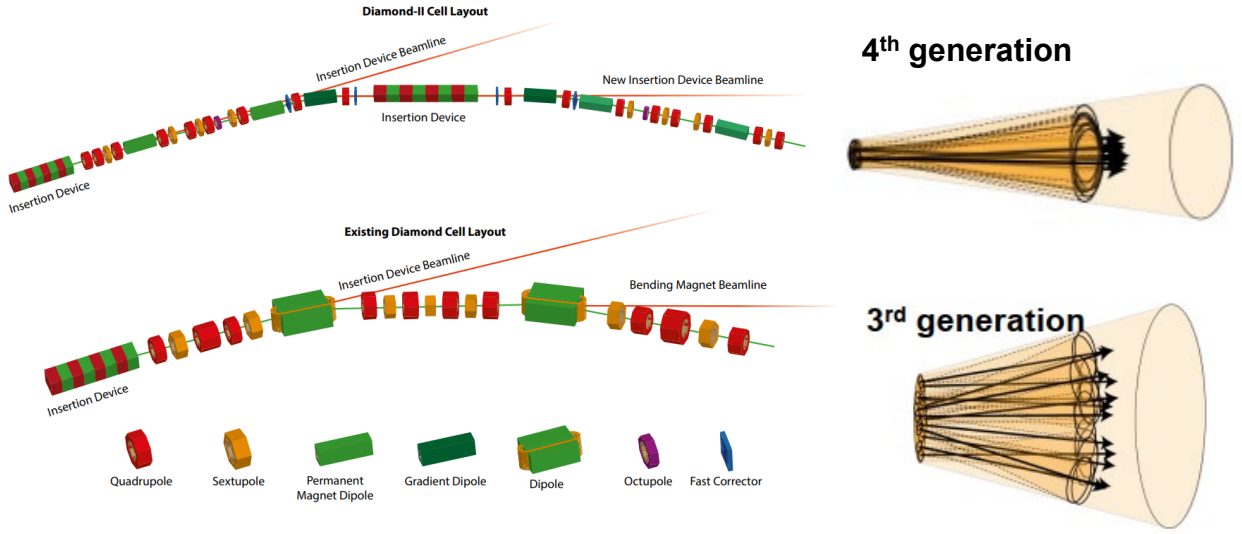
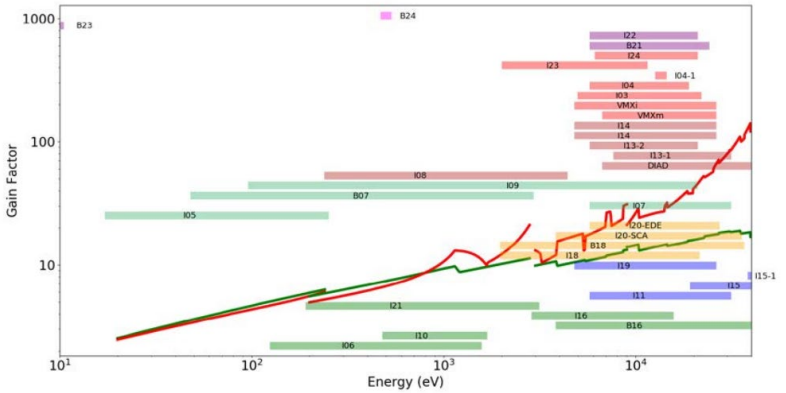
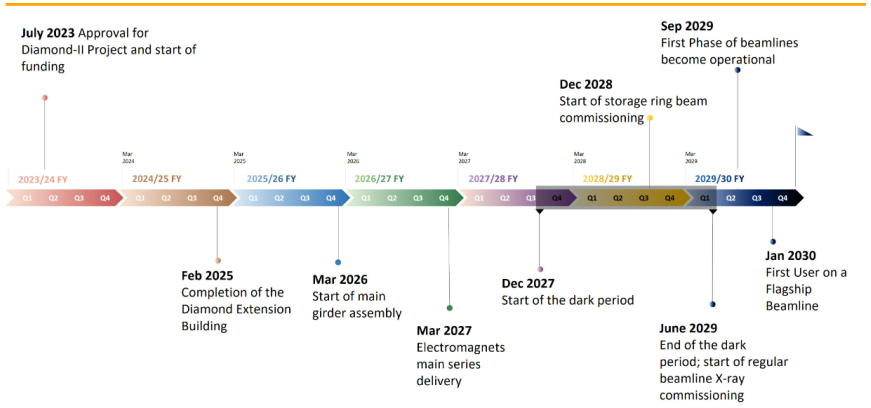
Credit: https://www.diamond.ac.uk/Diamond-II.html

Motivation

- Diamond II upgrade
- Up to 10^{12} ph/mm^2/s
- Many beamlines >20keV
- Mpixels for 2029
- ~100µm pixels
- ~100kHz rate







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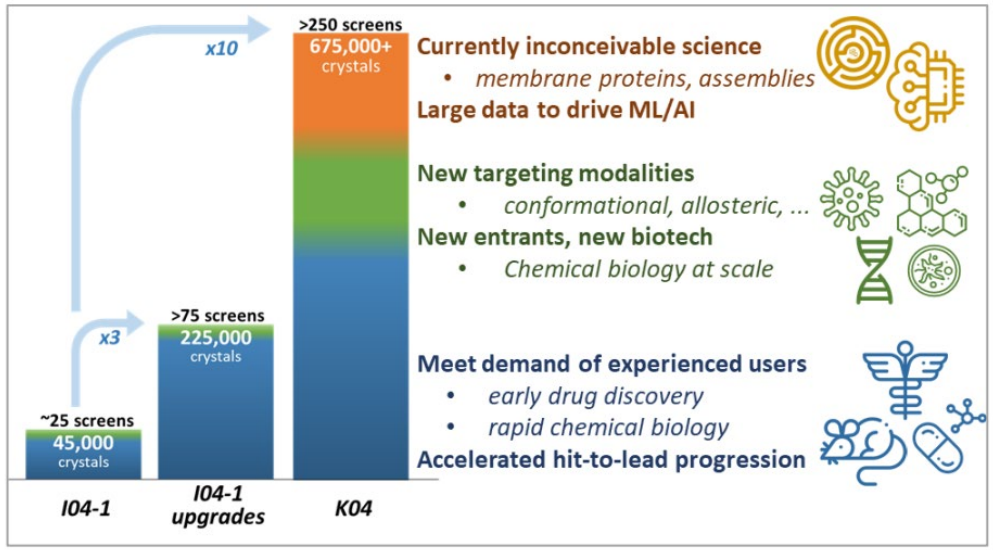
Motivation



- K04 Ultra-XChem
- Serial MX for drug discovery
- 25keV increase diffraction yield relative to radiation decay
- Higher flux for weakly diffracting, inhomogeneous crystals – membrane proteins and large complexes

Credit: https://diamond.ac.uk/Diamond-II/beamline-updates/flagship-beamlines/K04.html

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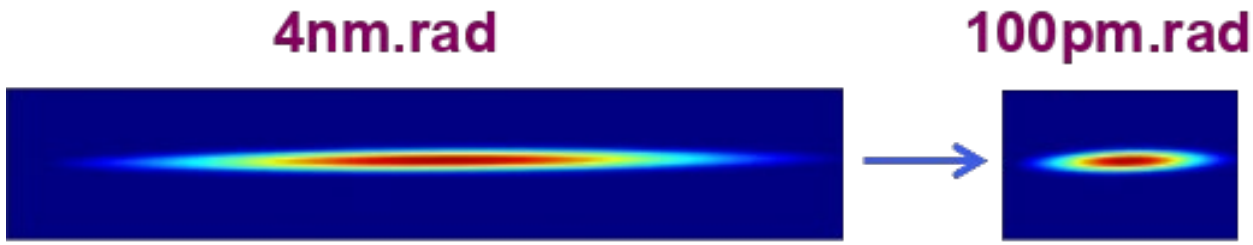
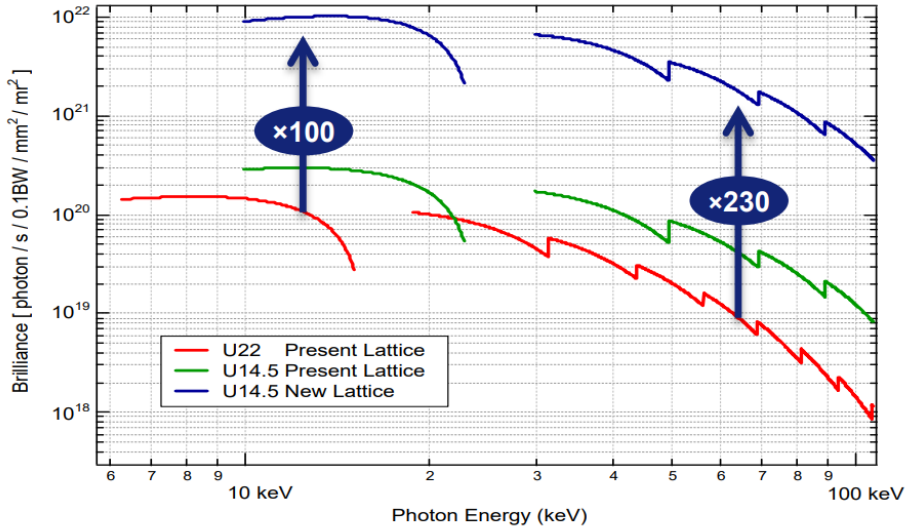
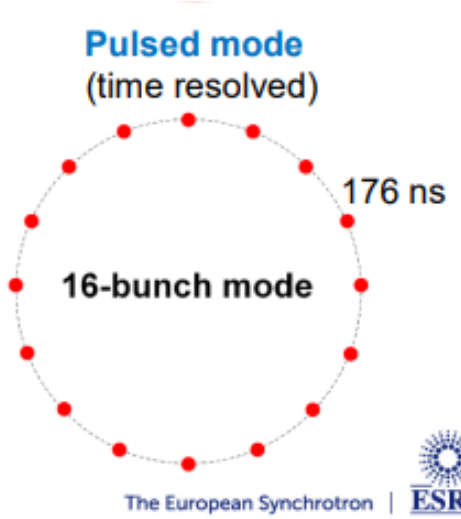
Motivation

- ESRF-EBS
- 30-100keV
- >>10^9 ph/mm^2/s
- 10-100s kHz
- Sufficient flux for time resolved with 16-bunch mode

A. Ropert, J.M. Filhol, P. Elleaume, L. Farvacque, L. Hardy, J. Jacob, U. Weinrich, **"Towards the Ultimate Storage Ring-Based Light Source"**, Proc. EPAC 2000, Vienna.







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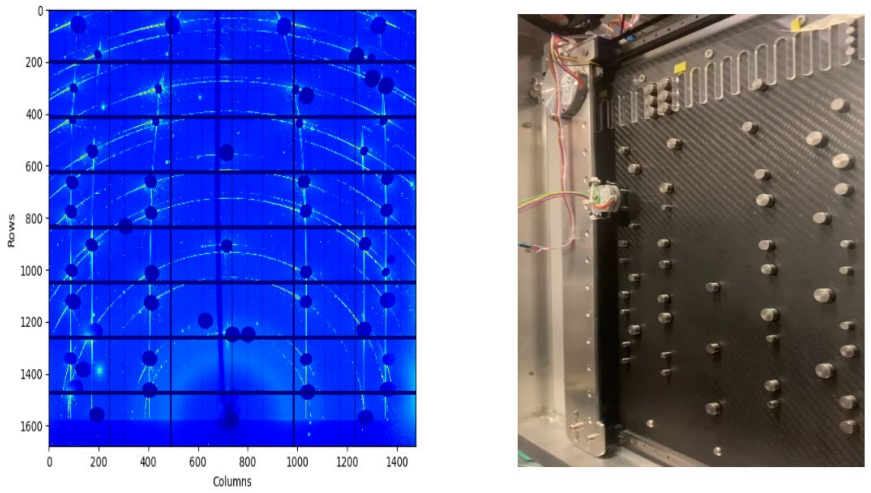
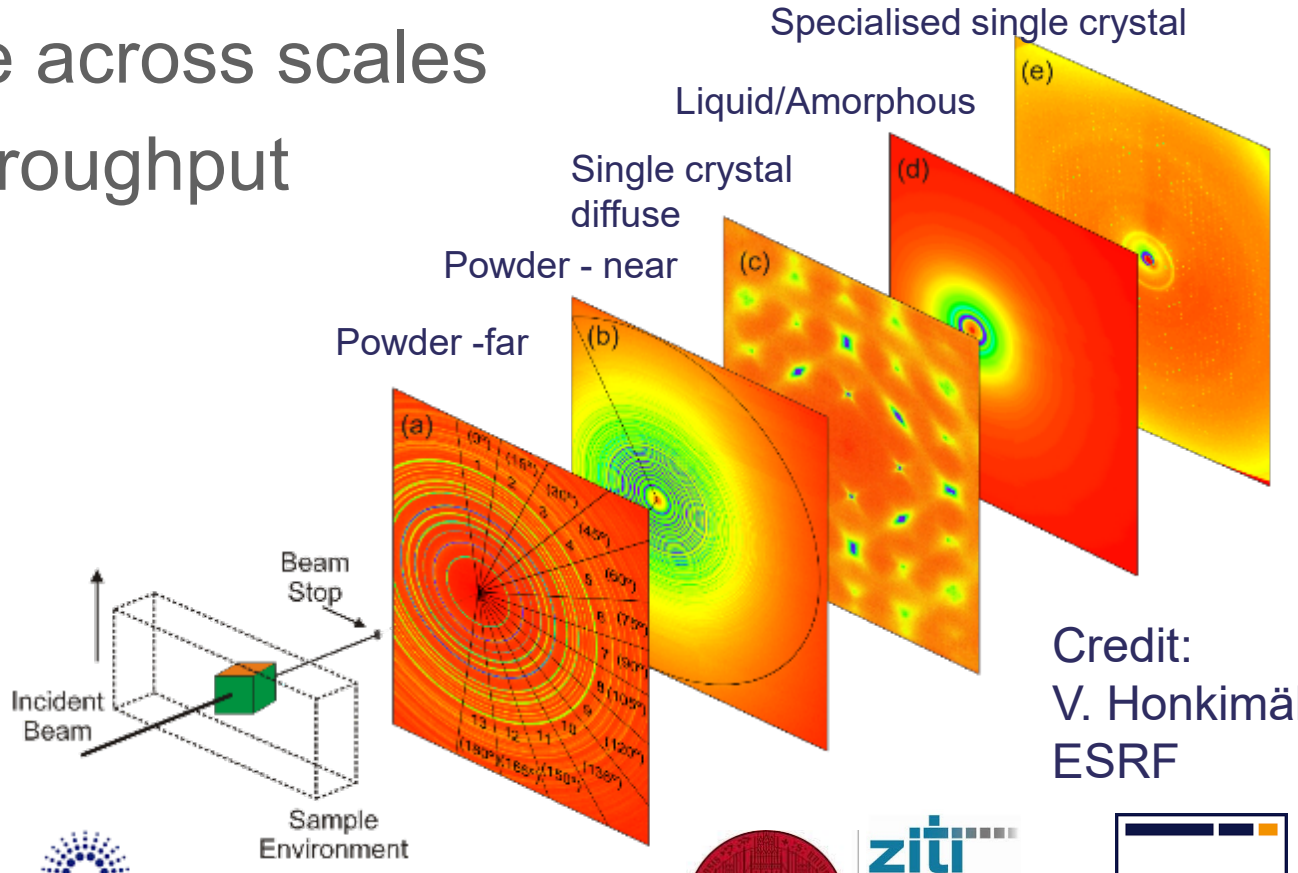
Motivation

- Example of material science across scales
- Current detectors limiting throughput



Current detector with magnetic beam stops



Credit:
V. Honkimäki
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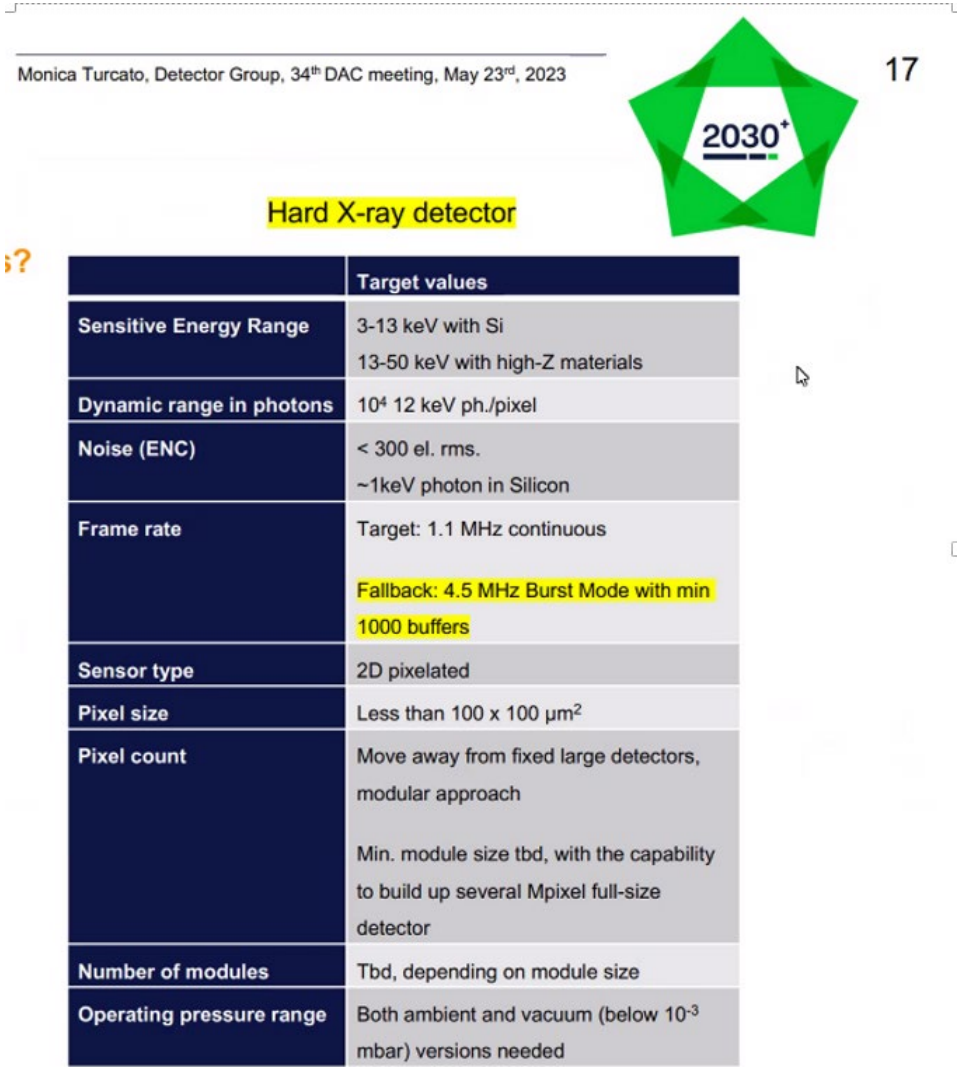
EuXFEL

Version 1.0 of XIDyn won't get to EuXFEL 2030 specification

- High energy
- Pixel size ~100µm
- ~10^2 not 10^4 pulsed
- 4.5MHz burst for 100s not 1000s
- Continuous at 100s kHz not MHz



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Requirements

Parameter	Continuous	Burst Timing
Operation	Constant with tolerable deadtimes	256 Frame capture and slower readout
Energy Range [keV]	25keV typical	30-100keV
Resolution [photon]	0.25-1	1
Flux [ph/mm^2/s]	~10^{12}	~10^{11}
Pixel Size [µm]	~100	~100
Frame Rate [kHz]	~10-100	5700 for 16 bunch mode
Instantaneous Flux [photons]	~100	~200
Power [W/cm^2]	5	

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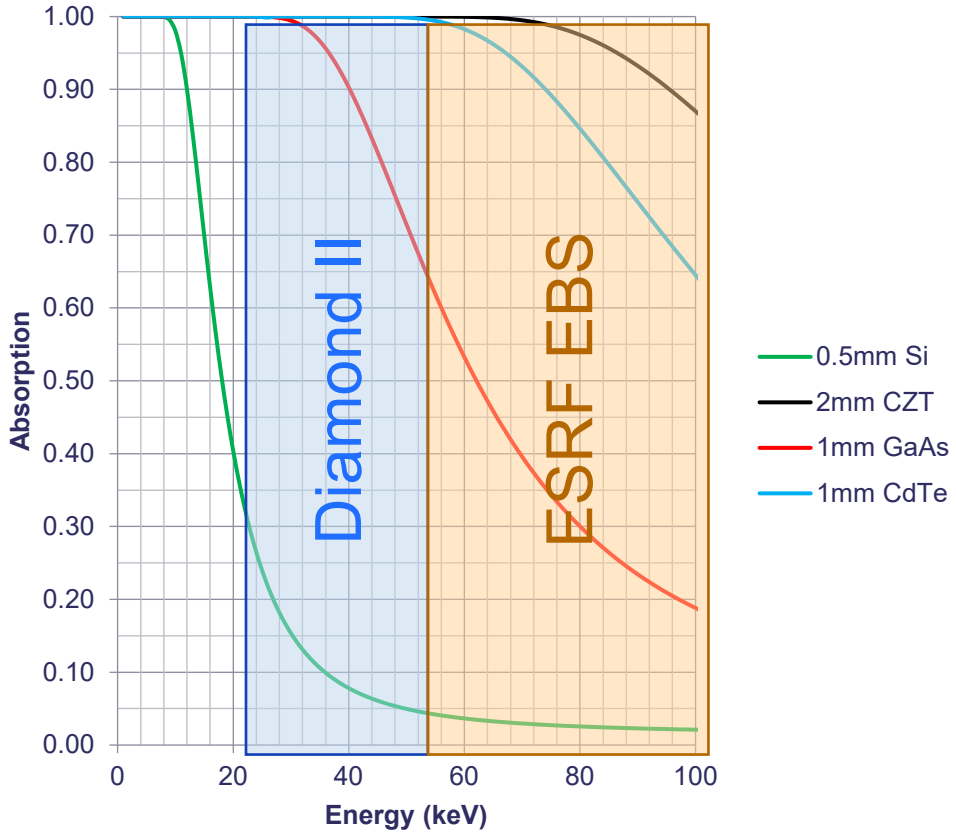
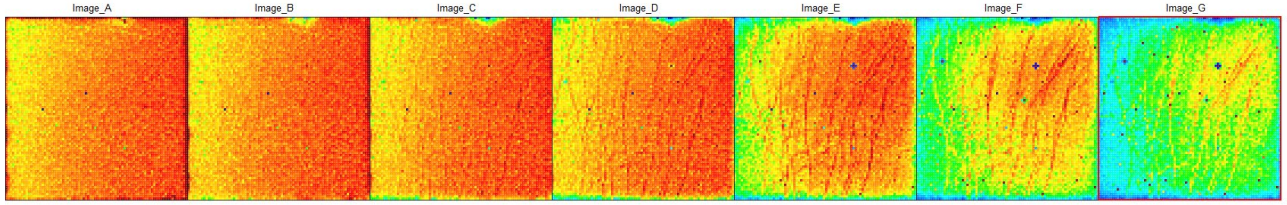
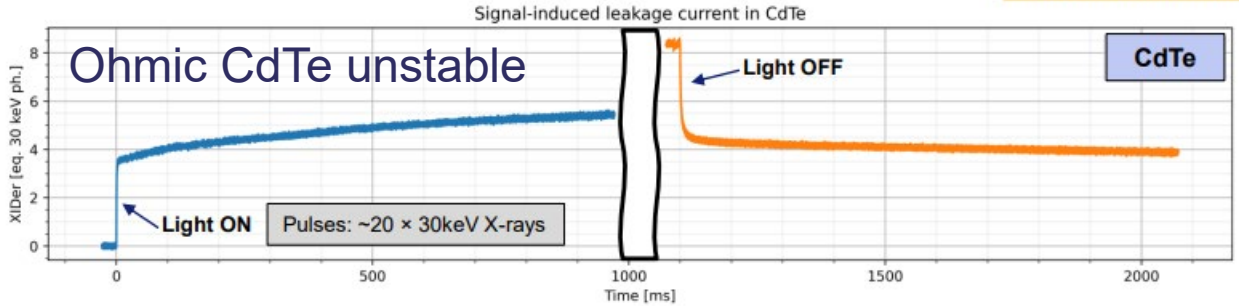
Energy Challenge

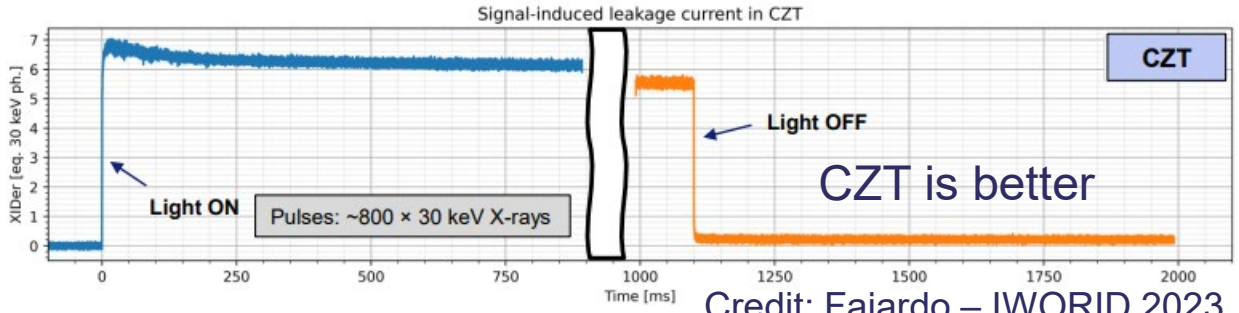


Schottky CdTe polarises with time and very unstable under high flux



ON/OFF interval: 5 minutes





Credit: Fajardo – IWORID 2023

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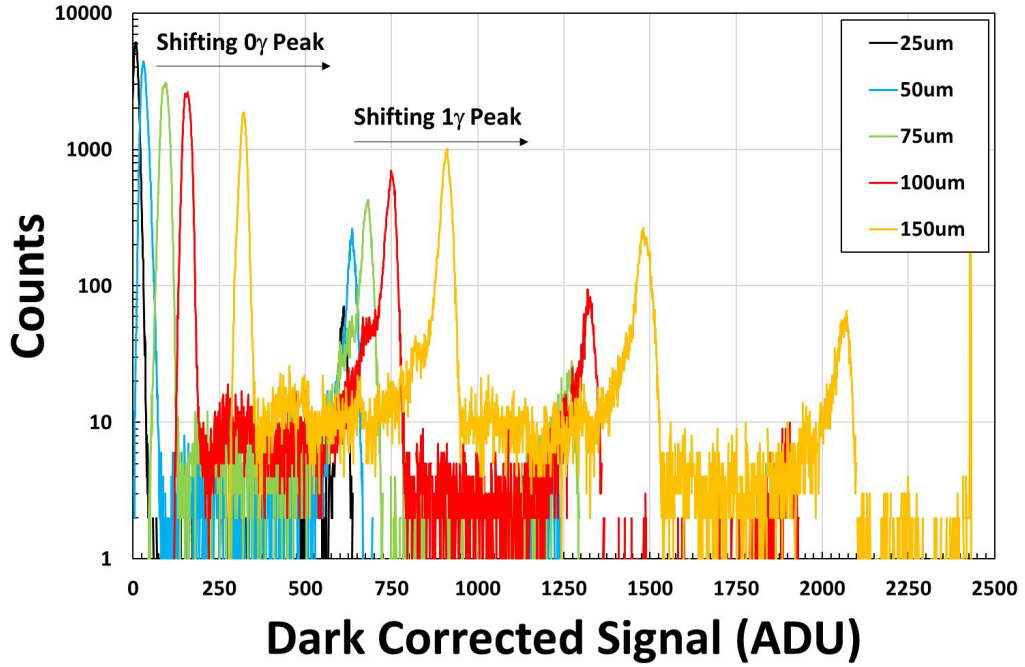
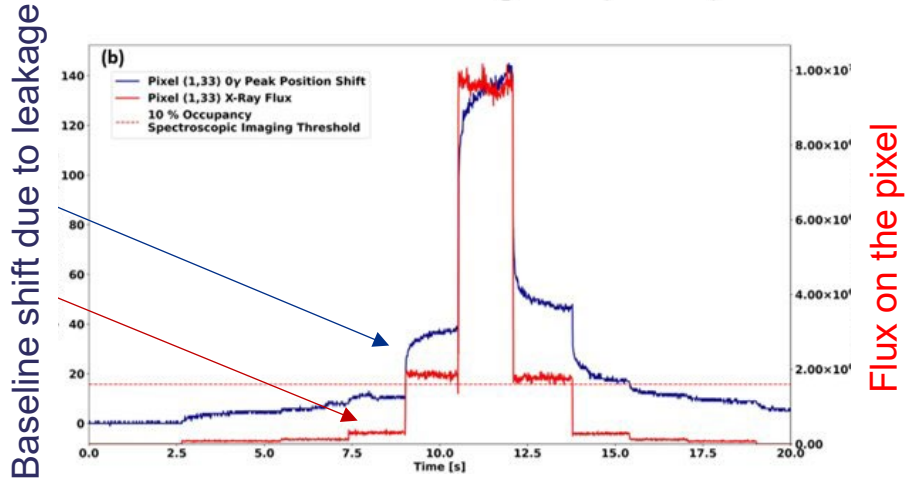
HF-CZT

- Increasing 20keV mono beam size on HEXITEC-MHz ASIC
- 0ph = dark+leakage current
- Flux up 10^7ph/mm^2/s
- Observed an excess leakage current ~100pA/mm^2
- Small pixel, short integrations all help to mitigate effect





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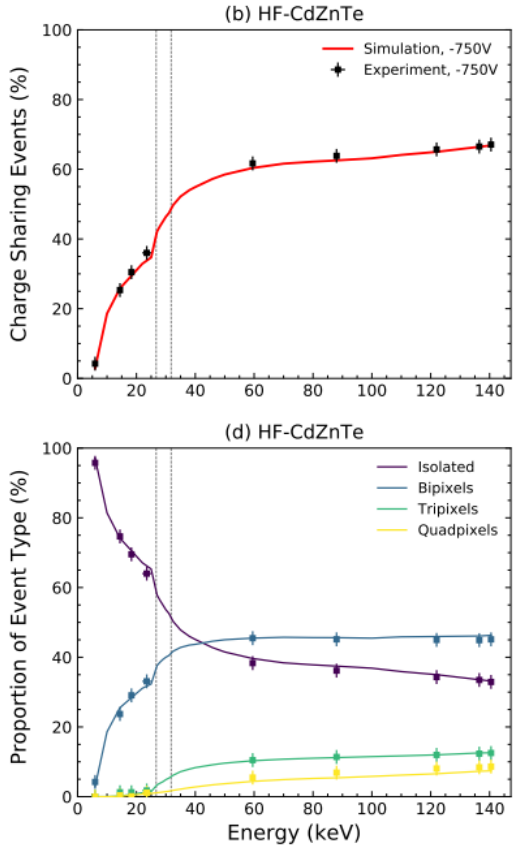
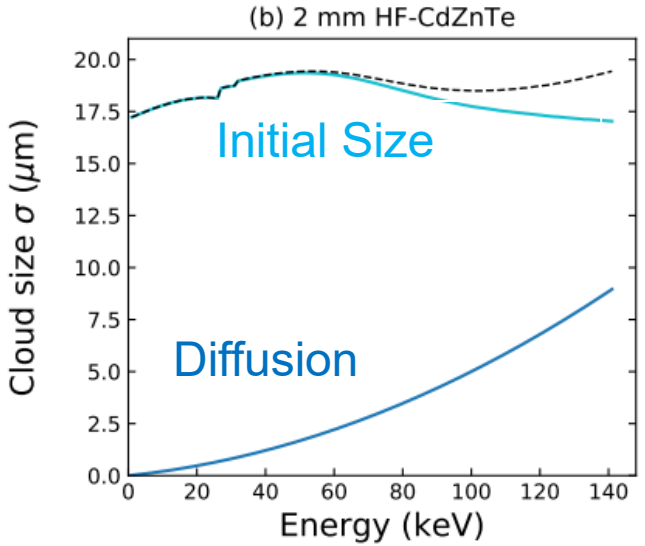
HF-CZT – Charge cloud size

- 250µm pixels simulated and measured on 2mm thick
- Assuming a Gaussian
  - FWHM @ 60keV = 45µm
  - FWTM @ 60keV = 80µm
- Could go thinner
  - 1.5mm offer by Redlen
  - For comparison 1mm CdTe
    - FWHM @ 60keV = 35µm
    - FWTM @ 60keV = 70µm



Kjell Koch-Mehrin
Thesis - here



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Flux Challenge

Adaptive Gain Integrating Detectors

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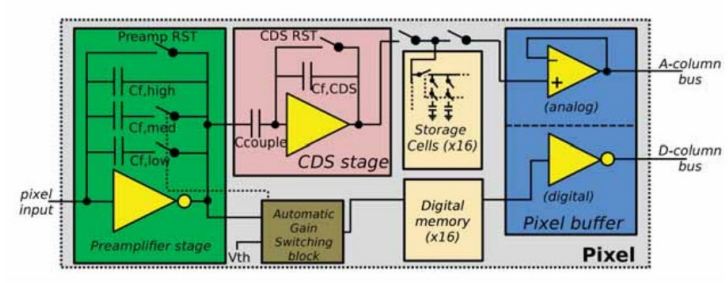
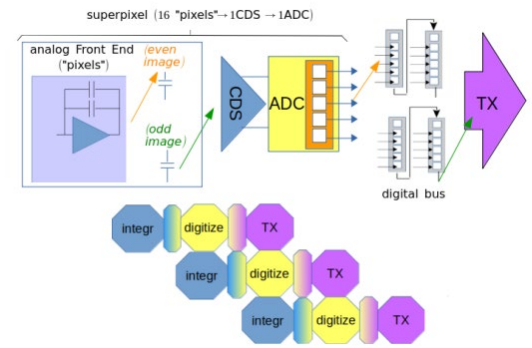
15th International Workshop on Radiation Imaging Detectors
23–27 June 2013,
Paris, France

Prototype characterization of the JUNGFRAU pixel detector for SwissFEL

A. Mozzanica,[a,1] A. Bergamaschi,[a] S. Cartier,[a,b] R. Dinapoli,[a] D. Greiffenberg,[a] I. Johnson,[a] J. Jungmann,[a] D. Maliakal,[a] D. Mezza,[a] C. Ruder,[a] L. Schaedler,[a] B. Schmitt,[a] X. Shi[a] and G. Tinti[a,c]





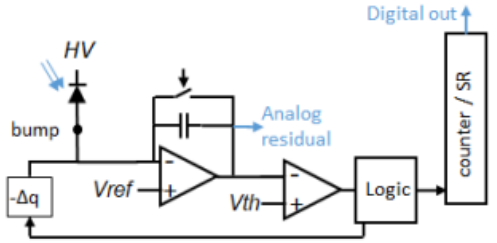
14th International Conference on Synchrotron Radiation Instrumentation (SRI 2021) IOP Publishing
Journal of Physics: Conference Series **2380** (2022) 012093 doi:10.1088/1742-6596/2380/1/012093

Development of CoRDIA: an Imaging Detector for next-generation Synchrotron Rings and Free Electron Lasers

A Marras[1], A Klujev[1], S Lange[1], T Laurus[1], D Pennicard[1], U Trunk[1], C B Wunderer[1], M L Hafiane[2], T Hemperek[2], T Kamilaris[2], H Krueger[2], T Wang[2] and H Graafsma[1,3]

1) Center for Free-Electron Laser Science CFEL, Deutsches Elektronen-Synchrotron DESY, Germany
2) University of Bonn, Bonn, Germany
3) Mid Sweden University, Sundsvall, Sweden

Charge Integrating and Cancellation



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Published: June 23, 2020

High dynamic range CdTe mixed-mode pixel array detector (MM-PAD) for kilohertz imaging of hard x-rays

H.T. Philipp[a,1] M.W. Tate[a] K.S. Shanks[a] P. Purohit[a] and S.M. Gruner[a,b]
[a]Laboratory of Atomic and Solid State Physics, Cornell University, Ithaca, NY 14853, U.S.A.
[b]Cornell High Energy Synchrotron Source (CHESS), Cornell University, Ithaca, NY 14853, U.S.A.
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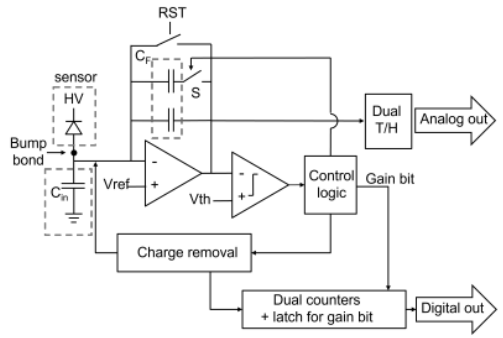
Characterization of 128 × 128 MM-PAD-2.1 ASIC: a fast framing hard x-ray detector with high dynamic range

D. Gadkari,[a,b] K.S. Shanks,[c] H. Hu,[a,e] H.T. Philipp,[a] M.W. Tate,[a] J. Thom-Levy[b,*] and S.M. Gruner[a,c,d]



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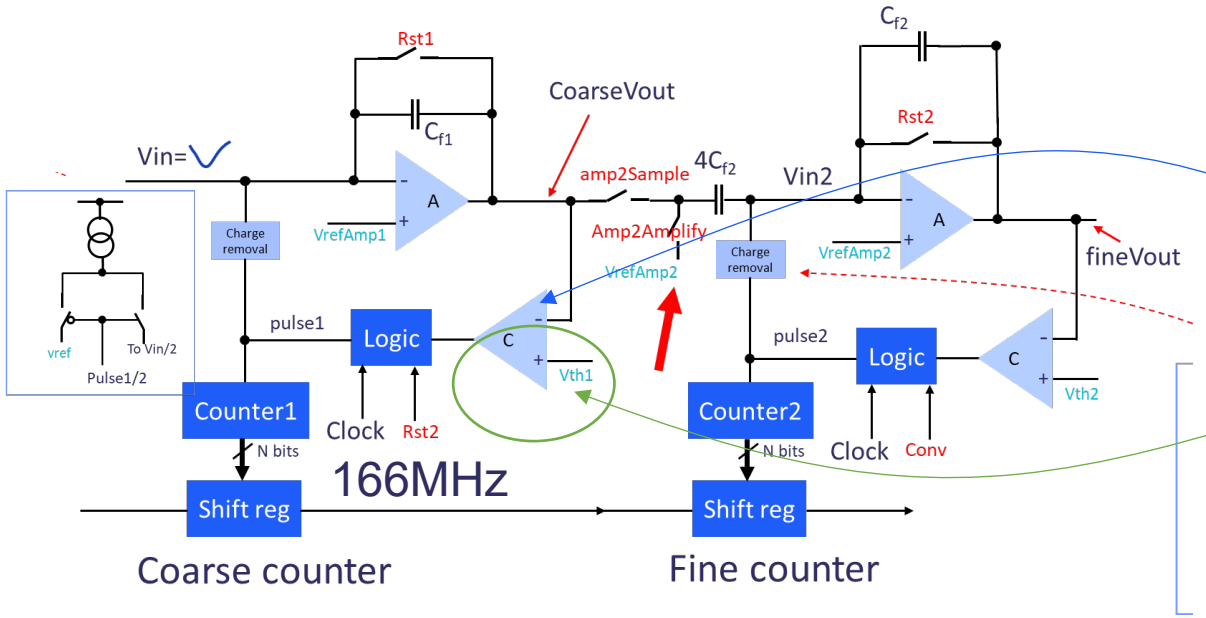
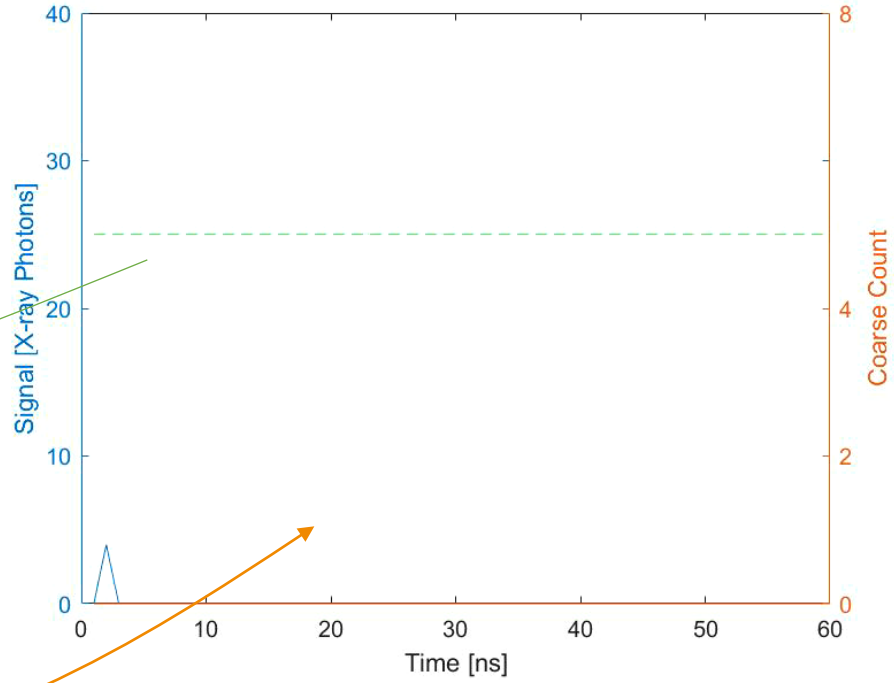
DynamiX – Coarse Stage





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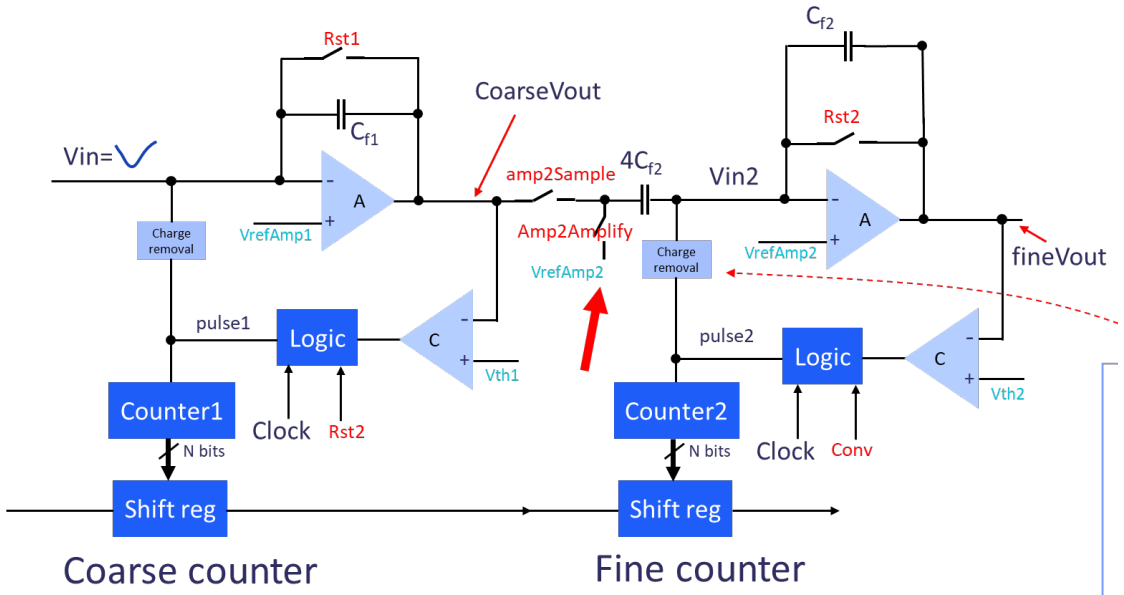
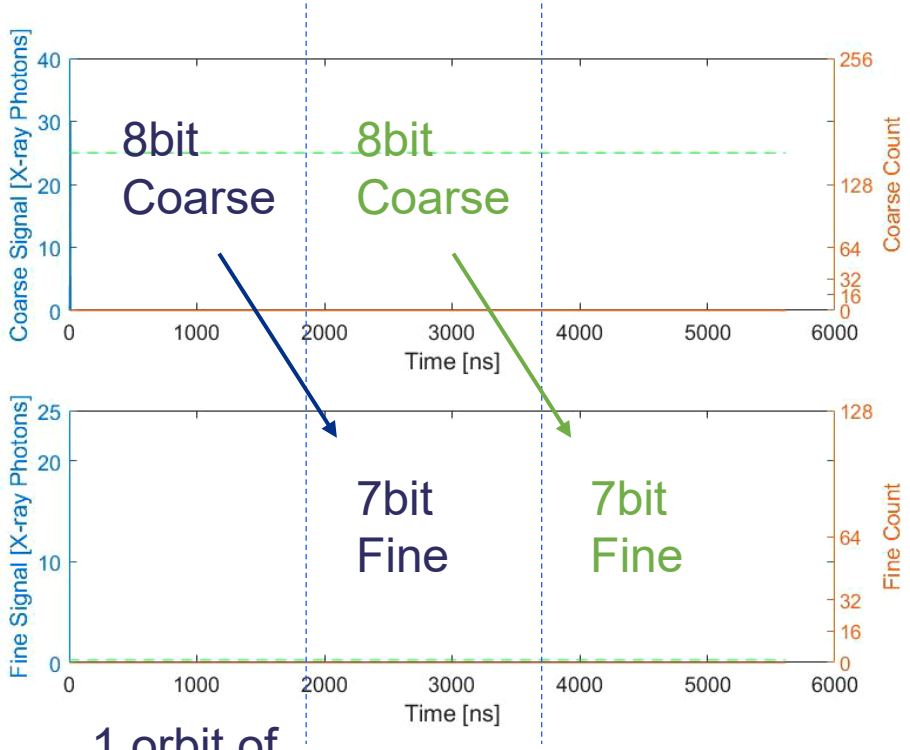
DynamiX – Transfer and Fine Stage



83MHz Counter
Constant Charge Removal



1 orbit of Diamond

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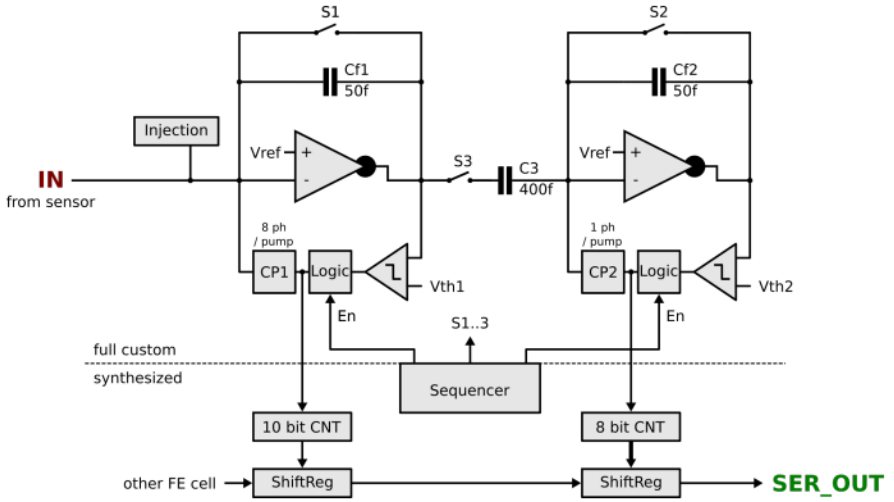
XIDer

- 2 stage cancellation
- Incremental digitisation
- 200MHz target for cancellation rate
- Multiple test structures inc probe output



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Accepted: January 27, 2021
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Concepts for the XIDer readout ASIC incorporating a pipelined ADC with very low dead time

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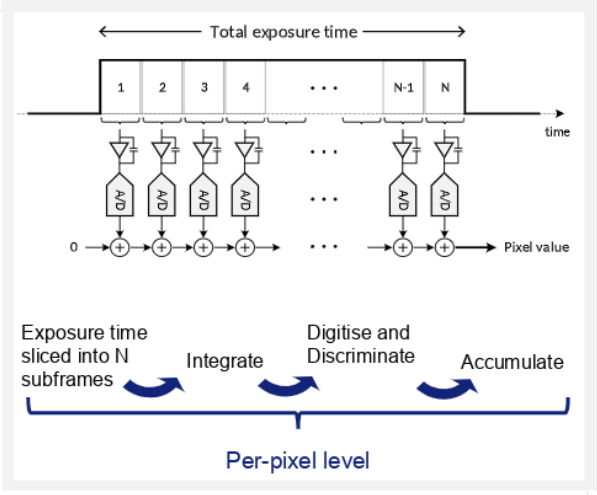
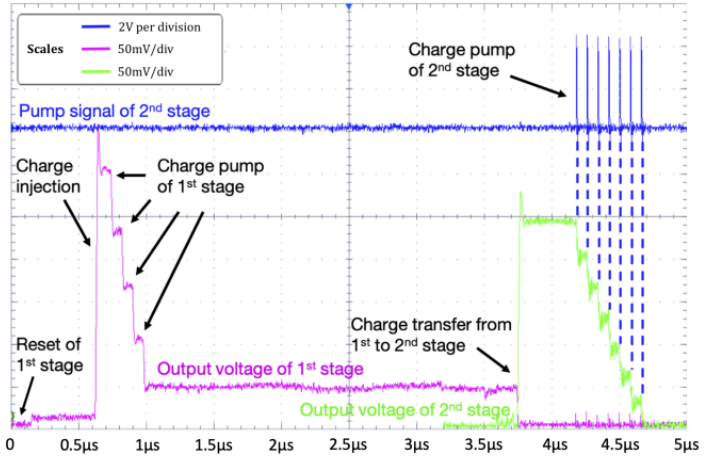
[a] Institute of Computer Engineering, Heidelberg University, Im Neuenheimer Feld 368, Heidelberg, Germany
[b] European Synchrotron Radiation Facility, 71 Avenue des Martyrs, Grenoble, France

E-mail: david.schimansky@ziti.uni-heidelberg.de





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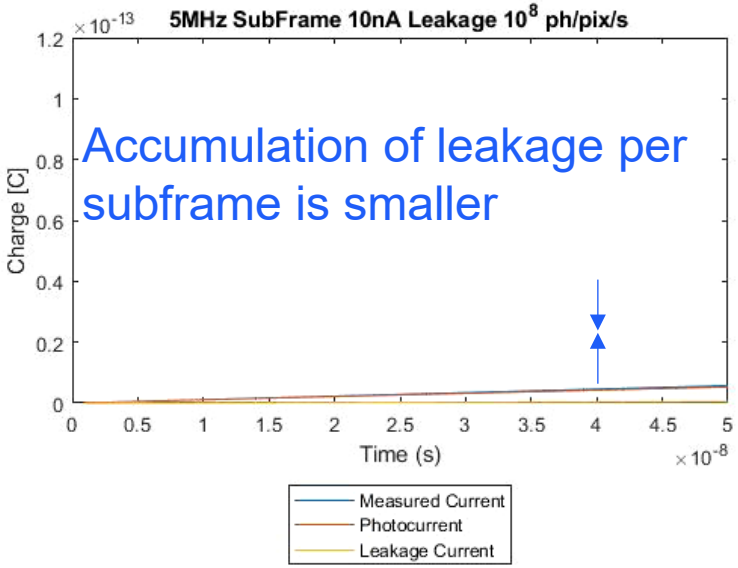
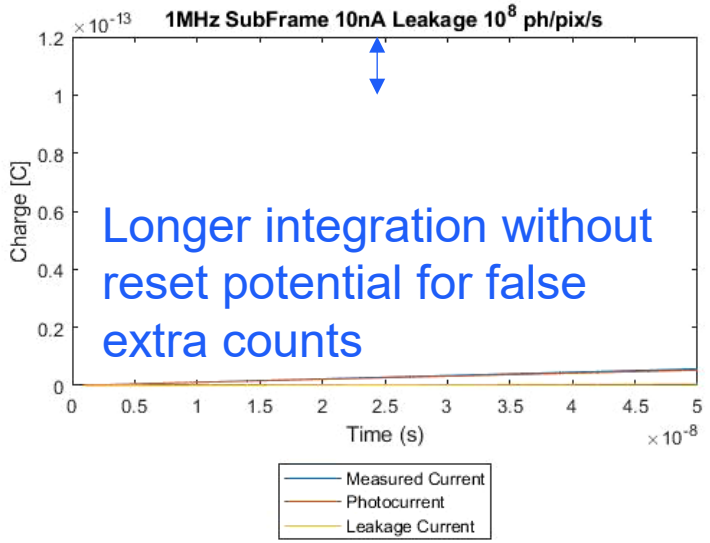
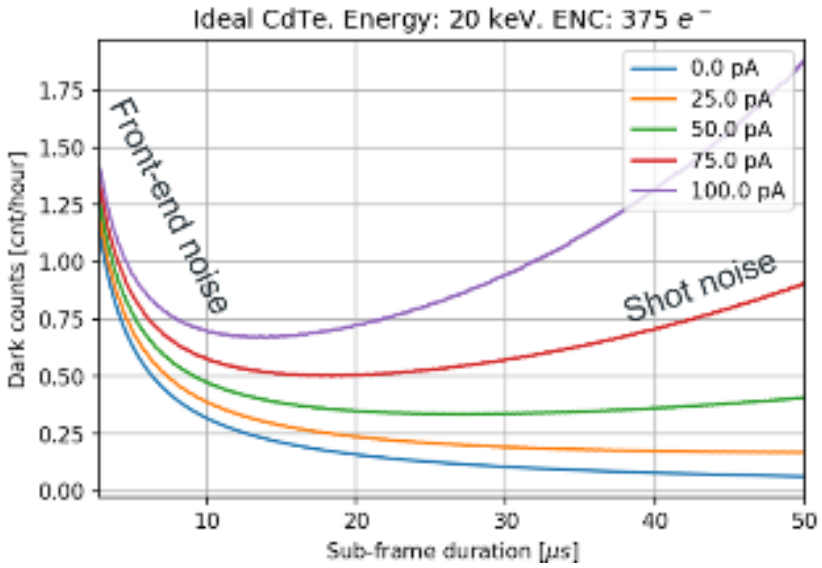
Benefit of incremental digitisation







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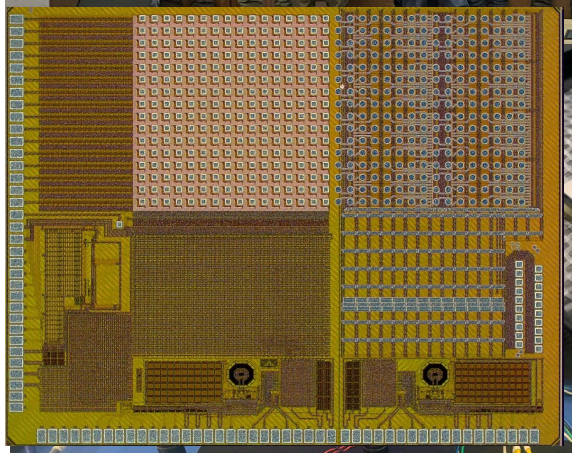
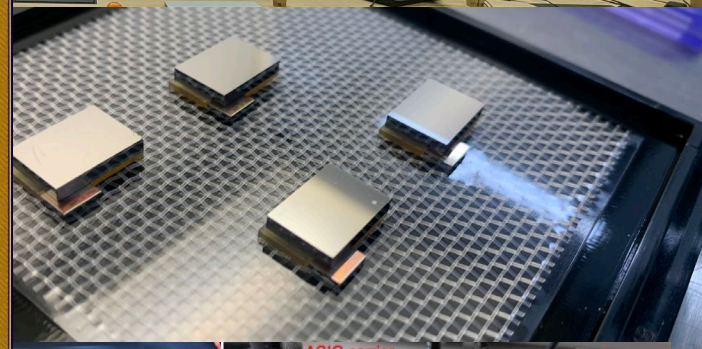
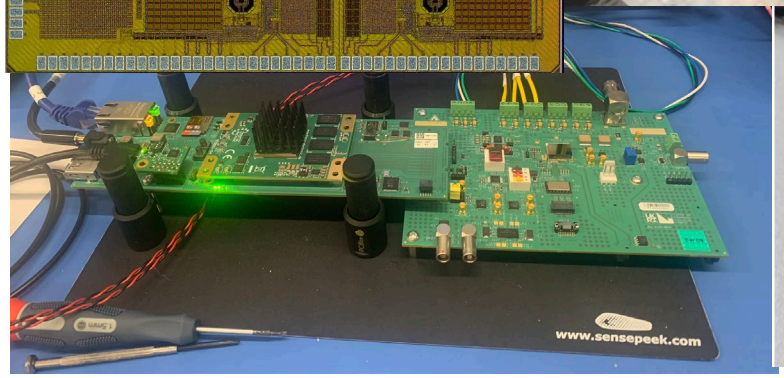
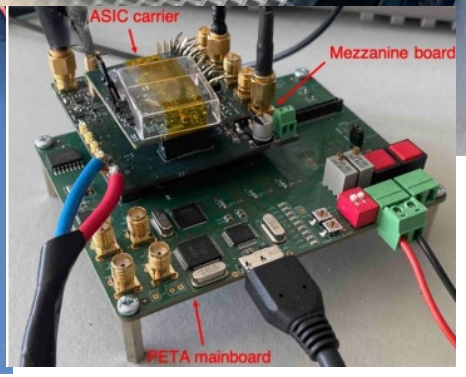
XIDyn MPW

- Enough similarities and requirements and design to collaborate
- Both 65nm TSMC designs
- 32x16 pixels
  - 16x6 of XIDer and DynamiX
  - 2x14.1Gbps serialiser/16x16
- HF-CZT on 110µm pitch
- Aim to be side by side pixel comparison









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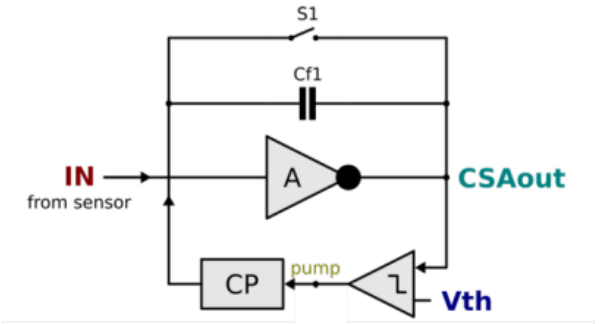
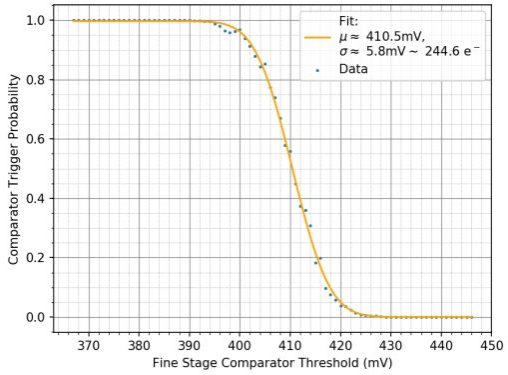
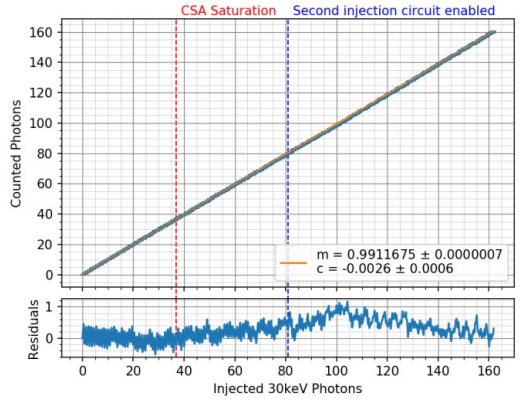
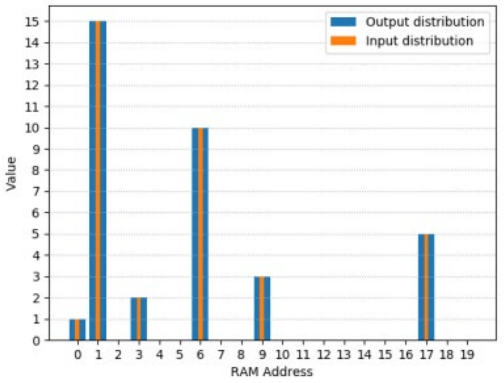
XIDer Pixel Results

- Threshold scan of the pixels gives a noise of σ=308e- for both stages combined
- Linearity scan for impulse test signal within spec
- Flexibly RAM for storing,veto, summing or histogram in pixel
- Charge transfer between coarse→fine ~77ns… ideally speed up in scaling to larger ASIC









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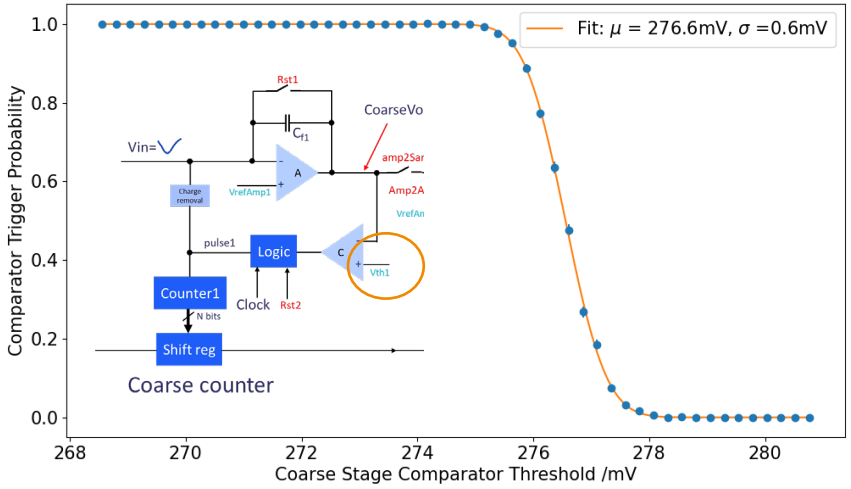
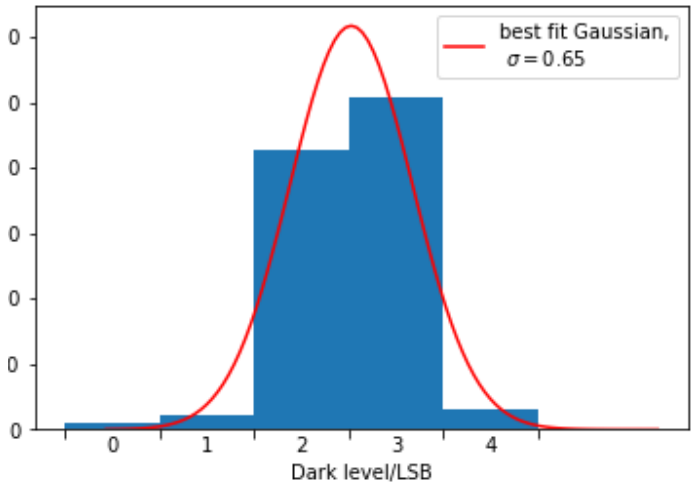
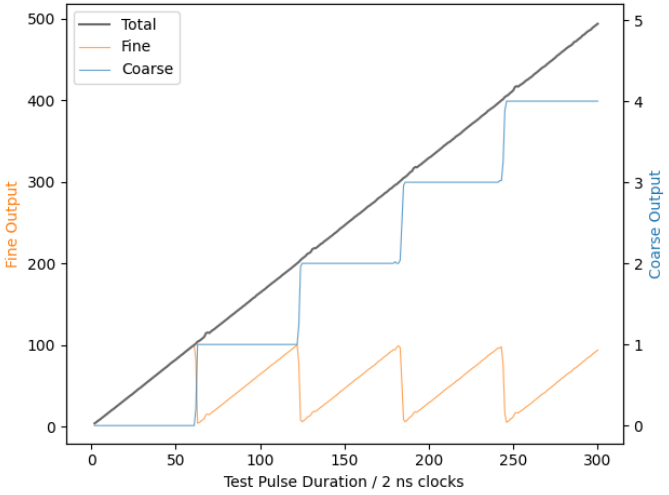
DynamiX Pixel Results

- S-parameter from coarse stage ~560e- → 6.5keV FWHM
- Transfer to fine stage + fine stage noise → 10keV FWHM







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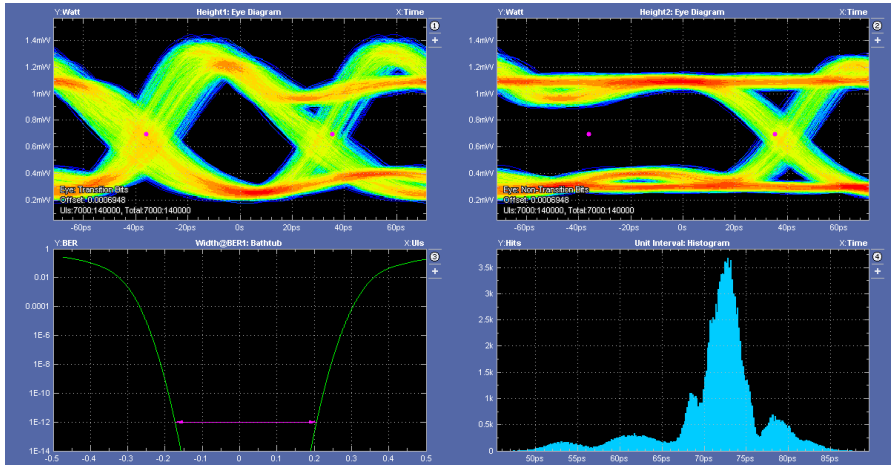
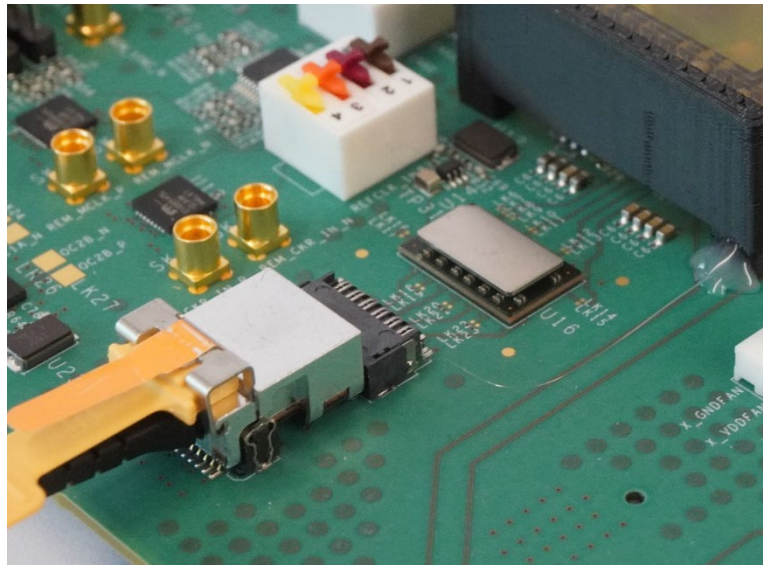
Serialiser Results

- Aurora encoded 64b66b CML
- 14.1Gbps working
  - Half speed contingency
- Conversion to optical via Samtec Firefly close to ASIC
- Receiver and frame build in FPGA with 100G UDP out
  - Just completed firmware milestone
  - All test data here via slower lines





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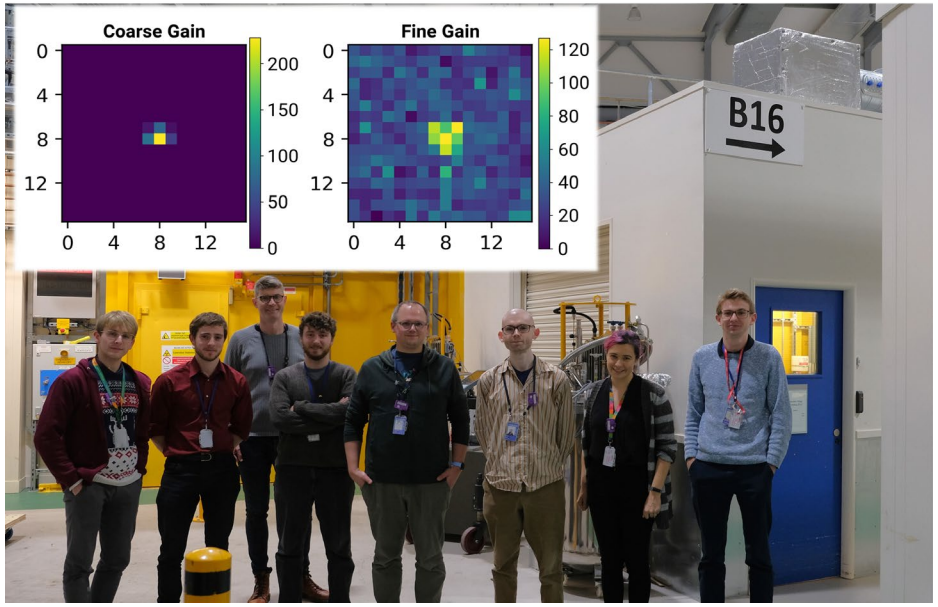
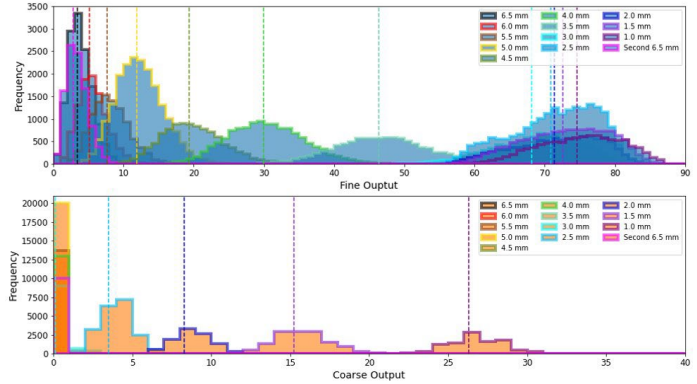
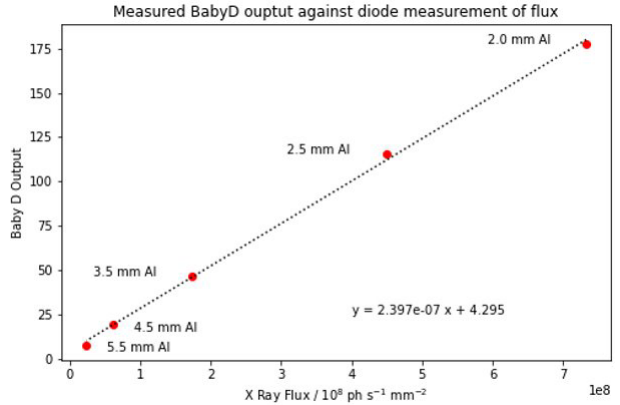
First X-ray Test

- 20keV mono-energy beam
- Change filters and beam-size to change flux on the detector
- Very preliminary!



Imaging (bonding)	Flux Range (10^9 ph/mm^2/s)	Single Photon
✓	✓	?





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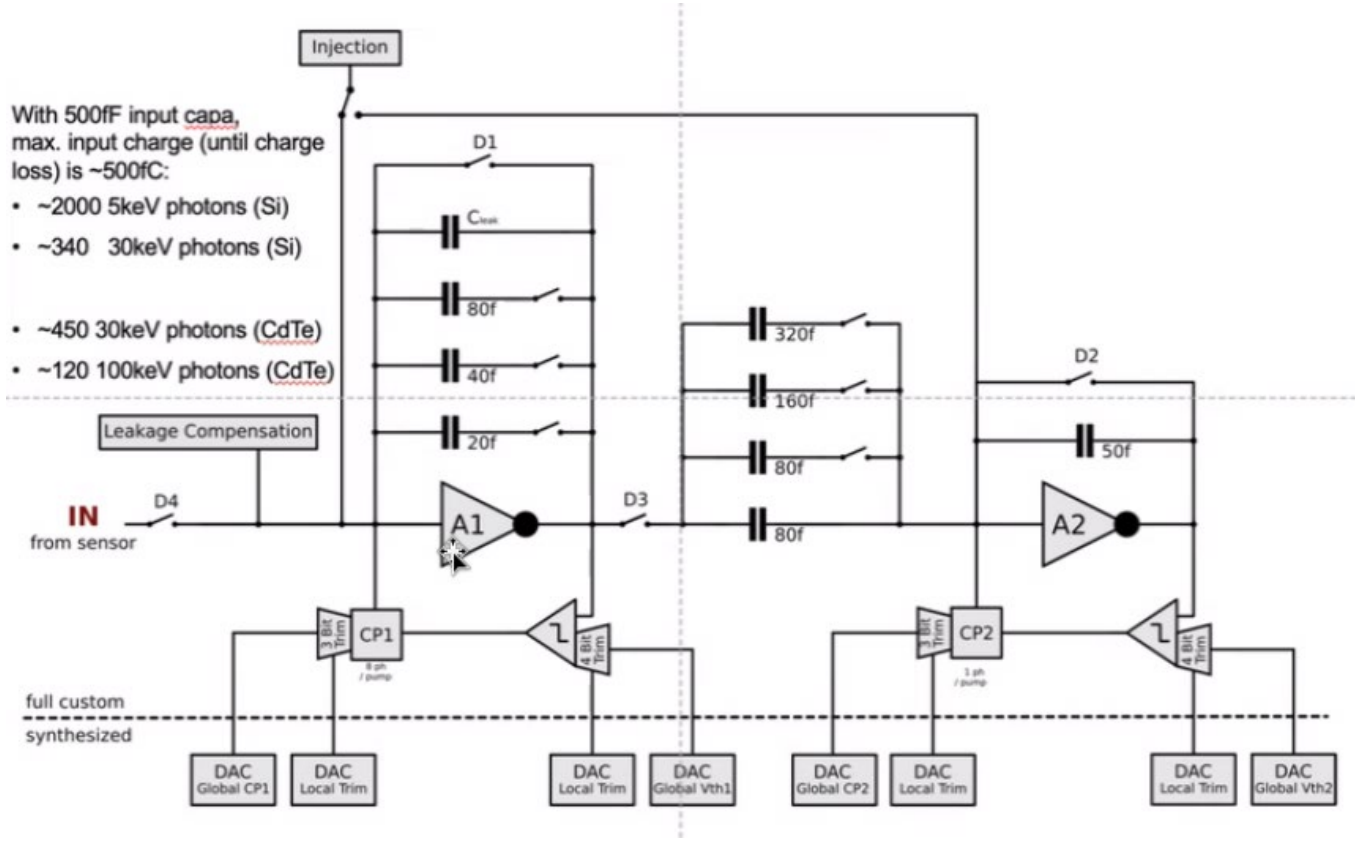
XIDyn Pixel

- Selectable gain for different energy beamlines
- In pixel trim for charge cancellation and voltage thresholds per pixel
  - help with IR drop
- Switch to disconnect from pixel
  - Prevent charge overflow
  - Asynchronous source
- Very high gain mode to help with single photon and calibration
  - Potential to measure leakage current and compensate?
- In pixel RAM to store up to x256 8bit subframes at 5.7MHz
- Store 16bit subframes, sum and readout



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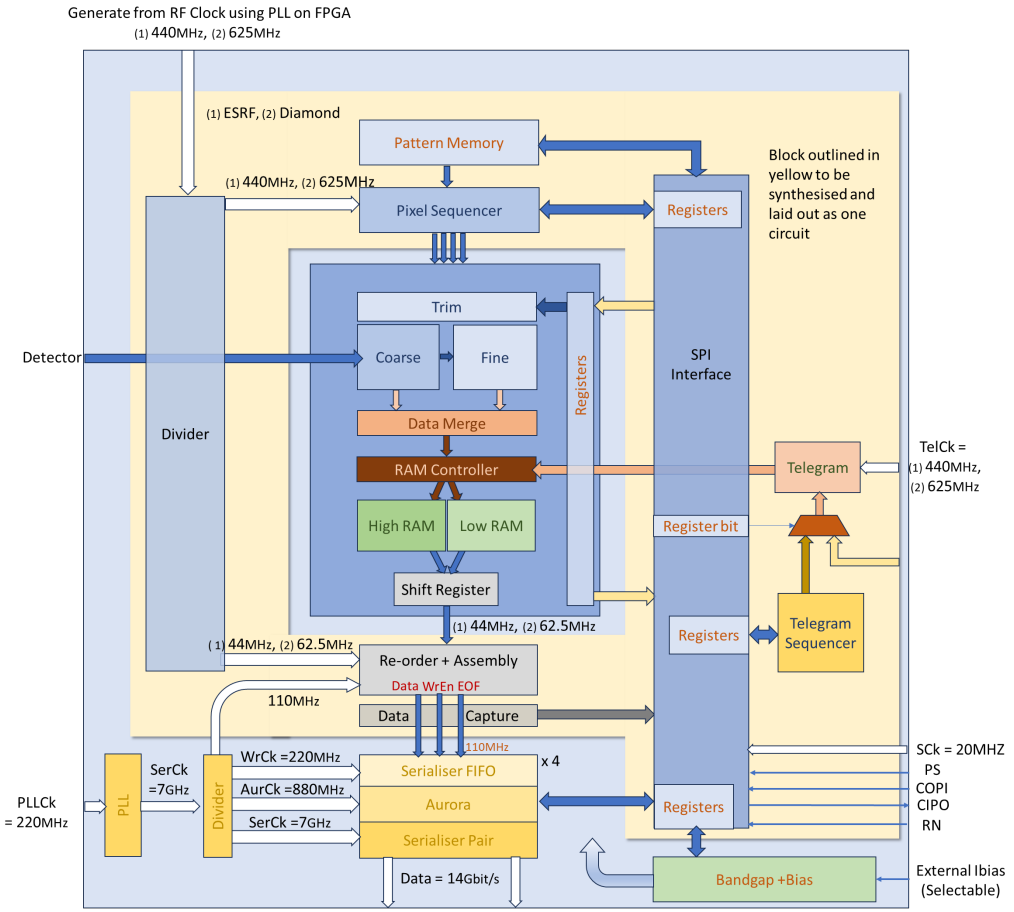
XIDyn Full Scale ASIC

- 144x192 pixels on 110µm pitch
- RAM per pixel for summing, storing or adaptively used over telegram command
- 144x32 pixels per 14.1Gbps serialiser
  - 177kHz continuous frame rate possible
    - e.g. 1 subframe per turn of Diamond at 533kHz… sum or average 4 subframes and readout at 133.25 kHz
  - Ability to use 1 of 6 serialisers
    - fewer lines, lower cost but still 30kHz continuous
  - 36 ASICs per Mpixel → 3Tbps/Mpixel or 6TBs/16M
- Master clock derived from RF clock



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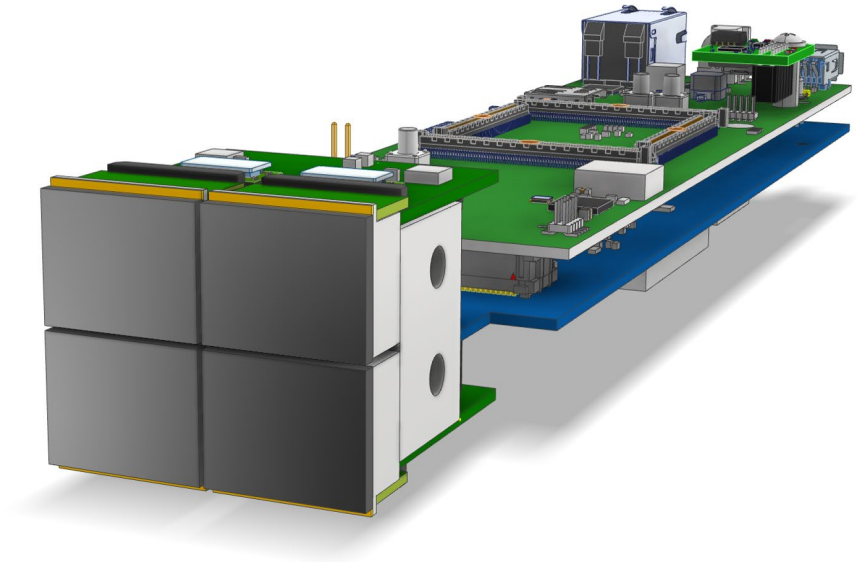
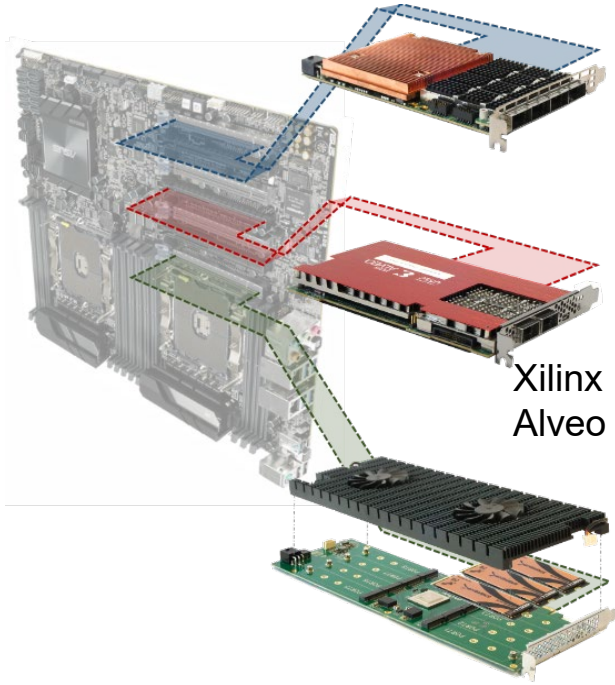
XIDyn Demonstrator

- Target to build a v1 2x2 module in 2025





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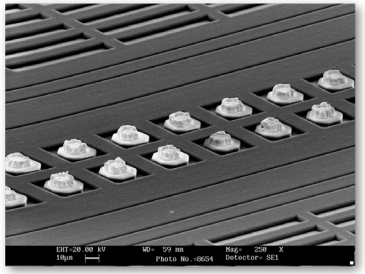
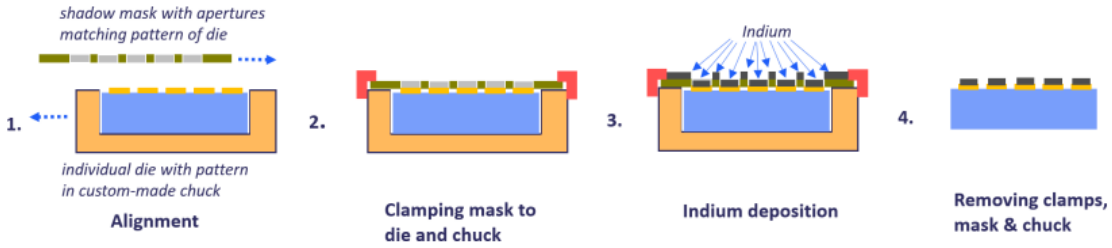
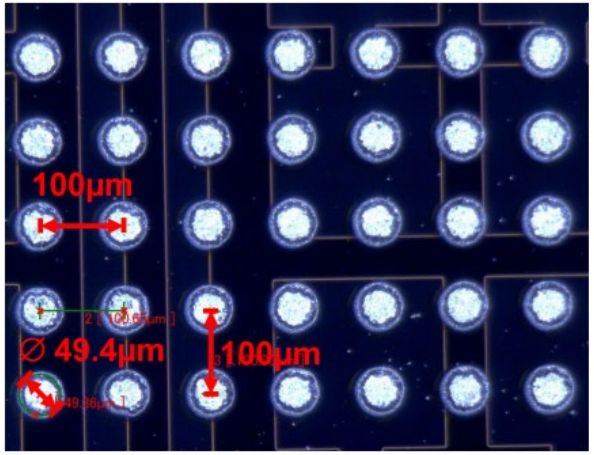
Bonding

- CZT is temperature sensitive and brittle
- Only available as single die
  - Lithography difficult
- Low temperature silver epoxy and gold studs
- In bonding with shadow masks







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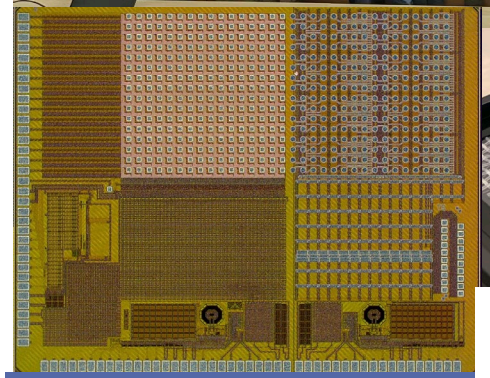
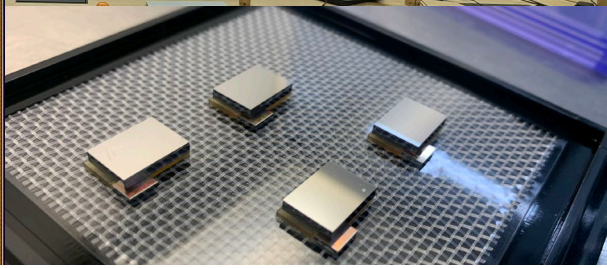
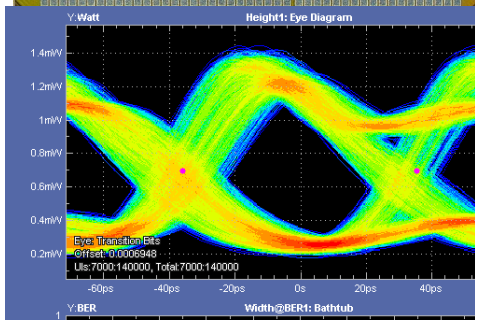
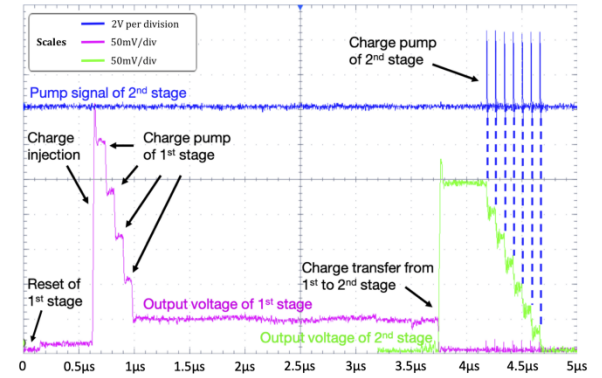
Summary

- 144x192 pixel v1 ASIC in design
  - >100kHz continuous at >10^{11}ph/mm^2/s
  - 5.7MHz burst capture
- 2x2 Camera demonstrator for 2025
- Mpixels for facilities in late 2020s
- CdZnTe detector tests, readout hardware, etc in parallel
- Future versions and wider collaboration welcome









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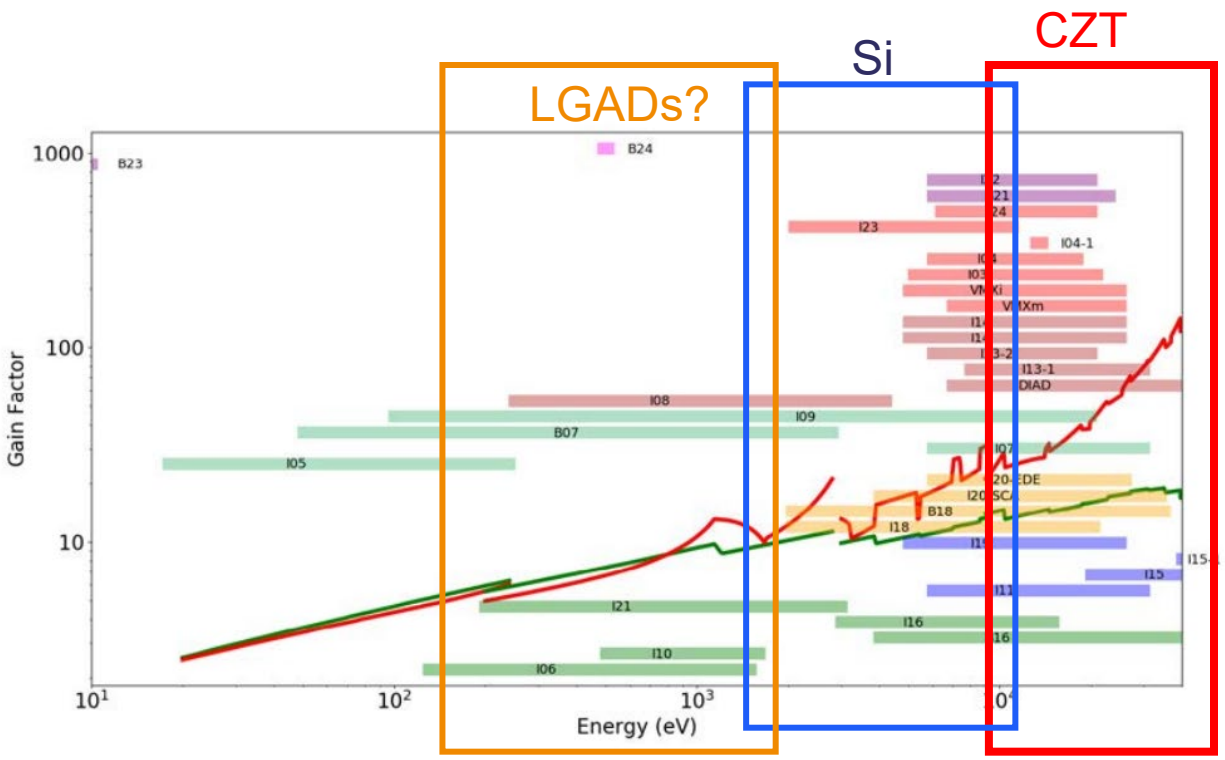
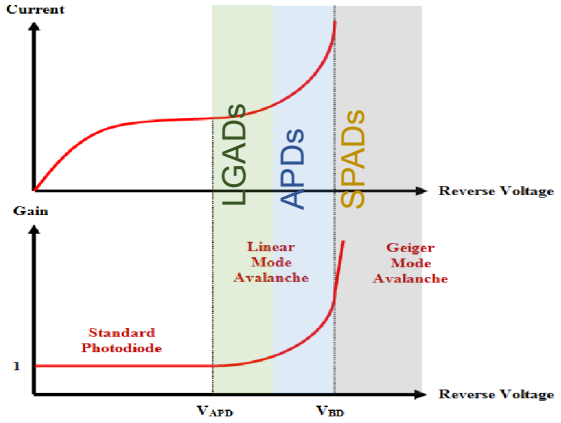
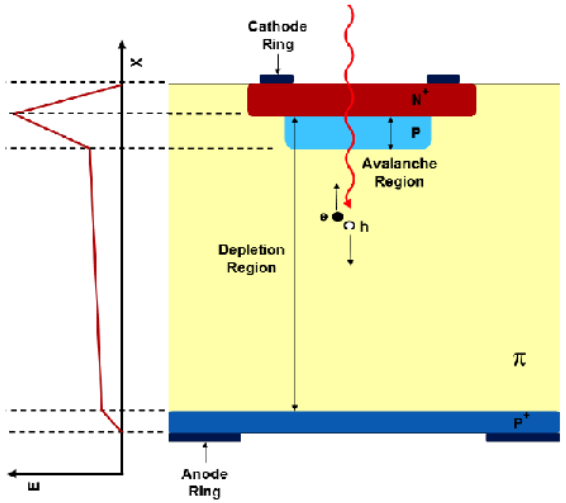
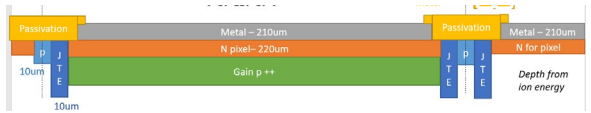
Back-up Slides

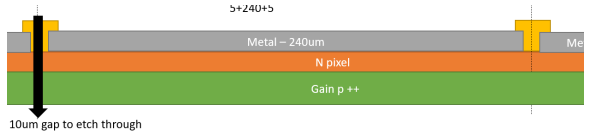
Low Energy?

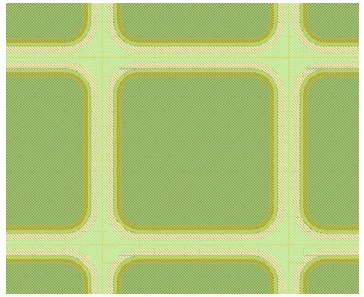


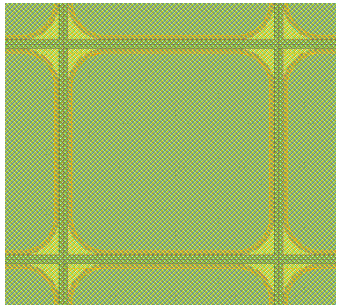












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More on CZT

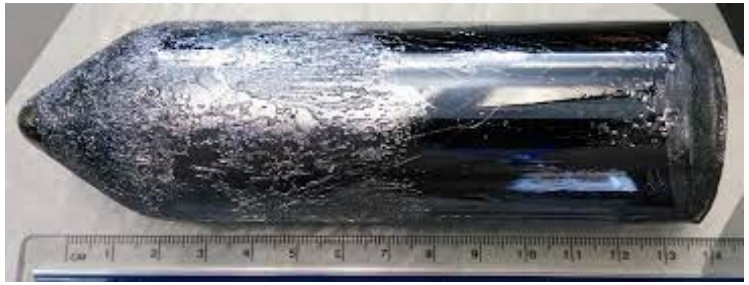
11TH INTERNATIONAL CONFERENCE ON POSITION SENSITIVE DETECTORS
3–8 SEPTEMBER 2017
THE OPEN UNIVERSITY, WALTON HALL, MILTON KEYNES, U.K.

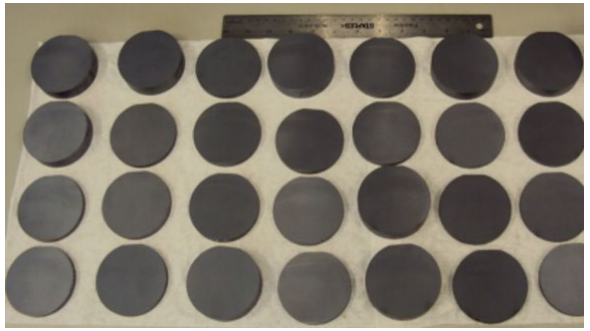
Characterisation of Redlen high-flux CdZnTe

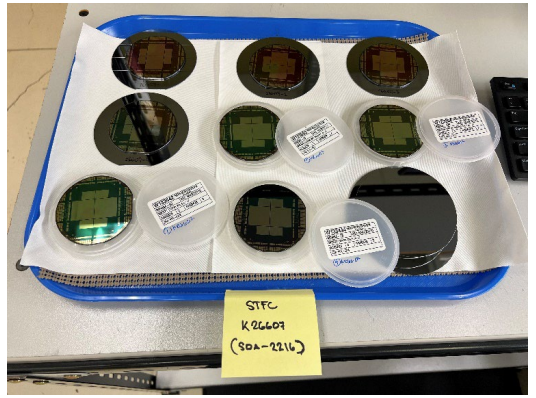
B. Thomas,[a,b,1] M.C. Veale,[a] M.D. Wilson,[a] P. Seller,[a] A. Schneider[a] and K. Iniewski[c]

Table 1. A summary of the measured charge transport properties of three "high-flux" Redlen CdZnTe detectors [14, 16].

	$\mu_e\tau_e$ ($\times10^{-4}$ cm^{2}V^{-1})	μ_e (cm^{2}V^{-1}s^{-1})	τ_e ($\times10^{-6}$ s)	$\mu_h\tau_h$ ($\times10^{-4}$ cm^{2}V^{-1})	μ_h (cm^{2}V^{-1}s^{-1})	τ_h ($\times10^{-6}$ s)
High Flux CdZnTe	11 ± 6	940 ± 190	1.2 ± 0.8	2.9 ± 1.4	114 ± 22	2.5 ± 1.4
Standard CdZnTe	100	1100	11	0.2	88	0.2







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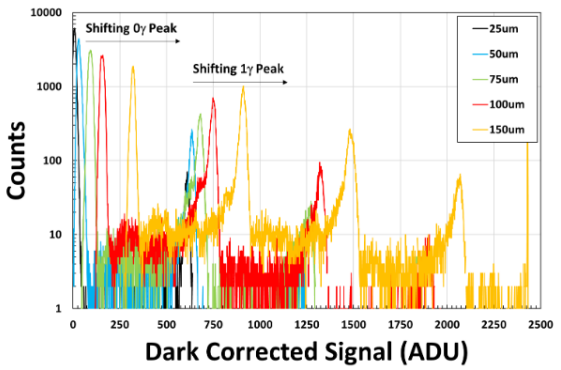
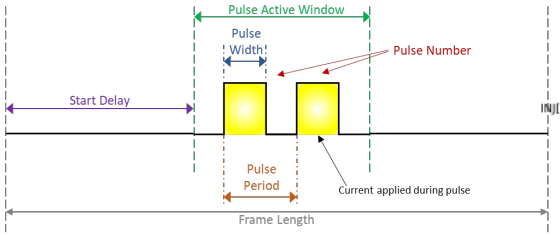
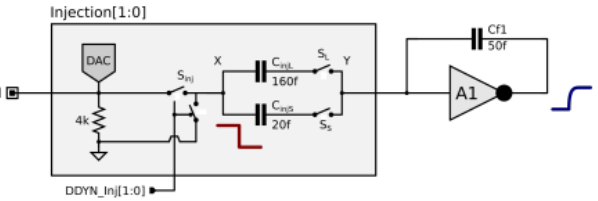
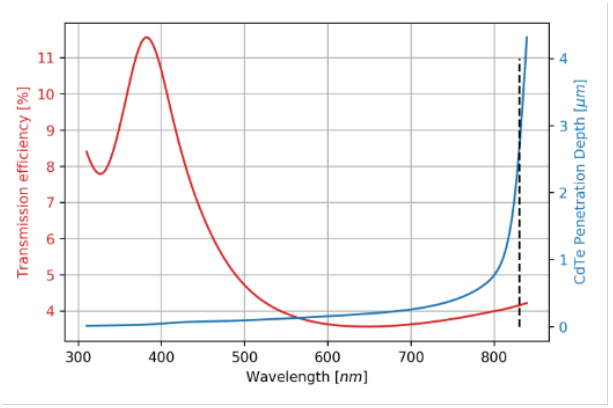
Calibration

- Single photon illumination to give E = ADU = Test Signal
  - Trim Vref, Vth and Cancel
- Test signal sweeps
  - Current source or voltage step
- LED sweeps
- Mono-energy beam illumination









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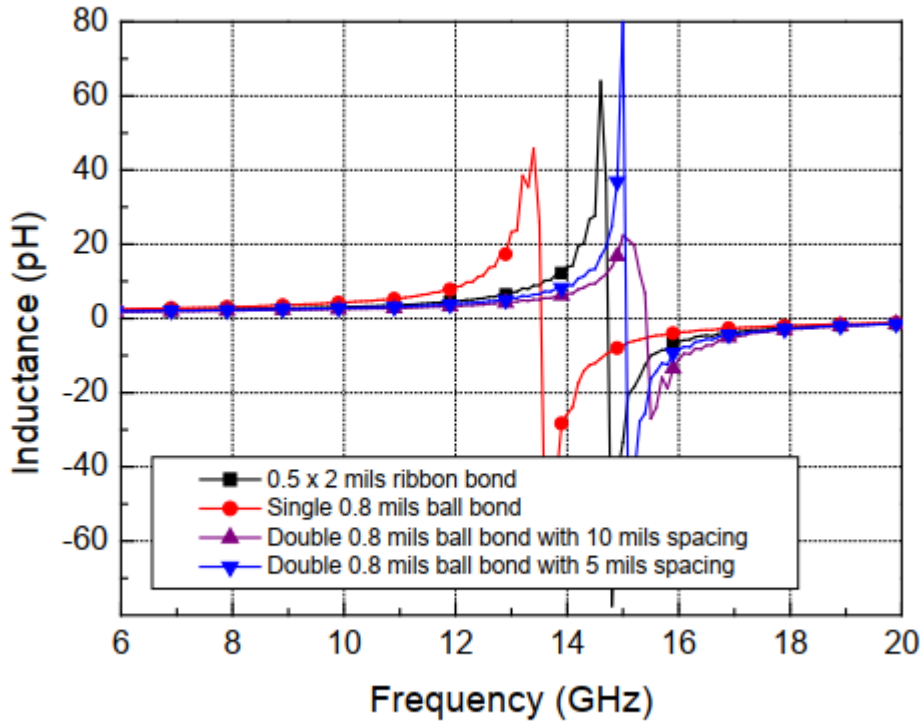
High Speed Data Output

- Impedance of wire bonds
- Materials for PCB and tracking
- Optical conversion
- Mitigation
  - Half speed serialiser
  - “Benchtop” Quad
  - Use test devices to prototype



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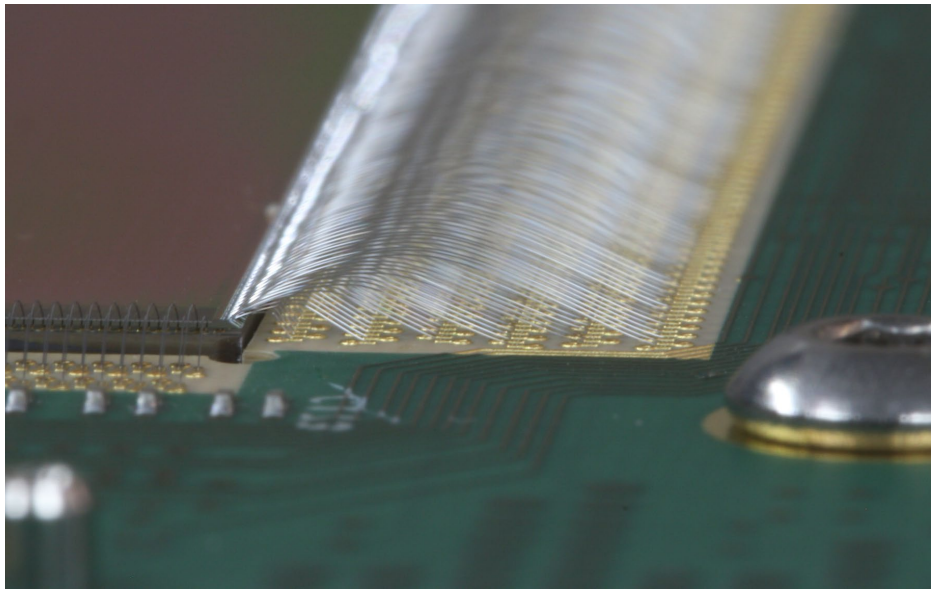
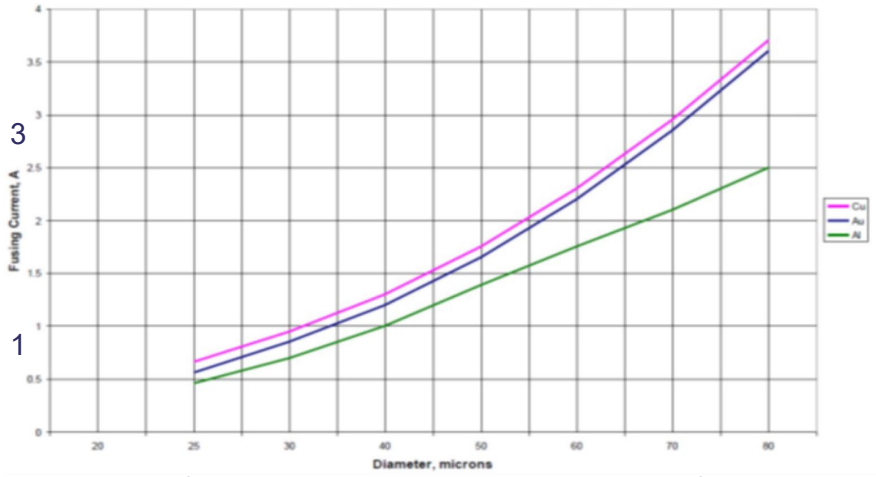
Bond Wires

Greedy ASIC designer -> Nightmare on the PCB



Fusing Current as a function of bond diameter



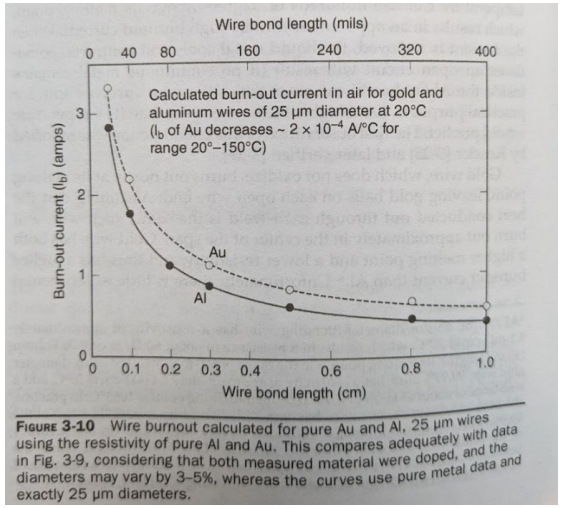
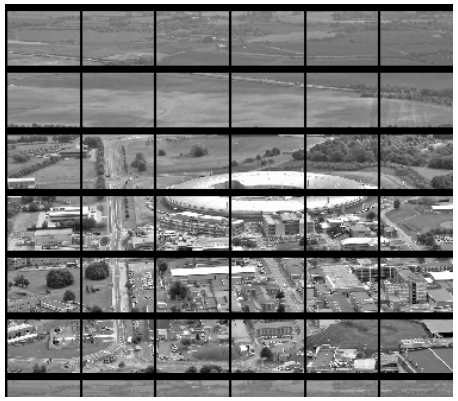


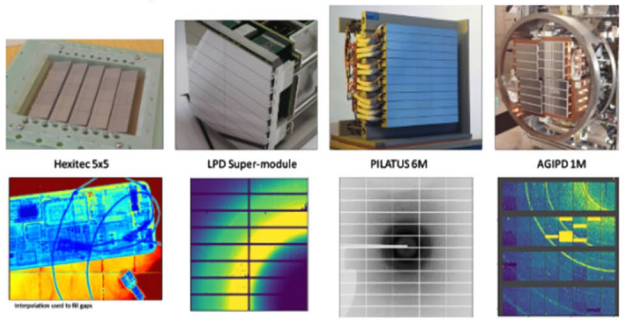
FIGURE 3-10 Wire burnout calculated for pure Au and Al, 25 μm wires using the resistivity of pure Al and Au. This compares adequately with data in Fig. 3-9, considering that both measured material were doped, and the diameters may vary by 3–5%, whereas the curves use pure metal data and exactly 25 μm diameters.

Fusing Current as a function of bond length

Dead Space



Other Examples and % Dead Area



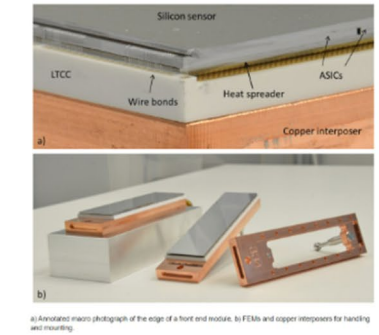
Examples of tiled systems. Hexitec and LPD are STFC systems, PILATUS by Dectris, AGIPD by DESY

System	Pixel Size	Pixels per tile (X,Y)		Missing Pixels Per tile (X,Y)		Dead Area (% X, Y)		Notes
LPD	500	128	32	4	4	3%	13%	Majority of dead area in guard bands
Hexitec	250	80	80	2	0	3%	0%	Compromise with overlapping Geom.
Pilatus	172	487	195	7	17	1%	9%	Gold standard for syncrotrons
Eiger	75	1028	512	12	38	1%	7%	
AGPID	250	498	128	42	30	8%	23%	Edge pixel issues between ASICs

Dead area % in X and Y – typically one dimension is sacrificed for wire bonds

Got to aim for <10% to be comparable to other systems. Will always be difficult to do better than 2-3% due to guard bands.

AGIPD and PILATUS – ASICs back to back with wire bonds on 2 sides



a) Annotated macro photograph of the edge of a front end module, b) FEMs and copper interposers for handling and mounting.

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Hexitec 2x6 Heat Exchanger

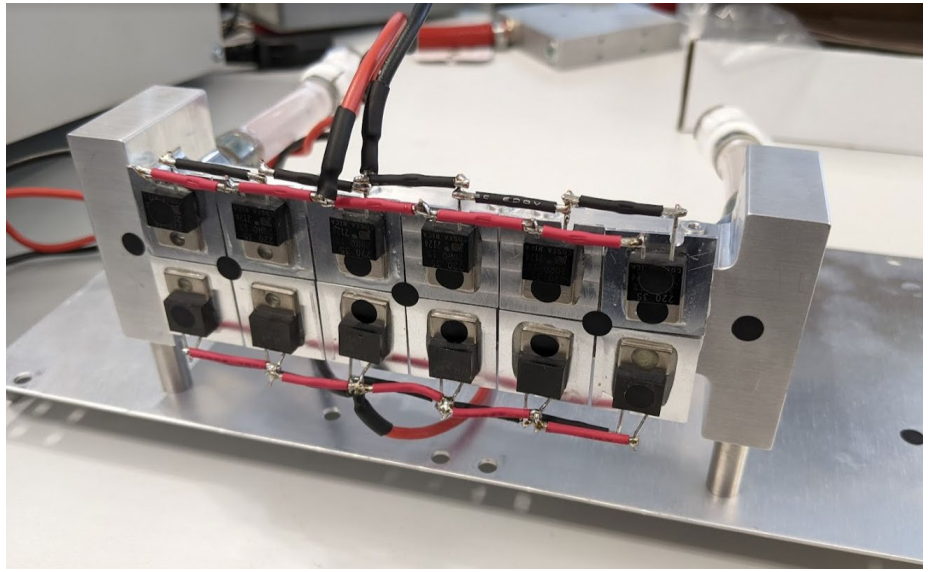
High Power Trials – Target 5W per cm^2

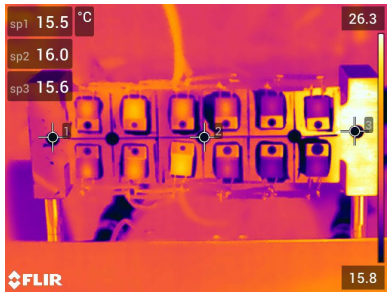
Various measurement points with Black stickers placed to give IR camera reading.

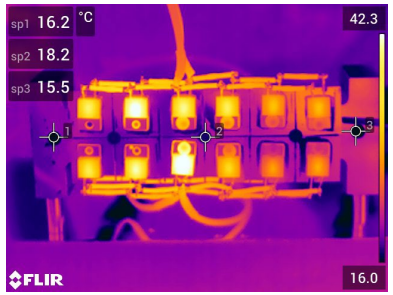
Two branches of resistive loads used to split current across 2 power supplies running up to 7.4A on each channel

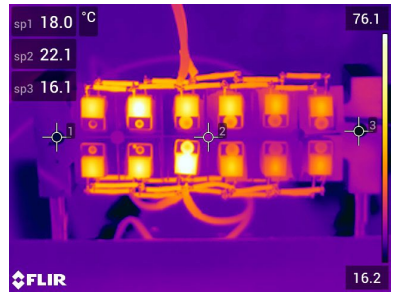
Load Resistors = 20 Ohm 1%
Glued to base plates with a thin layer of epoxy.

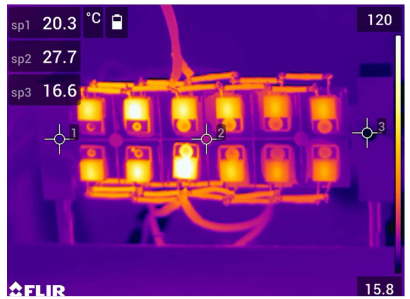
Chiller – Huber 280W set to 15C











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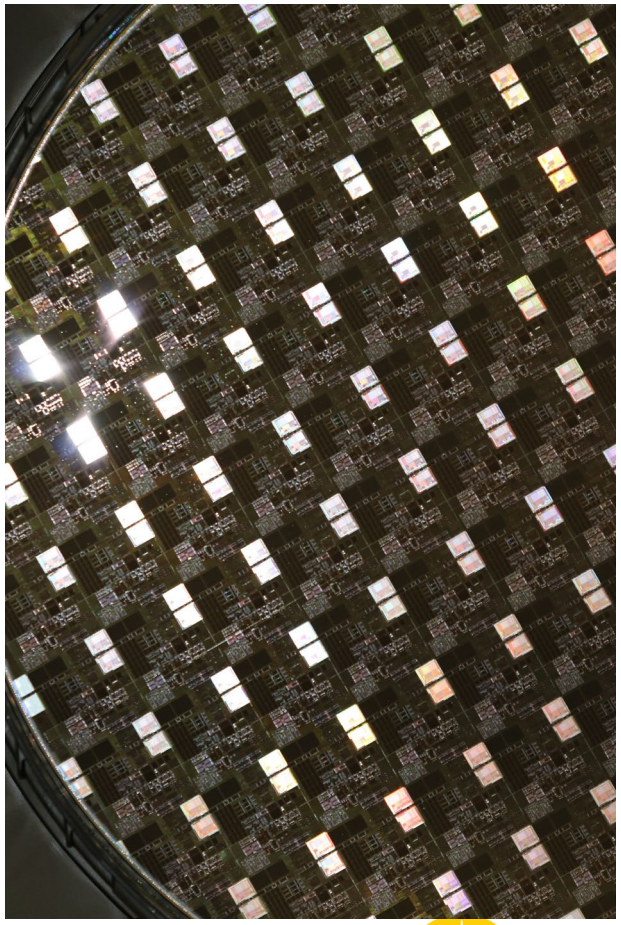
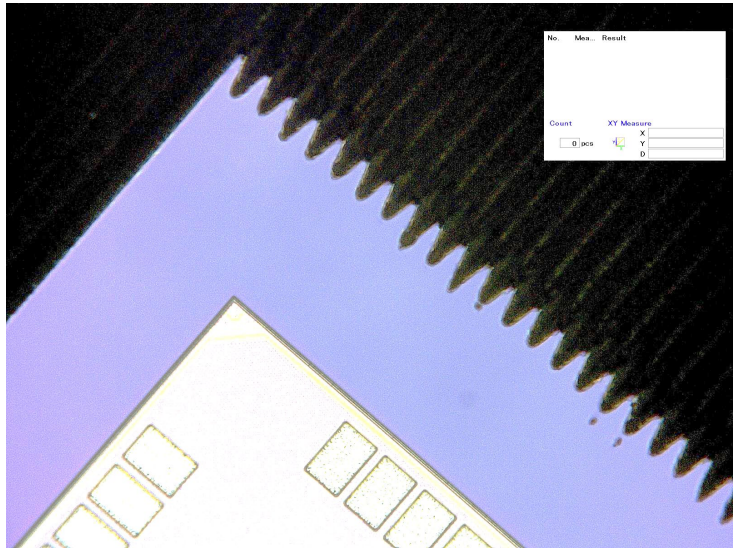
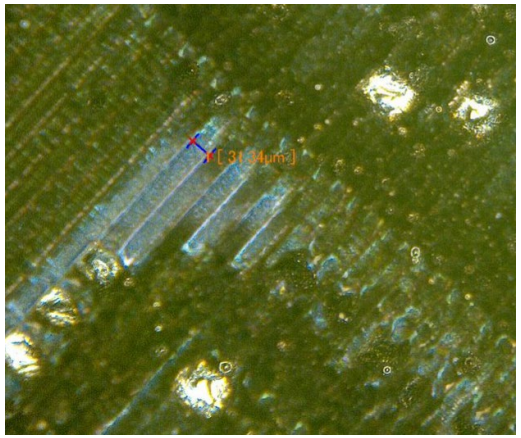
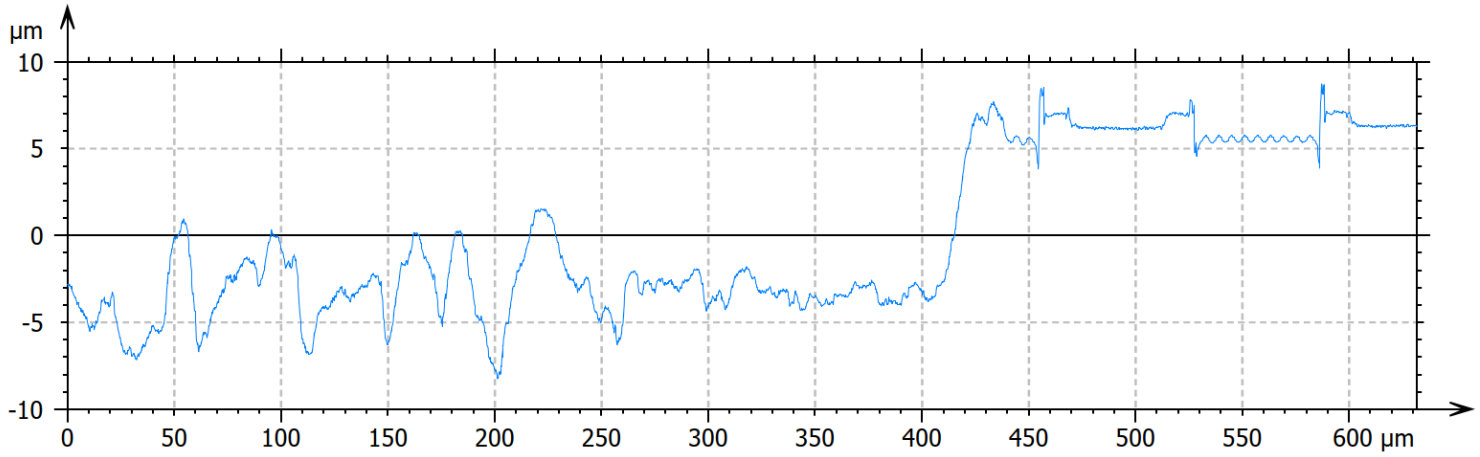
MPW Wafers









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