Digital data processing in pixelated readout ASICs

Robert Szczygieł
AGH University of Krakow

IFDEPS 2024

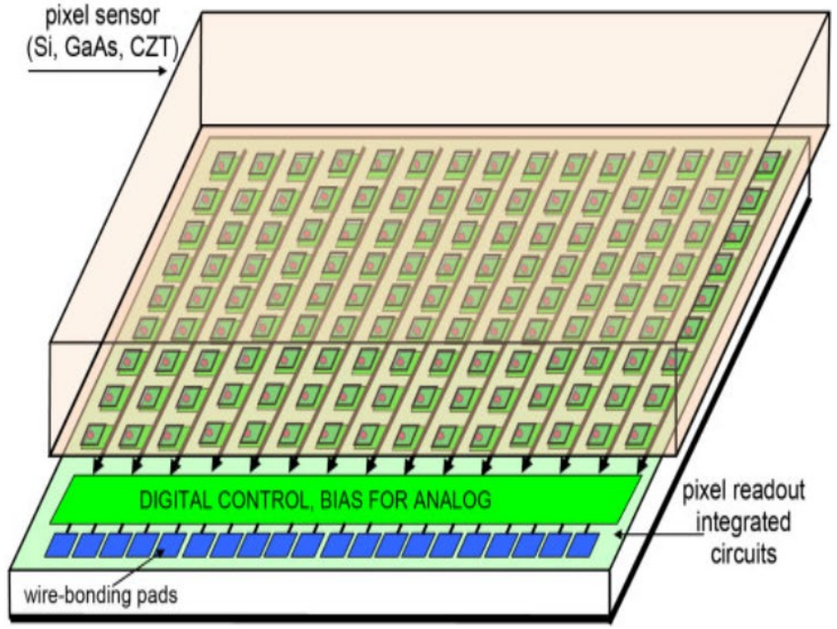
International Forum on Detectors for Photon Science

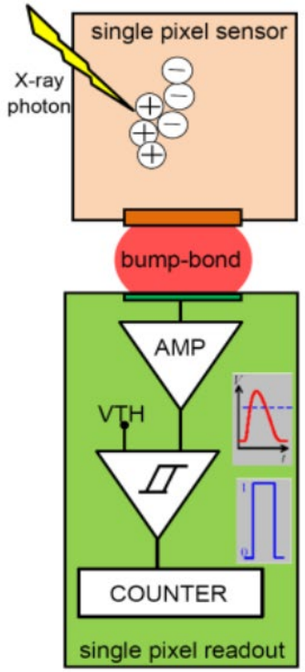
March 17-20, 2024

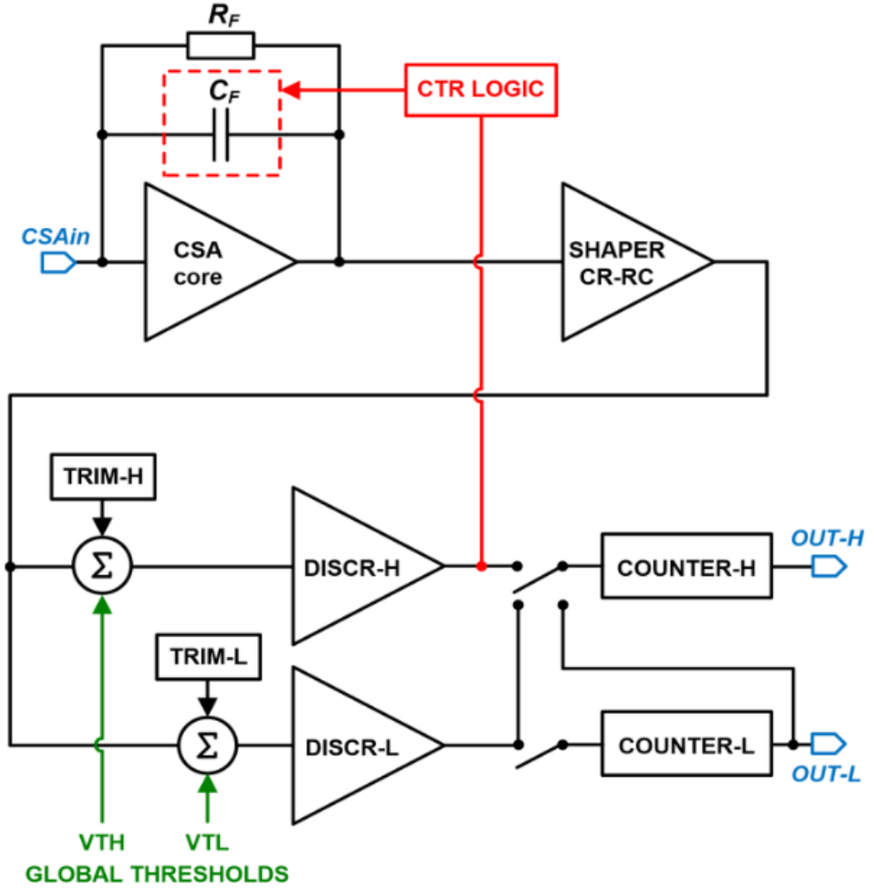
Outline

- Readout modes and design targets
- Increasing bit rate – serializer IP implementation
- Asynchronous center of gravity approximation
- 6-bit color imaging
- Increasing ADC resolution using neural network

Hybrid photon detectors

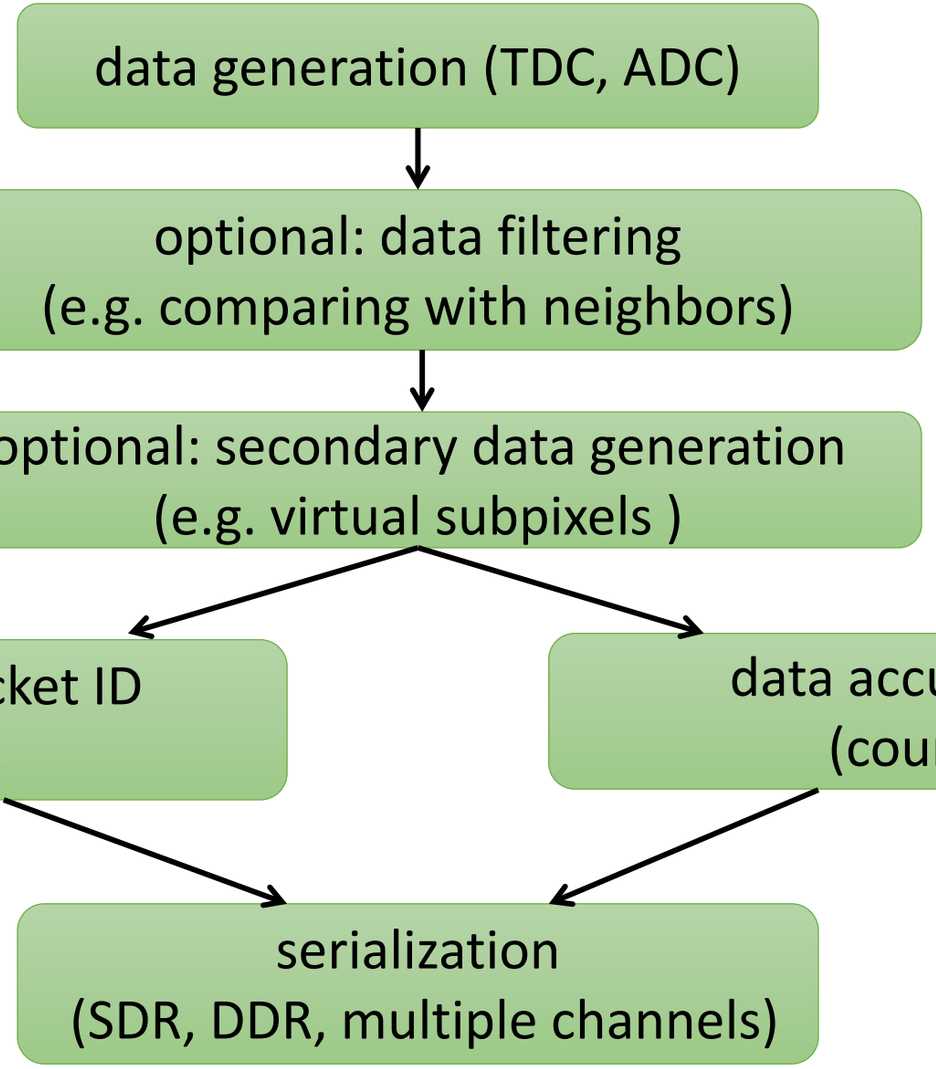






doi://10.1109/TCSI.2023.3241738

Pixelated ASICs readout modes



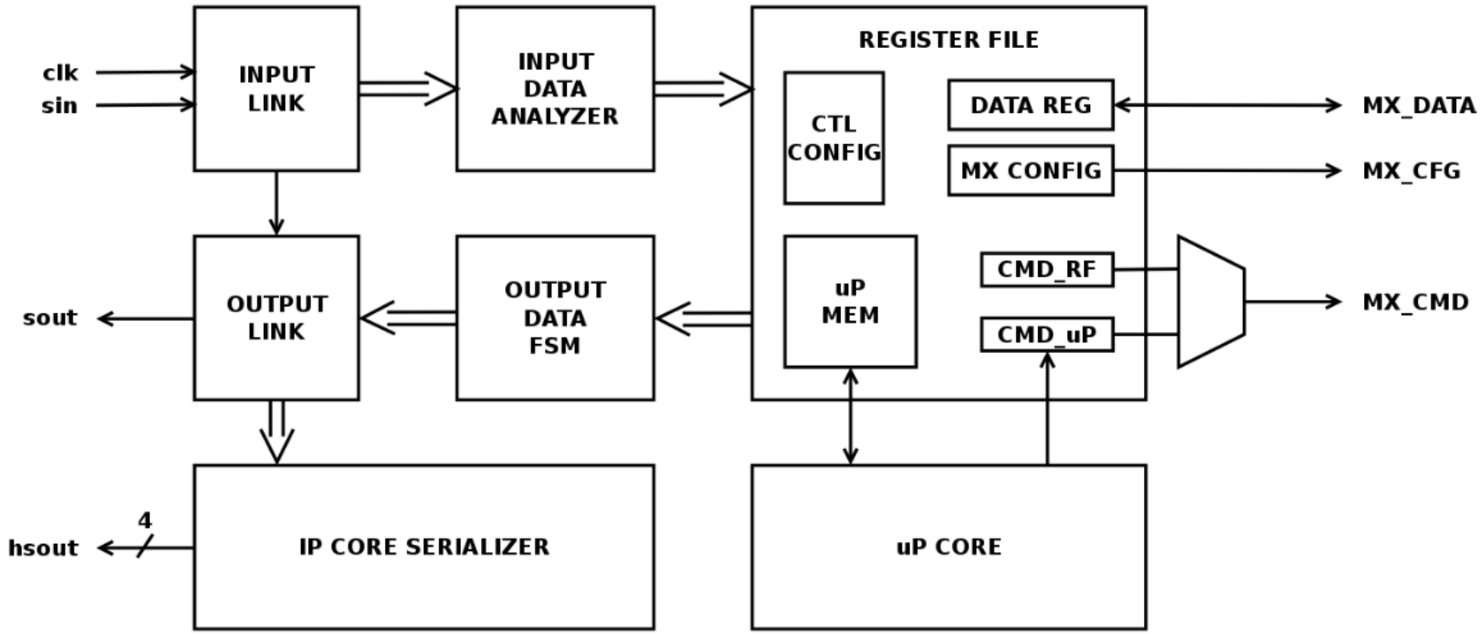
Single event mode

- bitrate proportional to event rate
- natural zero suppression
- targeting: timing or amplitude resolution, event rate

Data accumulation mode

- bitrate proportional to $\log_2$(event rate)
- targeting: count rate, number of bins/colors, frame rate

Pixel ASIC with integrated serializer IP



Instruction	Opcode	Description
LD	11dd dddd	**Load** - Load *CMD_µP* register (6 bit of data).
LDB	10dd dddd	**Load and branch** - Load *CMD_µP* (6 bit of data) ; if loop counter > 0 branch to the beginning of the current loop (PC = address from top of the branch address stack, decrement the loop counter value); if loop counter = 0 go out from current loop (PC = PC + 1, remove the loop counter value and the branch address from the stacks). This instruction should be used as the end of a loop.
LOOP	0010 dddd dddd dddd	**Loop start** - Saves a number of loop iteration (12 bit of data) on the loop counter stack and branch address (PC+2) on the branch address stack. This instruction should be used as the beginning of the loop.
BRA	01dd dddd	**Branch absolute** - Branch to address (6 bit of data). Maximum value 63.
WAITT	0001 xxxx	**Wait for the trigger** - Wait until trigger command.

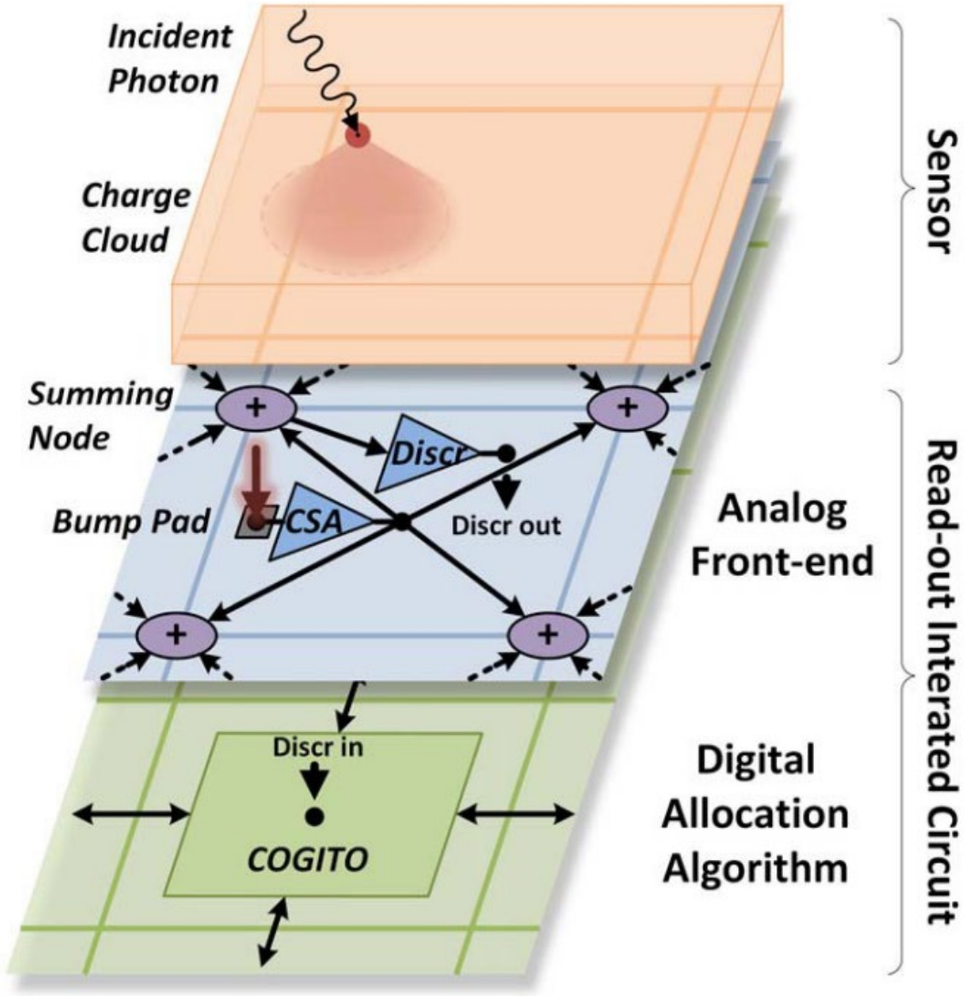
- technology: CMOS 40 nm
- base clock: 400 MHz
- **commercial serializer IP: 4 x 4 Gbps**
- complex IP constrains for implementation (SDC) and programming
- reasonable IP price

Pixel ASIC with integrated serializer IP

ASIC name	Number of output links	Operating frequency	Total output bit rate
Eiger [10]	32	100 MHz DDR	6.4 Gbps
Medipix2 [11]	32	100 MHz SDR	3.2 Gbps
Chromatix [12]	32	50 MHz SDR (200 MHz, untested)	1.6 Gbps
UFXC32k [8]	8	200 MHz DDR	3.2 Gbps
Timepix3 [13]	8	320 MHz DDR	5.1 Gbps
This work	4	4 GHz 8b10b encoded	12.8 Gbps

Design of matrix controller for hybrid pixel detectors. doi:10.23919/MIXDES.2018.8436909

Asynchronous approximation of a center of gravity

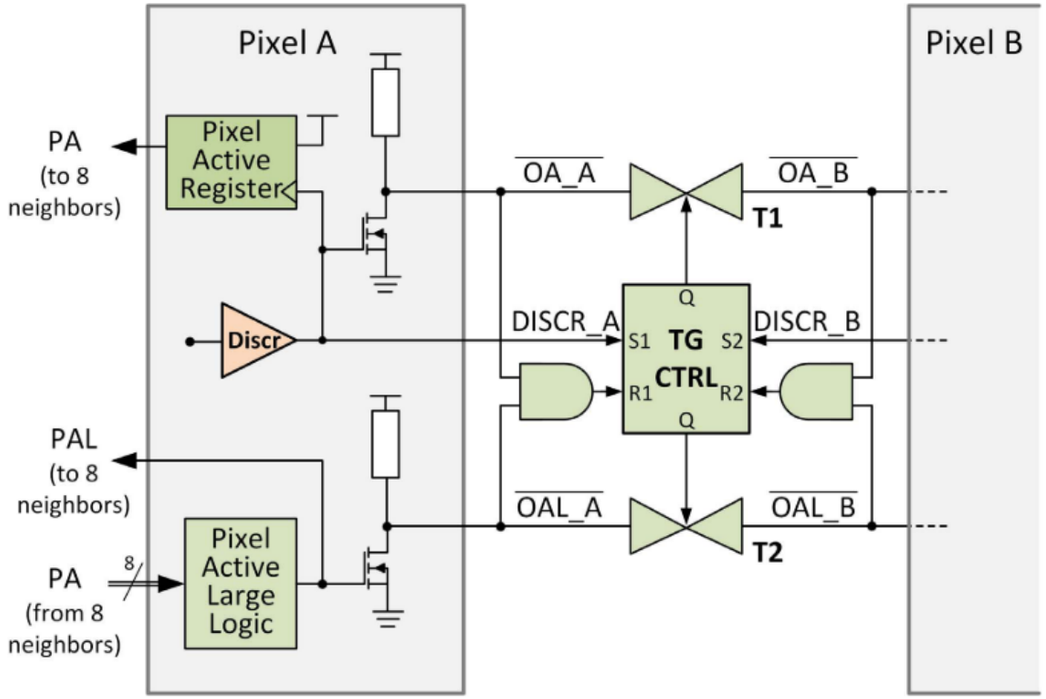


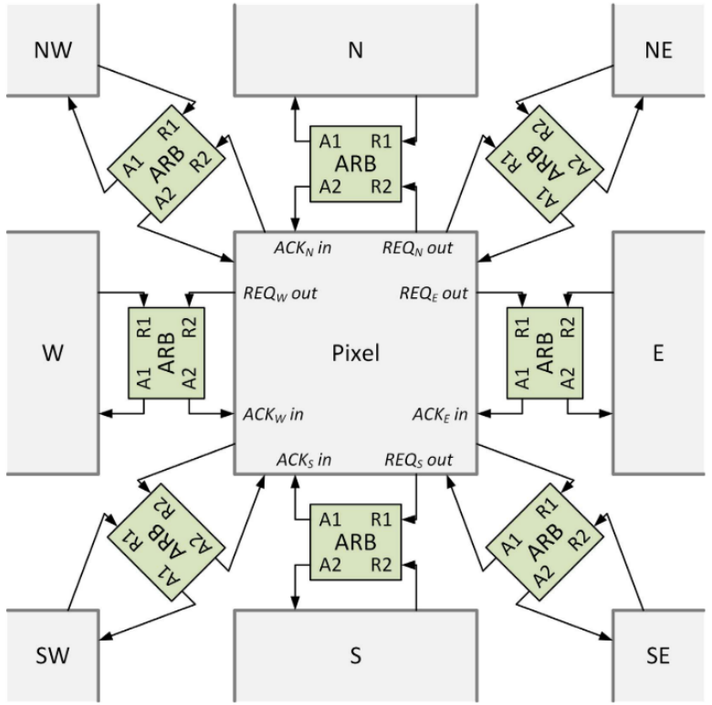
COGITO:

1. Sum analog signals from 4 pixels
2. Discriminate
3. Asynchronous digital processing to estimate COG.

Asynchronous Approximation of a Center of Gravity for Pixel Detectors' Readout Circuits. doi://10.1109/JSSC.2018.2793530

Asynchronous approximation of a center of gravity

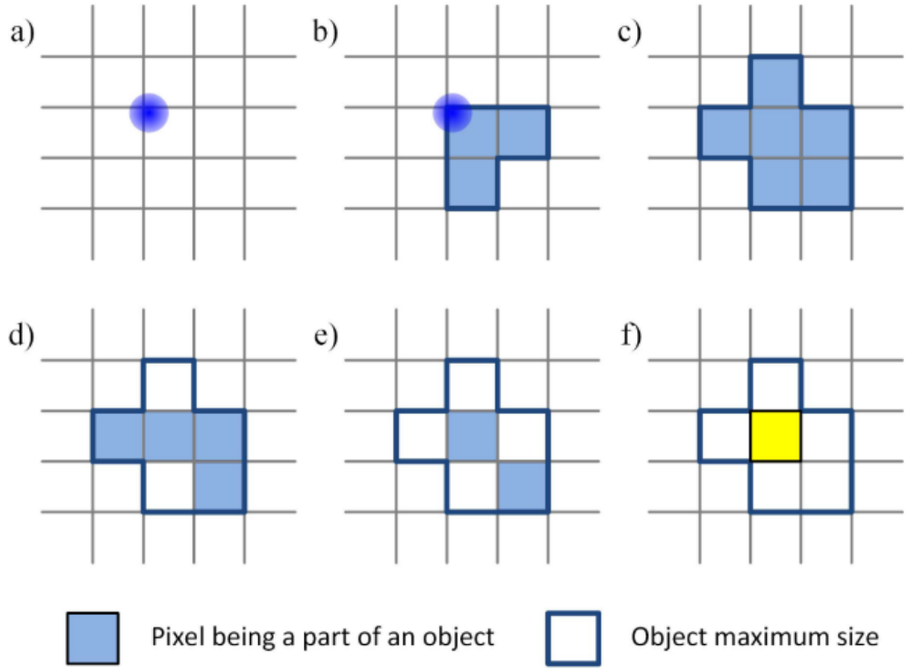




COGITO phases:

1. Expand
2. Shrink to 2x2
3. Select the winner

Asynchronous approximation of a center of gravity



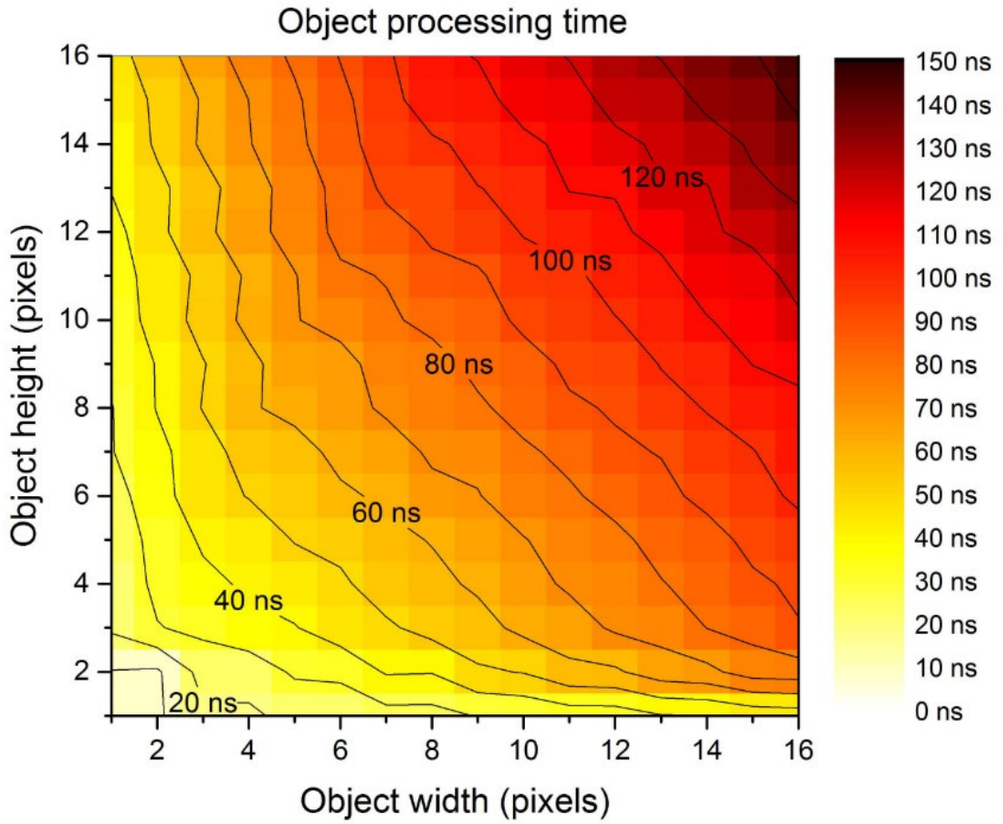
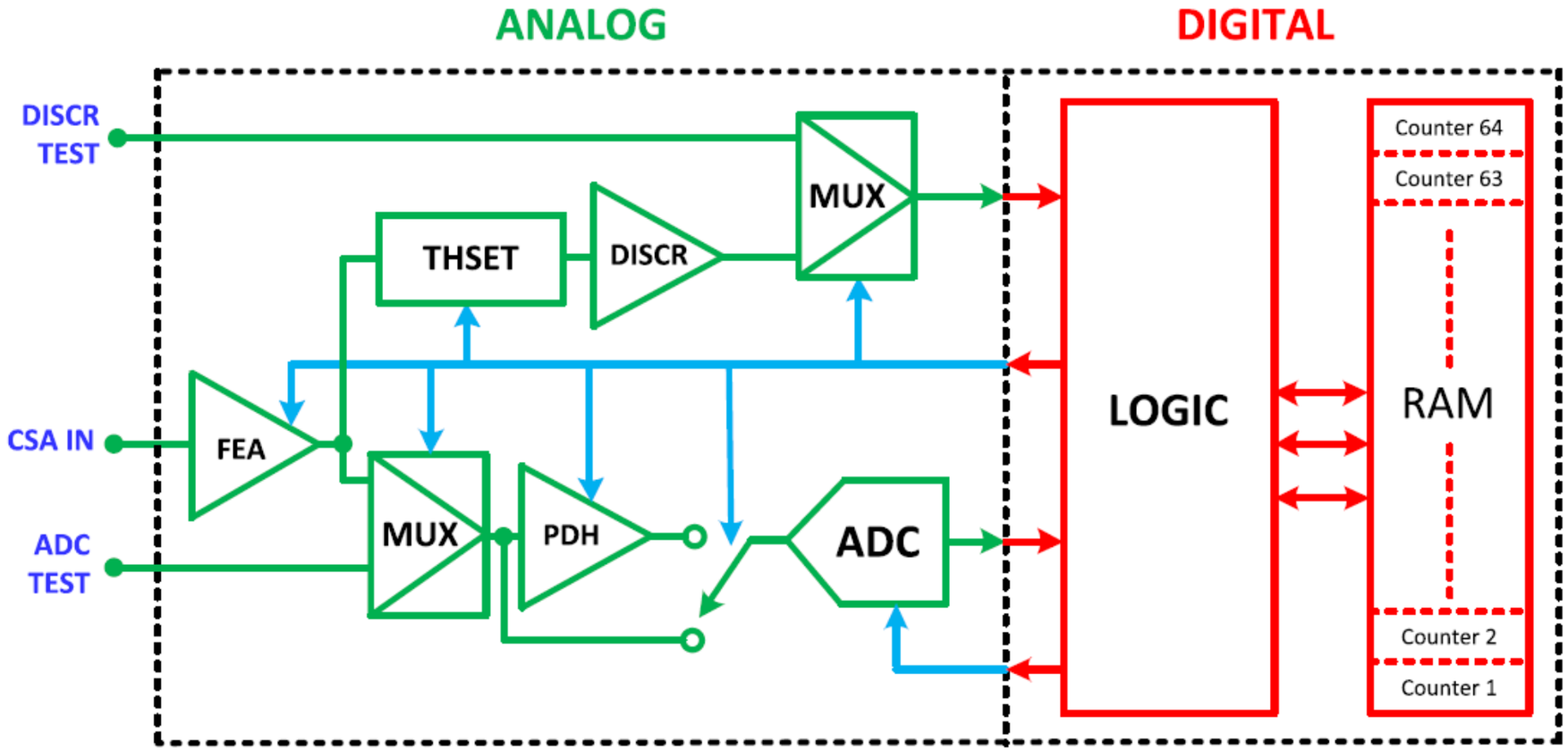


Fig. 12. Example of the algorithm operation. (a) Occurrence of an e (b) start of the maximization phase, (c) final object, (d) minimization phase, (e) end of the minimization phase, and (f) pixel estimating the center of gravity found.

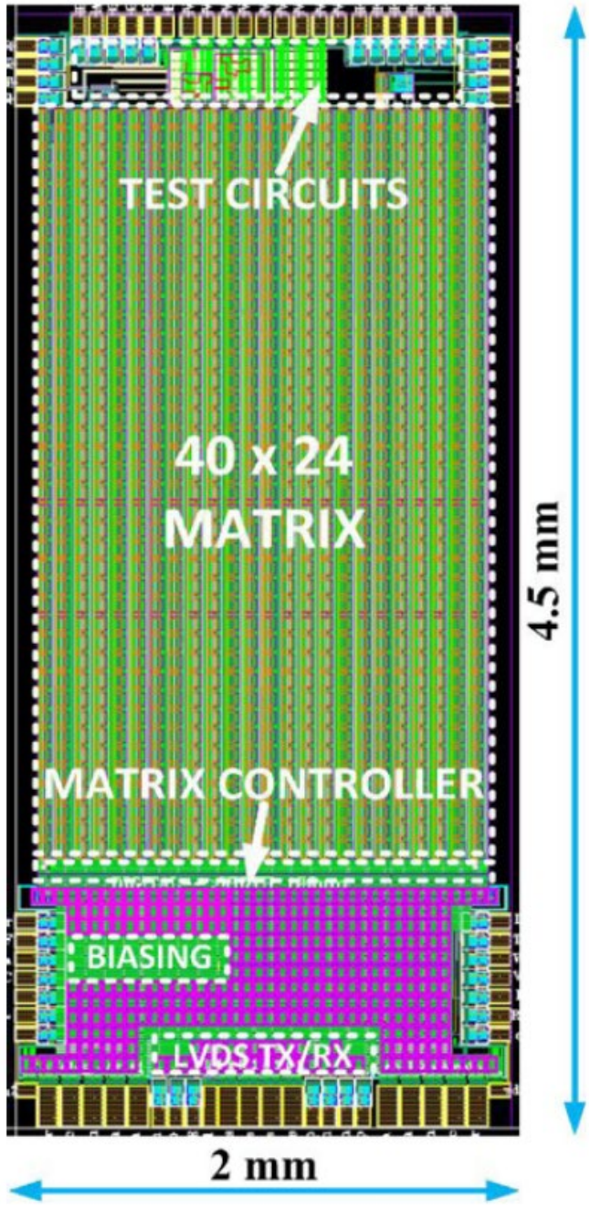
Chip produced in GF 55 nm. 16 x 16 pixels of 50 um pitch.

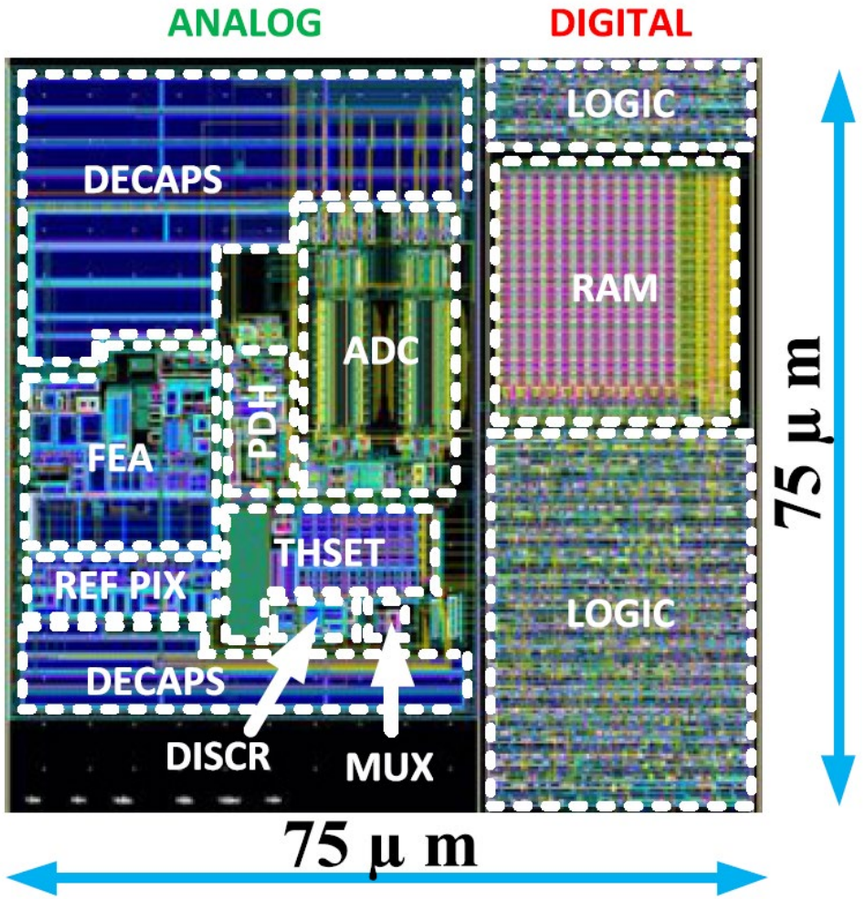
6-bit color imaging

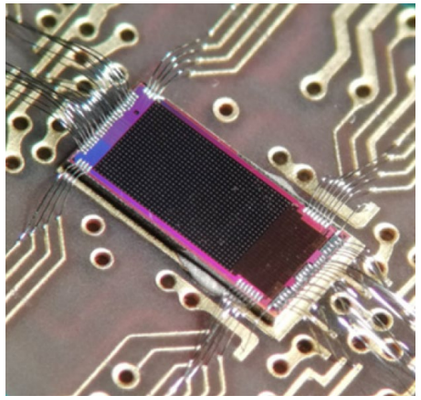


- technology: CMOS 40 nm
- 40 × 24 = 960 pixels
- 6-bit SAR ADC
- 64 × 12-bit RAM (= 64 counters, 12-bit each)
- read – increment – write RAM operation

- 22 clock cycles for pulse processing (SAR + RAM)
- 200 MHz clock frequency
- 64 × 12 = 768 bits / pixel / frame
- 3.7 ms full readout time

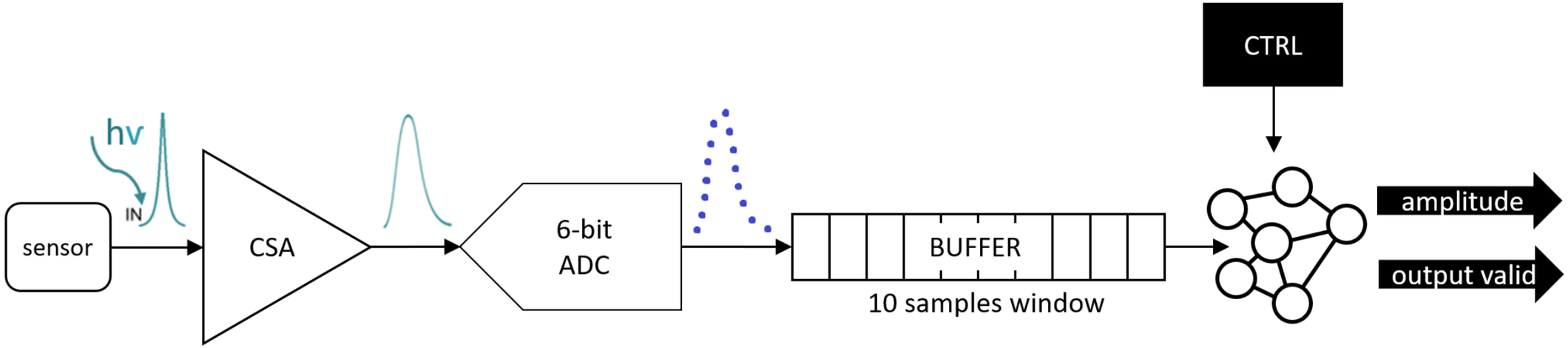


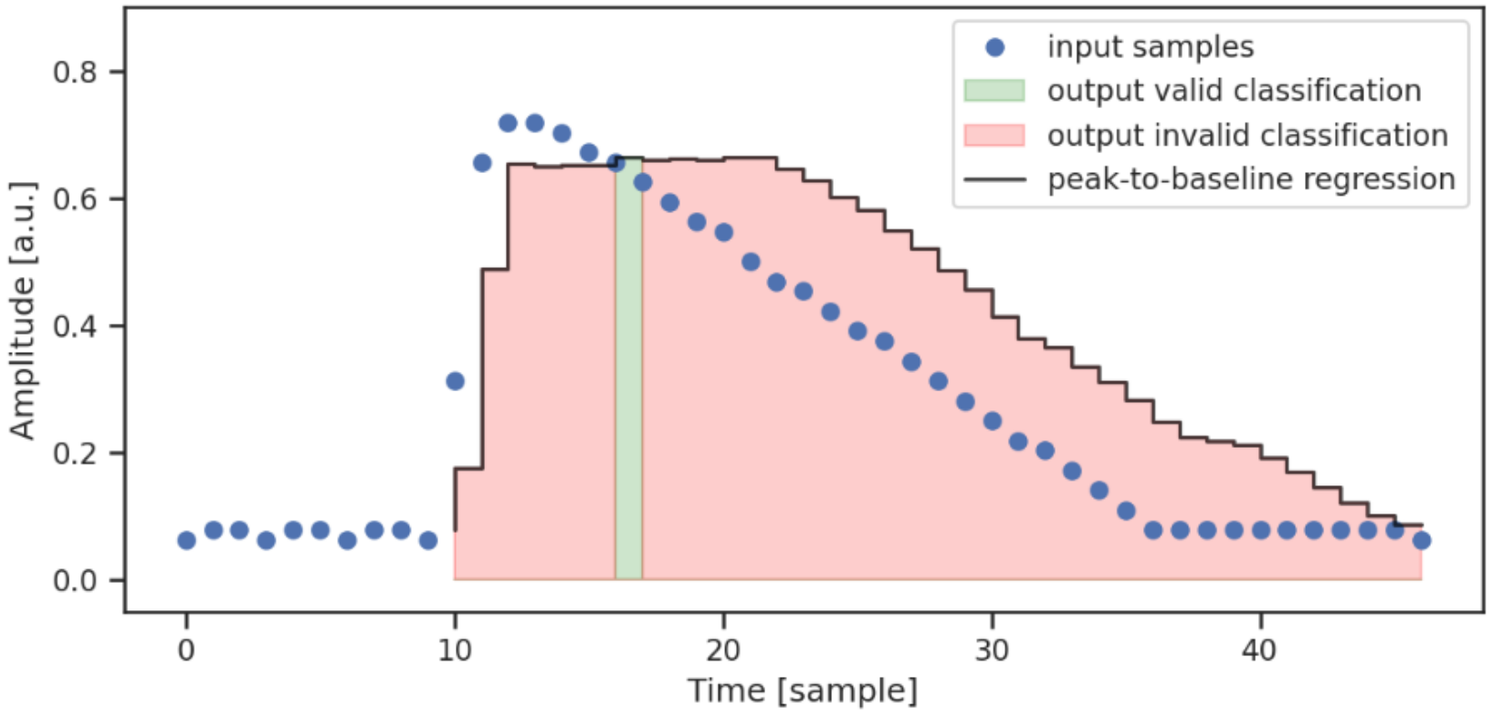




RAM size: 30 um x 30 um

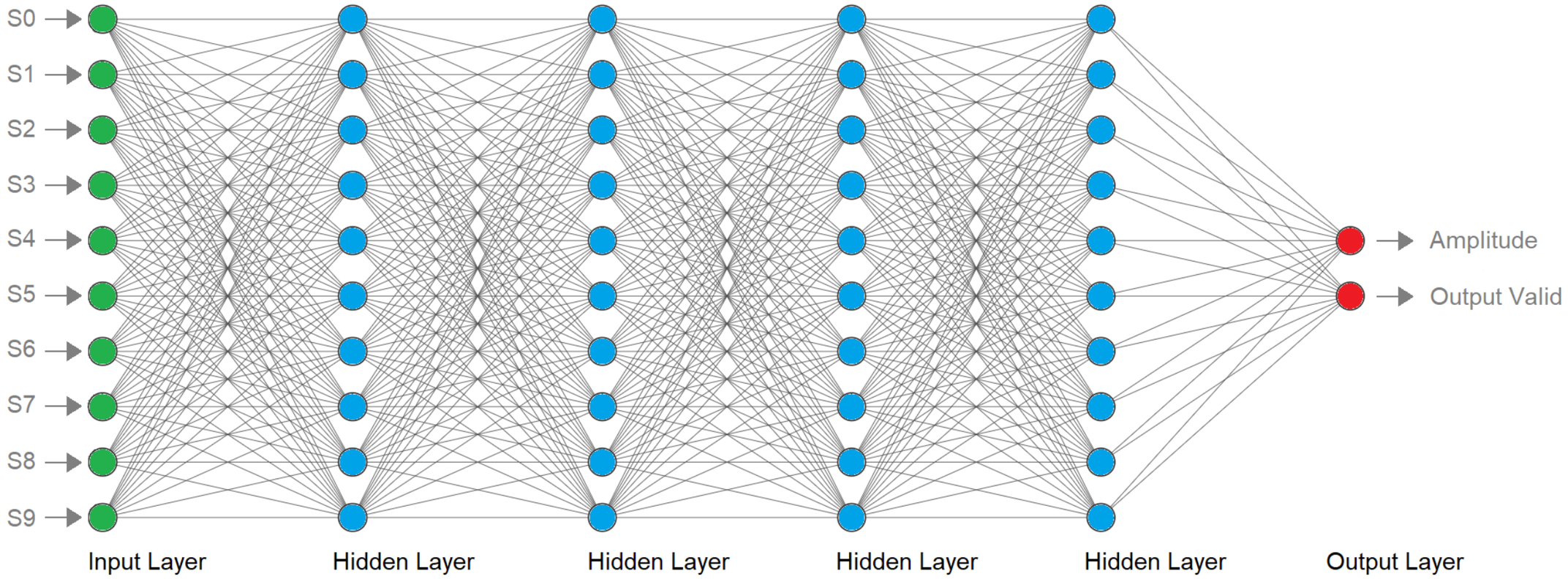
NN increased amplitude measurement precision





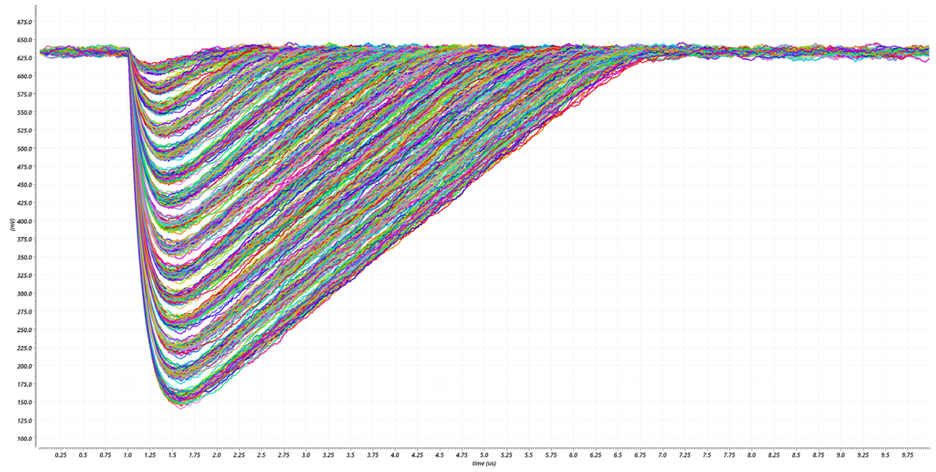
Tools used: Tensorflow, QKeras

Architecture: Multi-Layer Perceptron, 4 hidden layers, 420 weights



Training database

Spice simulated pulses

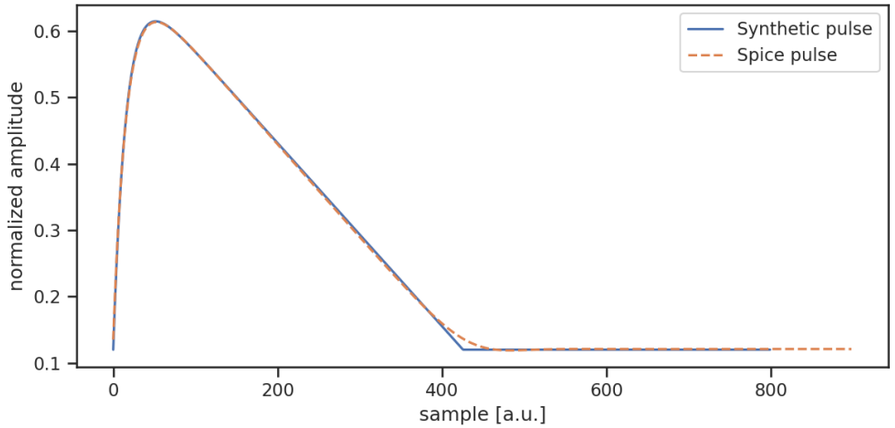


Data extraction

pulses

noise

Training database



- Normalized pulses amplitude (0;1)
- Unique pulses database (296 906 test vectors)
- Noise level: sigma (0;0.02), where 0.02 corresponds to ~100 e- ENC

Results – HDL ANN tests in FPGA

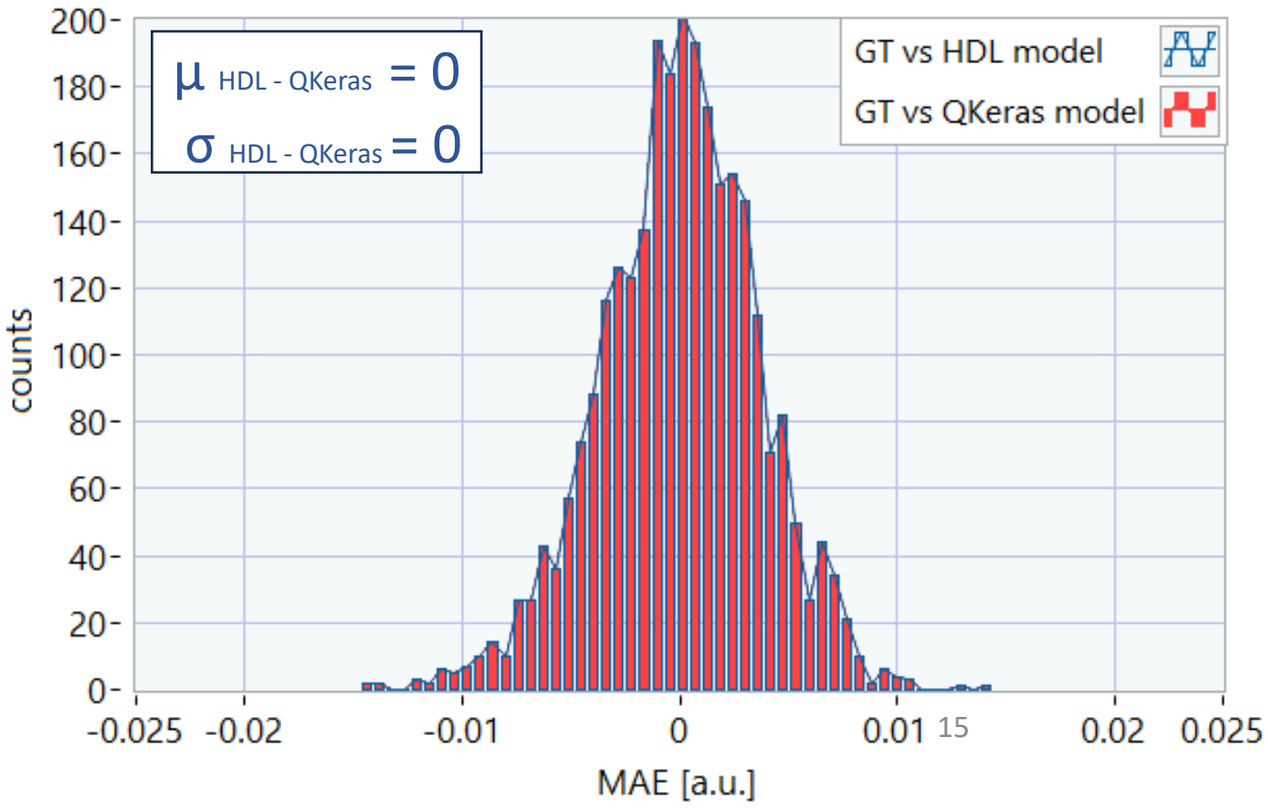
$$\mathrm{MAE} = \frac{\sum_{i=1}^{n} |y_i - x_i|}{n} = \frac{\sum_{i=1}^{n} |e_i|}{n}.$$

GT – Ground Truth – true pulse amplitude

1. Full reflection of HW limitations in Python ANN model →

2. Pulse detection: 100%

(noise 0.02, 10 000 test pulses)

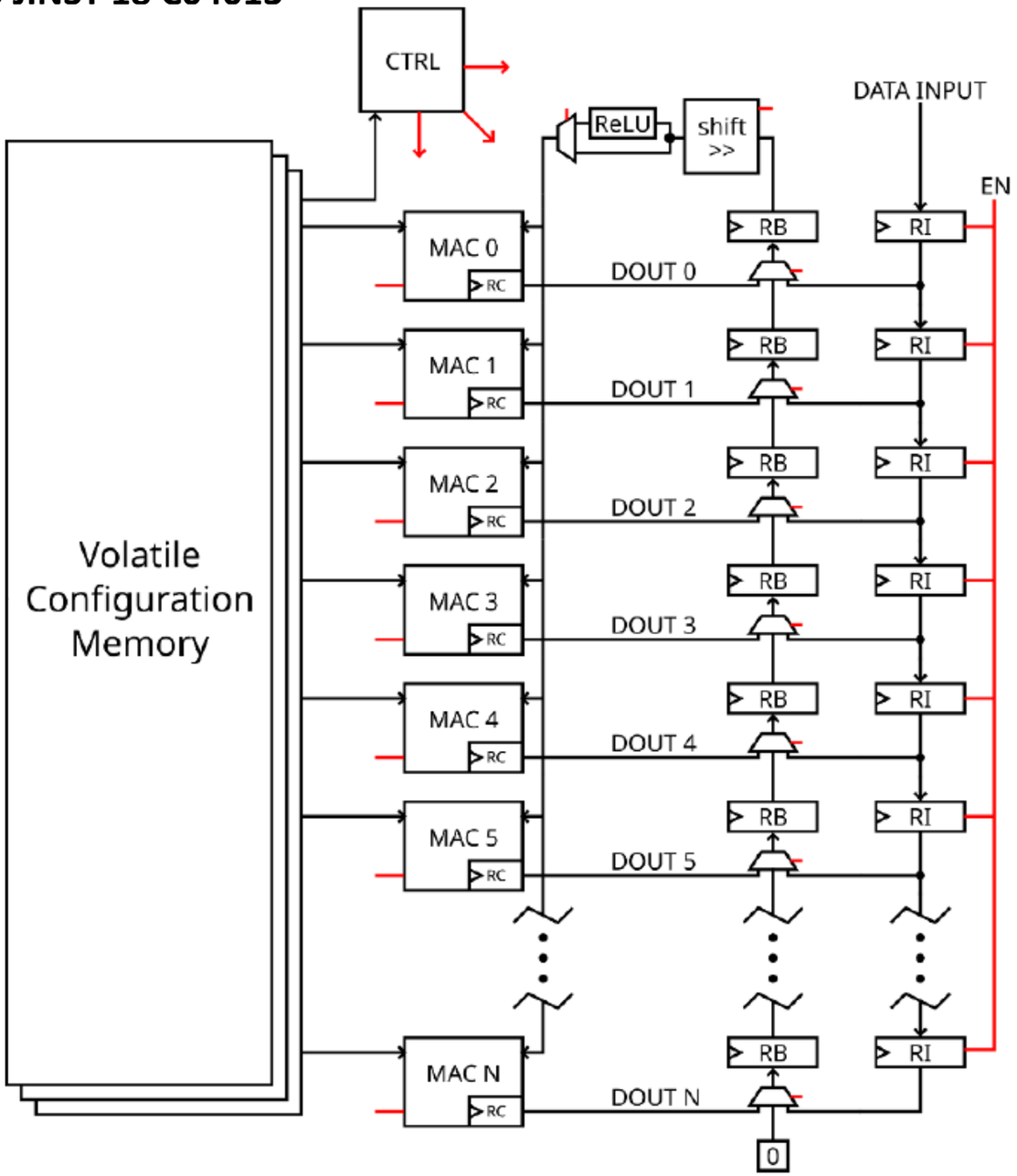


HDL ANN reconfigurable processor

HDL ANN parameters:

- architecture - MLP, 420 weights
- weights representation - FXP 12 bits
- accumulator's datatype - FXP 24 bits
- activation function - ReLU
- rounding method - truncate

HW limitations were reflected in Python ANN training (modified QKeras lib, anti-overflow monitoring, limited datatype) to mirror hardware behavior as closely as possible.

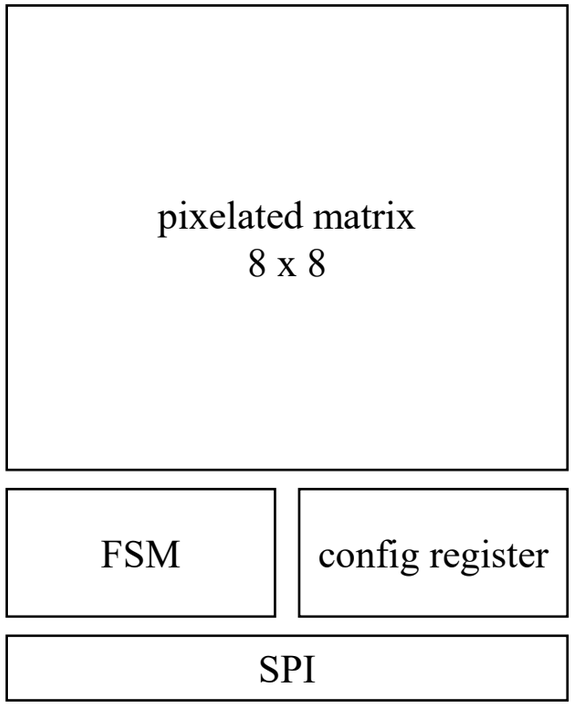


IntelPixel

- CMOS 28 nm technology
- chip size: 6.0 mm^2
- pixel size: 200 µm pitch
- in-pixel ANN

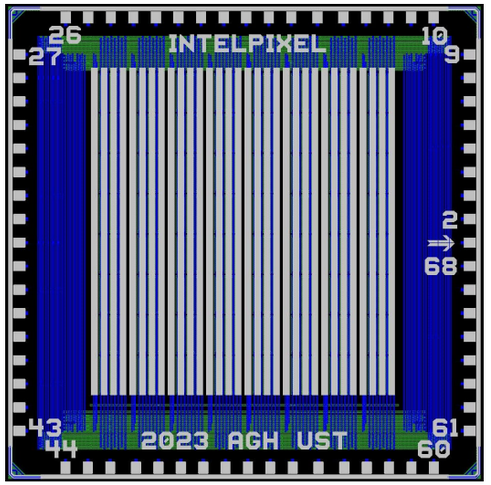
expected:
- middle of December 2023

IC scheme

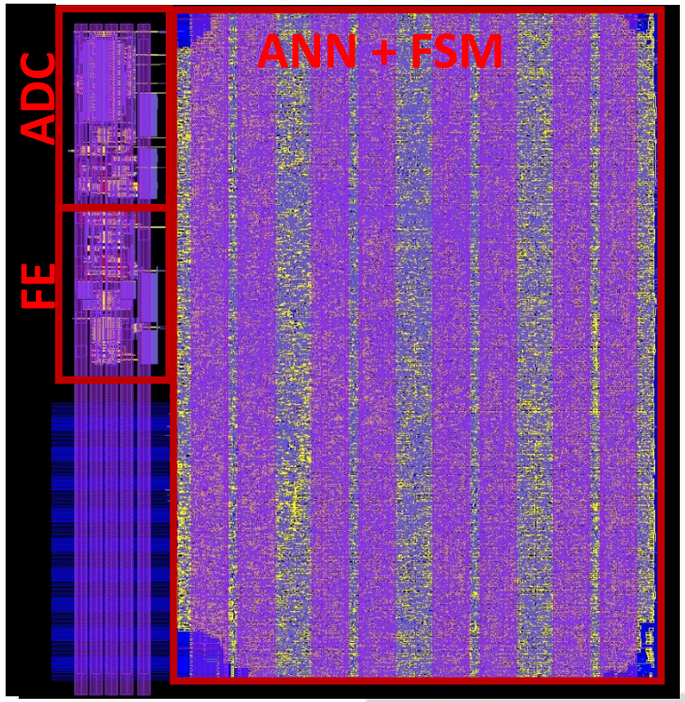


IC top

2.45 mm



pixel top



Unit	Gates	More details
Per chip	2.1M + 2k	1.3M P-type, 0.8 M N-type, ~2k outside pixels
Per pixel	33k	11k flip-flops and latches, 22k others

Conclusions

- Use fast serial links to transfer data from a readout ASIC – there are IP cores!
- Data preprocessing on chip is essential to limit the data rate. Neural networks can be helpful here.
- Implementation of data processing need more advance technology nodes (area/power/speed).
- The high prices of advance technology nodes will favor generic solutions, e.g., processors.

Acknowledgements
Paweł Gryboś
Bartosz Tutro
Kacper Urbański
Rafał Kłeczek
Piotr Kmon
Dominik Górni
Grzegorz Węgrzyn
Aleksandra Niedzielska
Krzysztof Sitko
Przemysław Drwal
Damian Kuźnar
Piotr Maj
Anna Kozioł
Piotr Otfinowski
Krzysztof Strzałka
Maciej Wielgosz
Grzegorz Deptuch

Backup

Europractice finfet prices can be found at:

https://europractice-ic.com/tsmc-university-finfet-program/#PricesTSMCfinfet