

Abstract No. citr363

Thermal Budget for Highest Free-Carrier Densities in 2D-doped *n*-type Si

P. Citrin, D. Muller, P. Northrup (Bell Labs) and H.-J. Gossmann (Agere)

Beamline(s): X15B

As silicon-based transistors in integrated circuits grow ever smaller, the concentration of charge carriers generated by the introduction of impurity atoms must steadily increase. Current technology is rapidly approaching the limit at which introducing additional impurity atoms ceases to generate additional charge carriers because the impurities form electrically inactive clusters. Realizing the practical limitations towards obtaining the highest free-carrier densities in *n*-type Si has been advanced this year through a study of highly 2D Sb-doped Si samples. As grown at low MBE temperature with δ -layer widths of ~ 15 Å, this system had been shown to exhibit electrical activities and dopant concentrations as high as $\sim 65\%$ and $\sim 10\%$, respectively. The effect of typical processing conditions on these 2D-doped samples was studied through rapid-thermal-annealing cycles of 600, 700, and 800°C and characterization with x-ray absorption, scanning transmission electron microscopy, and Hall measurements. Systematic decreases in electrical activity are observed (see figure) as a result of corresponding increases in Sb diffusion (this leads to expanded δ -layer widths and formation of electrically inactive Sb precipitates). Significantly, realistic processing temperatures of at least 700°C are still seen to yield carrier densities suitable for future 50 nm Si technologies.

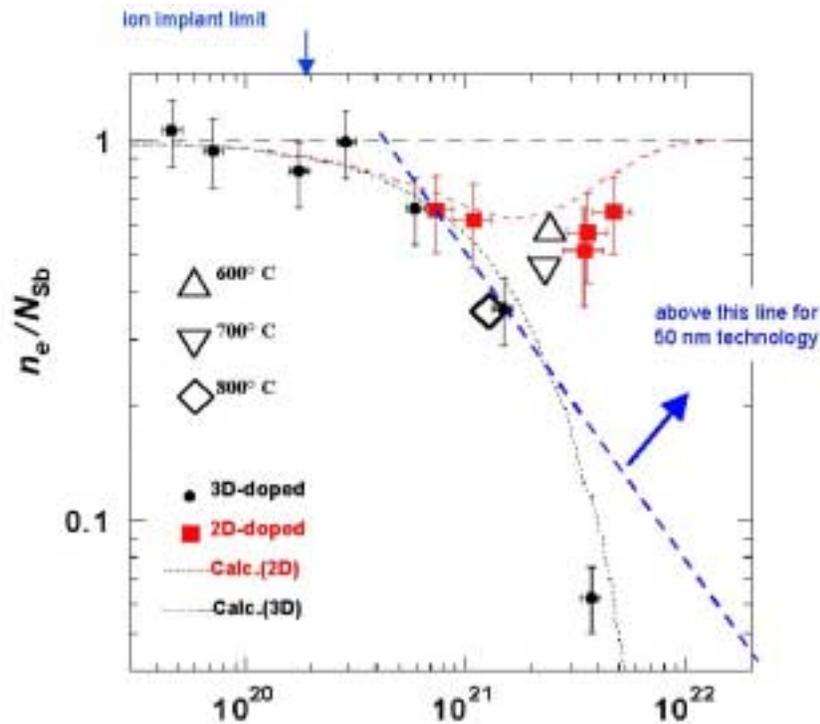


Figure 1. Electrical activity (expressed as per-cent fraction of free electron carriers per dopant atom) versus Sb dopant concentration in Si. The calculated electrical behavior for the bulk (3D) and δ -layer (2D) Sb-doped samples comes from D. J. Chadi et al., Phys. Rev. Lett. **79**, 4834 (1997) and P. H. Citrin et al., Phys. Rev. Lett. **83**, 3234 (1999), respectively.