

A BUNCH TO BUCKET PHASE DETECTOR USING DIGITAL RECEIVER TECHNOLOGY*

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Abstract*

Transferring high-speed digital signals to a Digital Signal Processor is limited by the IO bandwidth of the DSP. A digital receiver circuit is used to translate high frequency RF signals to base-band. The translated output frequency is close to DC and the data rate can be reduced, by decimation, before transfer to the DSP. By translating both the longitudinal beam (bunch) and RF cavity pickups (bucket) to DC, a DSP can be used to measure their relative phase angle. The result can be used as an error signal in a beam control servo loop and any phase differences can be compensated.

INTRODUCTION

The AGS Booster is designed to accelerate protons and ions injected from a LINAC and tandem Van de Graff respectively. Once injected the beams are captured in the RF bucket, accelerated and extracted to the AGS. While the motion of hadrons in the RF potential well is inherently stable it is not strongly damped [1]. Damping coherent synchrotron oscillations is the job of the phase loop and the phase detector is at the heart of this system.

Advances in speed and complexity of digital integrated circuits have changed the basic building blocks of Low Level RF design. Digital Signal Processors are commonly used in feedback loops as well as high speed Analog to Digital Converters. A bottleneck exists though in the transfer of data from high speed ADC to the computational units inside the DSP chip.

Digital receiver circuits take advantage of the relatively narrow bandwidth of the beam signal required by a phase detector. The center of mass of the bunch can be defined by the single spectral component of the beam at the RF frequency. If this spectral component is shifted to DC and band limited the sample rate can be significantly reduced. This technique will in turn reduce the IO bandwidth requirements of the DSP by shifting the burden to a dedicated signal processor designed to handle this high-speed data.

Off-the-shelf digital receivers have some distinct tradeoffs that will be discussed as well as how these tradeoffs may be eliminated by designing a custom receiver in an FPGA.

BASIC BLOCK DIAGRAM OF A DIGITAL RECEIVER

The block diagram in figure 1 is typical of a receiver channel. An RF input is passed through an anti-alias filter

to remove frequencies above the Nyquist limit. The signal is then digitized and the data stream enters the receiver IC. A complex Numerically Controlled Oscillator generates the Local Oscillator frequency for translation. The output of the NCO and the ADC are digitally multiplied (mixed). Two stages of filtering remove the unwanted sidebands and reduce the output sample rate. The circuit outputs complex base-band data at the decimated rate.

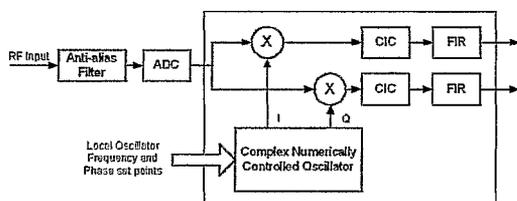


FIGURE 1: Block diagram of a digital receiver channel.

The NCO frequency set point can change dynamically as well as the phase offset of the channel. The order and decimation rate of the Cascaded Integrating Comb filter [2] can be adjusted and the Finite Impulse Response Filter coefficients can be downloaded. In addition to these basic structures Automatic Gain Control circuitry and a Cartesian to polar coordinate transform are provided.

PHASE DETECTOR CONFIGURATION

To implement a phase detector with digital receivers two signals need to be derived: the phase of the beam which is extracted from the wall current monitor and the phase of the RF potential well which is derived from the vector sum of the accelerating stations.

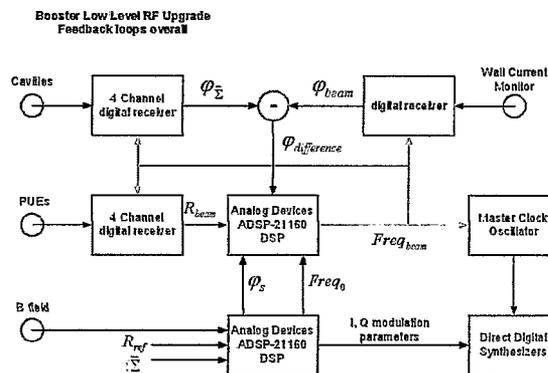


FIGURE 2: Block diagram of the phase detector configuration.

A four channel digital receiver will be used in the Booster Low Level RF design to measure the vector sum

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of the four accelerating stations. Each channel has individual phase control to compensate for the physical location of the cavity on the ring. The effective voltage gain received by the beam on each turn is the sum of the individual cavities rotated according to their physical position. The phase of the vector sum varies relative to the low level RF drive due to dynamic tuning of the ferrite loaded cavities and characteristics of the amplifier chain. This receiver will measure the deviation of the vector sum from the reference oscillator phase.

The phase of the beam is measured with one channel of a four channel digital receiver. The longitudinal beam pick-up is a resistive wall gap detector or wall current monitor this signal is brought out from the ring on high quality 7/8-inch semi-rigid coaxial cable. The coaxial cable preserves the bandwidth and reduces loss of signal amplitude. The beam receiver requires a large dynamic range to work with beam intensities from as low as 10^8 and as high as 3×10^{13} charges per pulse. The front-end electronics and processing gain give the receiver a dynamic range of ~ 90 db.

The two phase measurements are taken with respect to a reference oscillator the frequency of which is updated by feedback from the beam. Any deviation at the output of the receiver from DC will be corrected by feedback through the master oscillator and slave DDS chain (FIGURE 2). To ensure a consistent measurement the NCO in both receiver circuits and the master oscillator are updated simultaneously using an external synch pulse.

HARDWARE IMPLEMENTATION

The first prototype circuit has been built using an Intersil ISL5216 [4] digital receiver IC (figure 3). This chip offers several features:

- 95 MSPS input sample rate
- Four independent receiver channels
- 32-Bit numerically controlled oscillator
- Digital Automatic Gain Control
- 16-Bit uP interface

The output format can be phase, magnitude, I and Q, or frequency and the AGC circuitry boasts a 96db range. The increment value in the phase accumulator of the internal NCO can be updated with an external pulse, allowing all NCOs in the system to be updated synchronously.

The front-end circuit includes a low pass anti-alias filter followed by variable gain amplifier, RF transformer and an Analog Devices AD6644 A to D converter. The filter has been selected to pass only the highest bunch frequency in the Booster approximately 5MHz. The variable gain amplifier was added to ensure that low amplitude signals could be boosted to excite the most significant bits of the ADC. An RF transformer couples the AGC Amplifier to the A to D converter differentially and the outputs of the four converters connect in parallel to the Intersil receiver.

The circuit board is a modular daughter card designed to mate with a DSP carrier board also built at Brookhaven [3]. To communicate with the carrier board an Altera PLD

interfaces the Intersil receiver chip to the DSP global bus. The DSP global bus can transfer data at 40MHz, this is sufficient for updating the dynamic parameters of the receiver in real time as well as reading the output data.

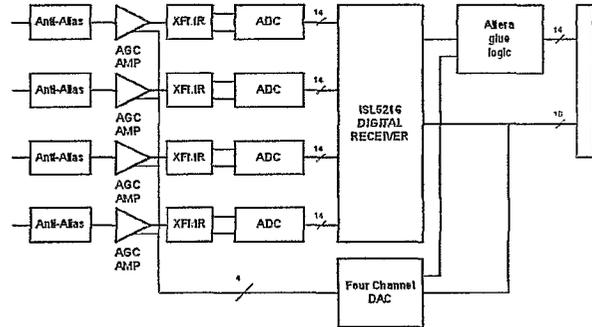


FIGURE 3: Intersil four-channel receiver block diagram.

PERFORMANCE

The prototype receiver has shown a usable dynamic range of 90db. Signal amplitudes of +10dbm down to -80 dbm were successfully measured. The AGC circuit maintained the amplitude of the output signal to within 6db over this range. Lowering the amplitude of the input signal further caused the AGC circuit to go out of regulation.

Out of band frequency rejection agreed with the data in the Intersil documentation [4]. During all tests the filter used was a 7-tap half-band FIR (HBF1) the coefficients of which are stored in Read Only Memory on the receiver IC. This filter provides rejection of approximately -120 db at $F_s/2$ and a 3db point at $F_s/4$. Other filters are also available with coefficients stored in ROM. These filters have a faster roll-off at the expense of more taps and a longer delay.

Group delay through the circuit is critical to using this technology in a feedback loop. To calculate the delay each stage must be evaluated. This is best shown by example.

Example delay calculation

We will design a system that has an input sample rate of 40MHz and an output rate of 1MHz. In the CIC filter we will decimate by twenty and then decimate by two in the output FIR Filter. The CIC filter has six taps therefore 3.5 clock cycles to the middle tap. With the decimation set to twenty the delay through this section will be: $3.5 \times 20 = 70$ clock cycles. We follow that with a 7-tap half band decimating filter with a decimation rate of 2. The delay due to the number of taps is four clock cycles we need two more clock cycles for data read and writes. The decimation is two and the sample rate has been reduced in the CIC filter by a factor of twenty this results in: $(4 + 2) \times 2 \times 20 = 240$ clock cycles. Finally pipeline delays and delays through the AGC circuit contribute 30 to 50 extra clock cycles. The total delay with this

arrangement is $70 + 240 + 50 = 360$ clock cycles or $9\mu s$ through the device.

Figure 4 shows an FFT of the data returned by the device with the input signal set to 10kHz offset carrier and an amplitude of -60dbm .

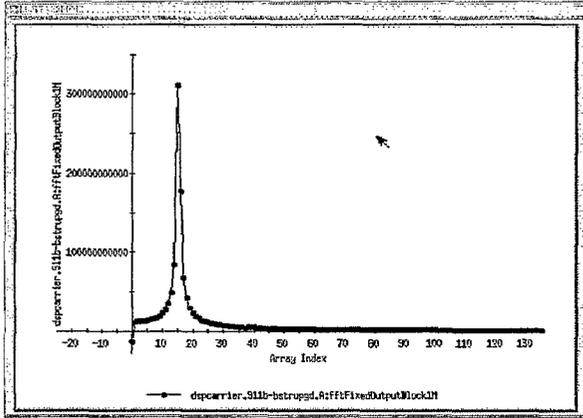


FIGURE 4: Frequency spectrum of a signal 10kHz offset carrier at -60dbm .

INTEGRATION

The digital receiver requires a support system that includes both hardware and software. A program provided by the manufacturer is used to define the internal registers of the receiver IC. After a configuration has been defined another program has been developed to translate the register description file into a format that can be used by the DSP to configure the receiver. This software has been tested successfully. In addition to DSP control software an application is being developed to read measurement data generated by the receiver and display these results graphically. The graph in figure 4 shows the output of this program.

The topology of the Booster beam control system uses several DSP carrier boards connected by high-speed data links to compartmentalize system functions. To test the receiver in-system a program running on another carrier card will calculate the beam frequency as a function of dipole field strength. This data stream is used to update the local oscillator in the receivers. This code has been developed and tested. Once the frequency program and receiver control program have been integrated measurements with beam can commence.

CONCLUSIONS

The prototype receiver has produced the expected results and finding an optimum filtering solution with minimal delay is ongoing. The immediate goal is to integrate the receiver into the Booster Low Level RF system. Once integrated, the booster RF frequency sweep

can be used to drive the receiver LO and beam signals can be observed during the acceleration cycle.

In addition to measuring the bunch to bucket phase this receiver will also be used to measure the radial position of the beam. The normalized beam position will be detected using two receiver channels connected to the horizontal plates of a pick-up electrode. This will provide the radial position input to the LLRF feedback loops [5].

While the Intersil device has a high level of integration the data path is not optimal for the DSP used in our system. In order to take full advantage of the high speed data links available on the Analog Devices ADSP-21160 DSP an FPGA based receiver is being designed. This design will have a full 32-bit interface to the host DSP for changing dynamic variables and result data will be passed to the DSP using a pair of high-speed Link-Ports [6].

In addition to improvements to the IO structure the FPGA based design will use a single phase accumulator for the four channels reducing the complexity of data transfer and synchronization. The current design requires three write cycles to update the frequency or phase of each channel. Reading the measured data from the receiver requires two read cycles per parameter. This overhead will limit the useful bandwidth of the device.

Digital receiver technology along with digital beam control systems will greatly improve the flexibility and reliability of this and future accelerators.

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