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A LOW NOISE RF SOURCE FOR RHIC*

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Abstract

The Relativistic Heavy Ion Collider (RHIC) requires a low noise rf source to ensure that beam lifetime during a store is not limited by the rf system. The beam is particularly sensitive to noise from power line harmonics. Additionally, the rf source must be flexible enough to handle the frequency jump required for rebucketing (transferring bunches from the acceleration to the storage rf systems). This paper will describe the design of a Direct Digital Synthesizer (DDS) based system that provides both the noise performance and the flexibility required.

INTRODUCTION

The low level rf system for RHIC must provide drive to the accelerating cavities at a harmonic number of 360, the storage cavities at a harmonic number of 2520, a Landau cavity at a harmonic number of 2563 as well as a local oscillator signal at a harmonic number of 480 with a 10.7 MHz offset used for processing radial position signals. In addition, outputs at several other harmonics of the revolution frequency are generated to provide timing to instrumentation. Maximizing beam lifetime during a store requires that rf noise be kept to a minimum. One added constraint is that the process of transferring beam from the accelerating system to the storage system requires some delicate frequency manipulations [1]. In order to generate all the frequencies required and still have the flexibility required for rebucketing, a system was designed using a master DDS to provide an output signal at a harmonic of the revolution frequency that is used to drive the clock of all other DDSs. Thus, only the master DDS needs to have its data continuously updated throughout the acceleration cycle. This ensures that the outputs of all the DDSs are phase locked since the only thing changing is their common clock. A block diagram of this system is shown in Figure 1. As an added benefit of this configuration, it is extremely easy to add new output signals at different harmonics as the need arises.

IMPLEMENTATION

Crystal Oscillator

Since the output phase noise of a DDS is primarily determined by the noise of the reference clock driving it [2], the noise of all the DDS outputs is determined by the noise of the 300 MHz oscillator. The 300 MHz signal is generated from a 5 MHz crystal oscillator with frequency multipliers used to provide a 300MHz output. It was

implemented in this manner because crystals at 5MHz can be made with much lower phase noise than higher frequency crystals. Even allowing for the frequency multipliers, it was determined that this method would provide the lowest phase noise clock signal to the master DDS. A plot of the phase noise of the 300 MHz oscillator (measured with an Agilent E4440) is shown in Figure 2. An added benefit of starting with the 5 MHz oscillator is that it was very easy to provide a 10 MHz reference signal, locked to the main system clock, to all the instrumentation.

DDS Outputs

The DDS used was the Analog Devices AD9854 which has a maximum clock frequency of 300 MHz. Since the practical limit on the output frequency of a DDS is 40% of the clock frequency (due to filtering requirements), there was no way to use the fundamental output to provide the signals required at 200 MHz. The solution to this problem was to take advantage of the alias signals inherently produced in the output spectrum of a DDS as a result of the sampling process. In order to generate the higher frequency signals, one of the alias signals from the DDS was used. This method is only useful because the reference clock to the DDS is itself a harmonic of the revolution frequency. By using the first alias signal above the clock, the output frequency for the storage cavities is given by equation 1:

$$f_{\text{STORE}} = f_{\text{CLK}} + f_{\text{FUNDAMENTAL}} \quad (1)$$

Since the clock frequency is $2048 \times f_{\text{REV}}$, setting the fundamental DDS output to a harmonic of 472 yields the desired results as shown in equation 2:

$$f_{\text{STORE}} = 2048 \times f_{\text{REV}} + 472 \times f_{\text{REV}} = 2520 \times f_{\text{REV}} \quad (2)$$

One drawback to this solution is that the amplitude of the desired signal is greatly reduced relative to the fundamental output due to the inherent $\sin(x)/x$ amplitude roll off of DDS outputs. Therefore, a significant amount of gain is required (~30 dB in this case) to get the desired alias signal up to a useful level. To prevent the amplifiers from being driven into saturation, the fundamental output must be filtered out first. Careful consideration must be given to both the clock and fundamental frequencies used to ensure that the desired output is not too close to the null in the $\sin(x)/x$ response.

Power Supply Filter

Starting with a low noise oscillator was not the only requirement for providing a low noise rf source. Experience has shown that there were significant power line harmonics at 60, 120 and 180 Hz offsets from the carrier which were especially damaging as they are inside

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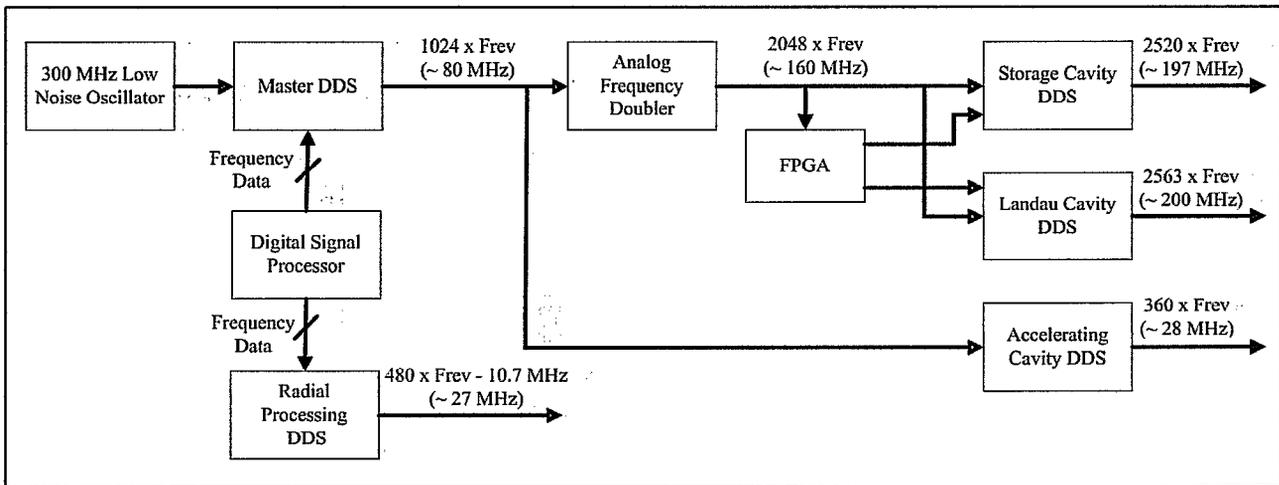


Figure 1. System Block Diagram

the band of synchrotron frequencies. In order to reduce this noise, the power for the DDSs is derived from high quality voltage regulators which were followed by active filters to minimize noise, specifically at the line harmonics [3]. A similar scheme is used to supply power to the 300 MHz oscillator.

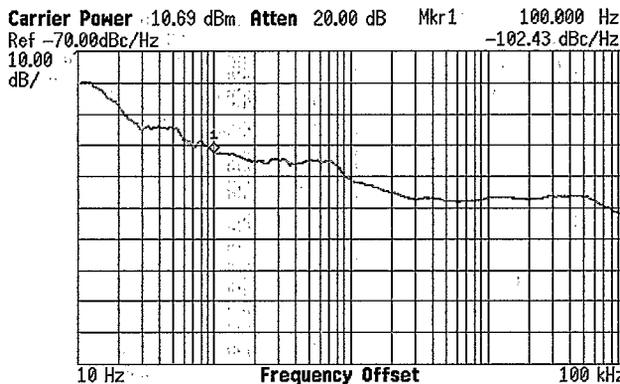


Figure 2. Phase noise of 300 MHz oscillator

RESULTS

A prototype system was installed in one of the RHIC rings during Run 3 and the results were immediately apparent. During a RHIC store there is always beam loss associated with Intra-Beam Scattering and possibly a contribution from rf noise as well. After installation of the prototype system there was a clear reduction in beam loss over the course of a store as a result of the decreased rf noise. Prior to the start of Run 4, new systems were installed for both rings, which allowed the use of the new 'frequency jump' rebucketing.

Signal Purity

The output spectrum of the storage cavity drive is shown in Figure 3 and Figure 4. In previous years, the storage cavities have been driven directly from an HP8644A signal generator and the output spectrum for that generator is shown for comparison in Figure 5. Figure 6 shows a plot of the phase noise of both the new storage

cavity drive and the HP8644A. While close in noise was important for beam loss considerations there was also an issue with noise further out that was inside the bandwidth of the power amplifier but outside the bandwidth of the cavity. This noise caused serious problems with heating of the rf windows. Earlier attempts to run the storage cavities with a step recovery diode driven by the accelerating system signal were unsuccessful because of this out of band noise problem. There were no problematic spurious lines in the spectrum with the new system and there was no increase in the measured temperature of the rf windows.

Rebucketing Frequency Manipulations

In order to accomplish the rebucketing process, the drive to the storage cavities is offset by several kilohertz to allow the cavities to be turned on without interacting with the beam. After all the cavities have been brought up to full voltage, a bunch rotation is started via modulation of the accelerating system voltage. When the bunches have rotated into the correct orientation, the frequency offset on the storage cavity drive is removed and the beam is captured in the storage system buckets. Clearly, the phase of the storage cavities with respect to the accelerating cavities must be correct when this happens. In order for the storage cavities to be properly phased with respect to

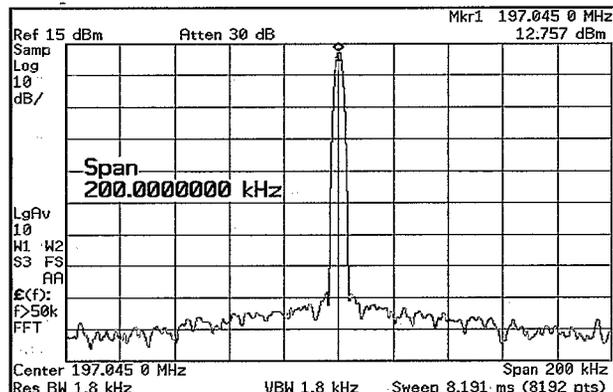


Figure 3. Storage Cavity Spectrum (200 kHz span)

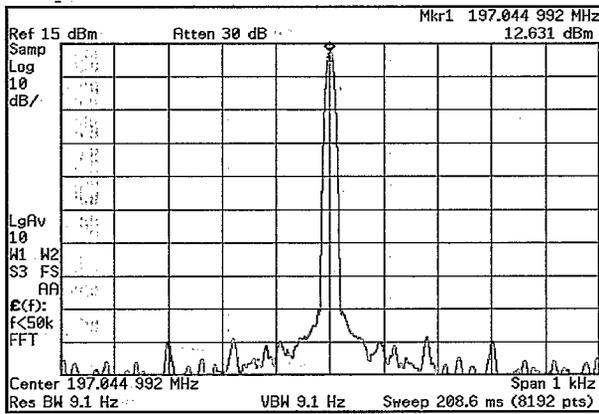


Figure 4. Storage Cavity Spectrum (1 kHz)

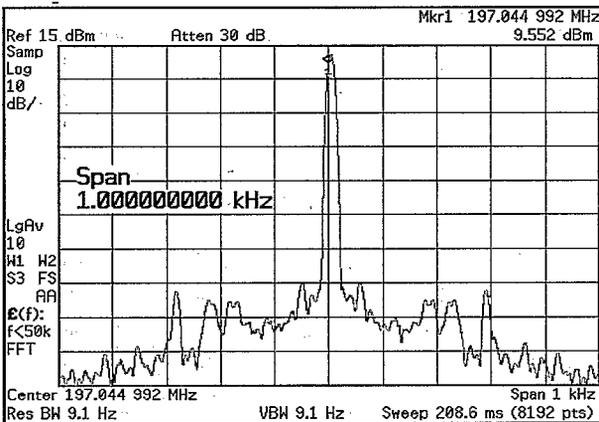


Figure 5. HP8644A Spectrum

the accelerating cavities, they must have the same phase relationship after the frequency jump as they had before the frequency offset was applied. This can be accomplished because the Field Programmable Gate Array (FPGA) that controls the application of the offset frequency is clocked by the same signal as the DDS providing the storage cavity drive. There is a phase accumulator implemented in the FPGA which keeps track of the total accumulated phase shift (modulo 360) and only allows the frequency jump to occur when this phase goes through zero. Since this phase accumulator is using exactly the same clock and frequency offset data as the DDS, there is no limitation on how long the offset is applied before returning to the original frequency. In

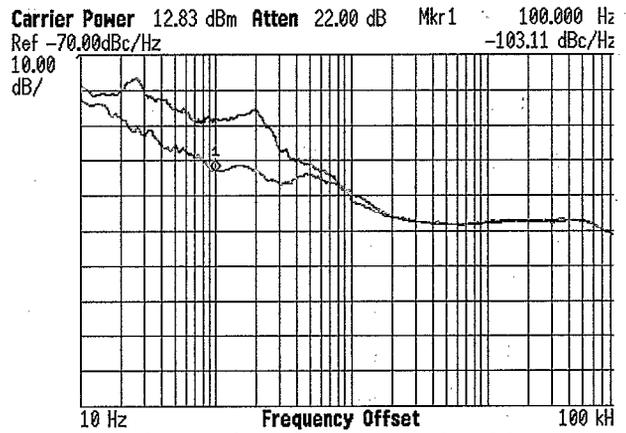


Figure 6. Phase noise of storage cavity drive (blue trace) and HP8644A (green trace)

tests, the offset was left running for three days and jumped back with exactly the right phase.

There was originally some thought of implementing the Numerically Controlled Oscillator (NCO) portion of the DDS in an FPGA with an external digital to analog converter to provide the analog output. This initially looked quite promising (for all the flexibility this would provide) but it eventually proved unusable. While the noise performance was actually quite good, it was dependant on the utilization of other portions of the FPGA. As other, non-related functions were added to the FPGA, the noise performance became dramatically worse.

CONCLUSION

The low noise DDSs have been installed in both RHIC rings which has extended beam lifetime. The 'frequency jump' rebucketing, made possible by the flexibility of this system, has become the standard rebucketing procedure and works with great reliability.

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