

FRONT-END ASIC FOR A SILICION COMPTON TELESCOPE *

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Front-End ASIC for a Silicon Compton Telescope

Gianluigi De Geronimo, Jack Fried, Elliot Frost, Bernard F. Philips, Emerson Vernon, and Eric A. Wulf

Abstract – We describe a front-end application specific integrated circuit (ASIC) developed for a silicon Compton telescope. Composed of 32 channels, it reads out signals in both polarities from each side of a Silicon strip sensor, 2 mm thick 27 cm long, characterized by a strip capacitance of 30 pF. Each front-end channel provides low-noise charge amplification, shaping with a stabilized baseline, discrimination, and peak detection with an analog memory. The channels can process events simultaneously, and the read out is sparsified. The charge amplifier makes use of a dual-cascode configuration and dual-polarity adaptive reset. The low-hysteresis discriminator and the multi-phase peak detector process signals with a dynamic range in excess of four hundred. An equivalent noise charge (ENC) below 200 electrons was measured at 30 pF, with a slope of about 4.5 electrons / pF at a peaking time of 4 μ s. With a total dissipated power of 5 mW the channel covers an energy range up to 3.2 MeV.

I. INTRODUCTION

A large field-of-view silicon Compton telescope was recently proposed for detecting Special Nuclear Materials (SNMs) [1-5]. Among other advantages, this instrument can operate at room temperature and achieve a high signal-to-noise ratio by reducing the background to the events that are reconstructed to the same location as the source of interest [6]. Other applications that can benefit from this development include nuclear astrophysics, high-energy solar observations, and nuclear medical imaging [2].

The Compton telescope, shown in Fig. 1, is composed of 24 layers of 3 \times 3 sensor arrays. Each array contains nine double-sided 2-mm thick silicon sensors each of 9 \times 9 cm², bearing orthogonal strips on the opposite sides. The strips are daisy-chained in both directions, realizing a total of 192 strips per side, each about 27 cm long (pitch \approx 1.4 mm). A bias voltage is applied to deplete the sensors, and the charge generated by the ionizing event induces on the strips a positive or a negative charge, depending on the sensor's side. The orthogonal arrangement allows the reconstruction of the position of the event in each layer.

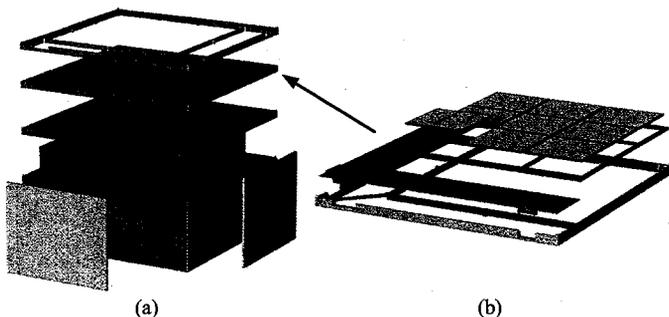


Fig. 1. Picture illustrating the concept of the Compton telescope (a), composed of 24 layers (b) of 3x3 daisy-chained silicon strip sensor arrays.

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To read out the signals from the 9216 strips (4608 for each polarity), a low-noise application specific integrated circuit (ASIC) is required. When connected to the strips that are characterized by a capacitance of about 30 pF, the ASIC must provide a resolution better than 3 keV FWHM (about 360 electrons rms), covering an energy range of 1.6 MeV without dissipating more than a few mW per channel.

The ASIC discussed here was developed for this purpose jointly by the Naval Research Laboratory (NRL) and Brookhaven National Laboratory (BNL). In this paper, we describe the ASIC's architecture, and report our first experimental results.

II. ARCHITECTURE OF THE ASIC

Fig. 2 shows the architecture of the ASIC that comprises 32 front-end channels, 32:1 multiplexers, bias circuitry, a test-pulse generator, two 10-bit DACs for threshold and test pulse control, configuration registers, and logic to control the acquisition, readout, and configuration. Each channel implements a low-noise charge amplifier, a shaper with stabilized baseline, a discriminator with trimming, and a peak detector with analog memory. Details of some of these circuit blocks are given below.

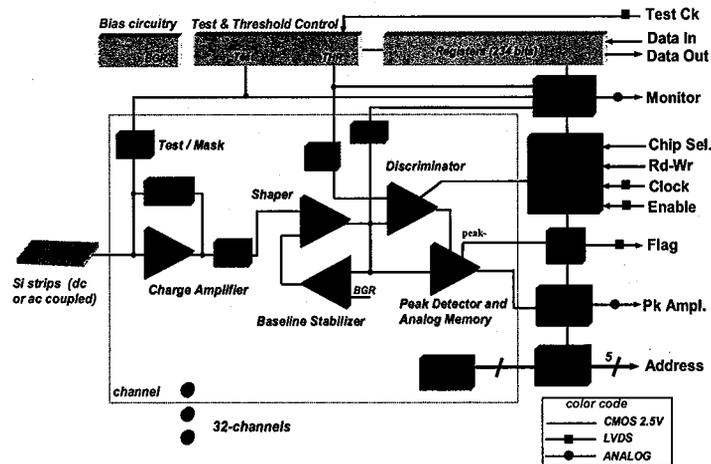


Fig. 2. Architecture of the 32-channel ASIC.

The charge amplifier input MOSFET M_1 is a p-channel of gate length $L = 0.36 \mu\text{m}$, and gate width $W = 3 \text{ mm}$ ($30 \mu\text{m} \times 100 \text{ fingers}$). Biased at a drain current of $400 \mu\text{A}$, the MOSFET is optimized for an external input capacitance of 30 pF [7]. With a transconductance $g_m = 9 \text{ mS}$ and a gate capacitance $C_{g1} = 4.8 \text{ pF}$, it contributes to the equivalent noise charge (ENC) with about 270 electrons at 1 μ s peaking time with the 30 pF input load.

The charge-amplification section (charge amplifier in Fig. 2) has three stages (see Fig. 3), all based on the adaptive continuous reset configurations discussed in [8] and [9]. The feedback capacitor of the first stage is 300 fF. The first and the second stage provide, respectively, a charge gain of 14 and 4. The third stage provides a signal inversion, which is enabled only for a

negative input charge polarity (dotted lines in Fig. 3), and bypassed in the other case (dashed line in Fig. 3). To have each reset stage to properly operate with either the negative or the positive input charge, a combination of both classical and mirror configurations is simultaneously implemented and alternatively enabled (MOSFETs indicated either in red for negative input charge polarity, and in blue with dots for the other case) depending on the input charge's polarity. The output of the last stage (the second or the third depending on the polarity), is connected to the virtual ground input of the shaping amplifier.

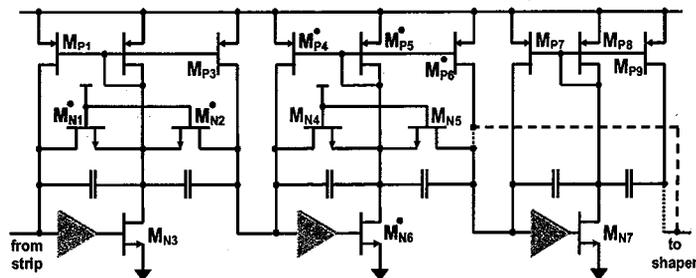


Fig. 3. Multi-stage charge amplification with adaptive continuous reset for operating with both polarities of input charge. The output is connected to the virtual ground input of the shaping amplifier.

To match the 30 pF strip capacitance, the input MOSFET M_1 has a relatively large gate size, which entails a small output resistance, $r_{o1} \cdot 9 \text{ k}\Omega$, and a relatively large gate-to-drain capacitance, $C_{gd1} \cdot 1.1 \text{ pF}$. To achieve a high voltage gain and wide bandwidth, the voltage amplifier typically implements a cascode, where the current is about one tenth of the drain current of M_1 . In our case, due to the small r_{o1} and large C_{gd1} , a single cascode (SCS) configuration, based on one MOSFET M_C as shown in Fig. 4(a), would considerably limit the amplifier's performance. With its relatively high input impedance, the SCS limits the dc gain and adds a pole at the drain of M_1 at relatively low frequency. In addition, it affects the pole-zero cancellation of the charge amplifier because of the contribution from C_{gd} which, multiplied by the gate-to-drain voltage gain of M_1 , integrates a non-negligible amount of the signal charge. The resulting effective increase in the overall feedback capacitance introduces an error in the pole-zero cancellation.

To improve the performance, the input impedance of the cascode must be reduced. We analyzed two solutions, both frequently adopted by designers: the amplified cascode (ACS) shown in Fig. 4(b), and the dual cascode (DCS) shown in Fig. 4(c).

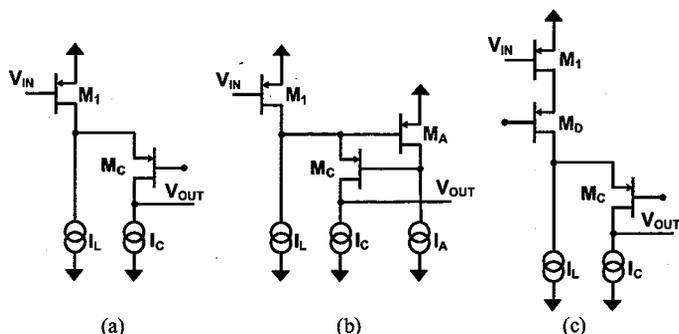


Fig. 4. Alternative cascode configurations: (a) single non-amplified SCS, (b) single amplified ACS, and (c) dual DCS.

The ACS controls the gate voltage of M_C through a feedback loop realized using the voltage amplifier M_A . The DCS has a second cascode M_D , located between M_1 and M_C , operating at the same current as M_1 . We compare the three configurations in Fig. 4 analyzing them in terms of impedance at the drain of M_1 , amplifier dc voltage gain, bandwidth, noise, voltage drop, and dissipated power.

In the following, $(g_{mC}, r_{oC}, C_{gsC}, C_{gdC})$, $(g_{mA}, r_{oA}, C_{gsA}, C_{gdA})$, and $(g_{mD}, r_{oD}, C_{gsD}, C_{gdD})$ are, respectively, the transconductance, output resistance, gate-to-source, and gate-to-drain capacitance of M_C , M_A , and M_D , while r_C is the resistance of the current source, I_C . In all cases and for all MOSFETs we assume a dc gain $g_m r_o \gg 1$.

In terms of the impedance, Z_{dd} , at the drain of M_1 , the comparison can be done at low frequency. It results in the corresponding resistances r_{dd} :

$$\begin{aligned} r_{dd} &\approx r_{o1} \frac{r_C + r_{oC}}{r_C + r_{o1} g_{mC} r_{oC}} && \text{SCS} \\ r_{dd} &\approx r_{o1} \frac{r_C + r_{oC}}{r_C + r_{oC} + r_{o1} g_{mA} r_{oA} g_{mC} r_{oC}} && \text{ACS} \\ r_{dd} &\approx r_{o1} \frac{r_C + r_{oD} g_{mC} r_{oC}}{r_C + r_{oD} g_{mC} r_{oC} + r_{o1} g_{mD} r_{oD} g_{mC} r_{oC}} && \text{DCS} \end{aligned} \quad (1)$$

and, within the typical cases of $r_C \gg r_{oC}$ and $r_C \gg r_{oD} g_{mC} r_{oC}$, both the ACS and DCS exhibit a similar r_{dd} performance.

In terms of the amplifier's dc voltage gain, A_0 , the results are:

$$\begin{aligned} A_0 &\approx \frac{r_C g_{m1} r_{o1} g_{mC} r_{oC}}{r_C + r_{o1} g_{mC} r_{oC}} && \text{SCS} \\ A_0 &\approx \frac{r_C g_{m1} r_{o1} g_{mA} r_{oA} g_{mC} r_{oC}}{r_C + r_{oC} + r_{o1} g_{mA} r_{oA} g_{mC} r_{oC}} && \text{ACS} \\ A_0 &\approx \frac{r_C g_{m1} r_{o1} g_{mD} r_{oD} g_{mC} r_{oC}}{r_C + r_{oD} g_{mC} r_{oC} + r_{o1} g_{mD} r_{oD} g_{mC} r_{oC}} && \text{DCS} \end{aligned} \quad (2)$$

So, again, within the typical cases, both the ACS and DCS exhibit comparable A_0 performance.

In terms of bandwidth, the SCS introduces in the amplifier's voltage transfer function only one pole (time constant τ_1), while the ACS and the DCS introduce two poles (time constants τ_1 and τ_2), but at higher frequency. For the case of the ACS the two poles can be complex conjugate, and consequently, the associated phase margin could make difficult for the designer to stabilize charge amplifier's feedback loop. To guarantee real poles the ACS must be designed to satisfy the following condition:

$$g_{mA} > 4g_{mC} \frac{C_{gd1} + C_{gsA}}{C_{gdA} + C_{gsC}} \quad \text{ACS} \quad (3)$$

and, assuming that (3) is satisfied, the three alternatives perform as follows:

$$\begin{aligned}
\tau_1 &\approx \frac{C_{gd1} + C_{gsC}}{g_{mC}} \approx \frac{C_{gd1}}{g_{mC}} && \text{SCS} \\
\tau_1 &\approx \frac{C_{gdA} + C_{gsC}}{g_{mC}}, \tau_2 \approx \frac{C_{gd1} + C_{gsA}}{g_{mA}} && \text{ACS} \\
\tau_1 &\approx \frac{C_{gdD} + C_{gsC}}{g_{mC}}, \tau_2 \approx \frac{C_{gd1} + C_{gsD}}{g_{mD}} && \text{DCS}
\end{aligned} \tag{4}$$

We note that if M_A operates with a size and current comparable to M_D , the ACS and DCS deliver comparable performances.

In terms of noise, performing for simplicity the calculations at low frequency and assuming an infinite load resistance r_c , it follows

$$\begin{aligned}
\overline{V_{ni}^2} &\approx \frac{\overline{V_{nC}^2}}{g_{m1}^2 r_{oi}^2} && \text{SCS} \\
\overline{V_{ni}^2} &\approx \frac{\overline{V_{nA}^2}}{g_{m1}^2 r_{oi}^2} + \frac{\overline{V_{nC}^2}}{g_{mA}^2 r_{oA}^2 g_{m1}^2 r_{oi}^2} && \text{ACS} \\
\overline{V_{ni}^2} &\approx \frac{\overline{V_{nD}^2}}{g_{m1}^2 r_{oi}^2} + \frac{\overline{V_{nC}^2}}{g_{mD}^2 r_{oD}^2 g_{m1}^2 r_{oi}^2} && \text{DCS}
\end{aligned} \tag{5}$$

where $\overline{v_{nC}^2}$, $\overline{v_{nA}^2}$, and $\overline{v_{nD}^2}$ are, respectively, the equivalent input noise voltages of M_C , M_A , and M_D , and $\overline{v_{ni}^2}$ is the corresponding equivalent contribution at the input of the amplifier. If M_A operates with a size and current comparable to M_D , the ACS and DCS offer similar performances.

In terms of additional voltage drop compared to the single cascode, for the ACS it depends on the gate-to-source voltage of M_A , while for the DCS it is controlled by the gate bias voltage of M_D . Considering that the source-to-drain voltage of M_1 and M_C can be contained in most cases within very few hundreds of mV, the two solutions exhibit an equivalent drop.

In terms of power dissipation, the ACS requires the additional current associated with M_A that, to contain the noise and satisfy (3), can be non-negligible.

Taking all these findings into consideration, we adopted the DCS configuration. The gate width of M_D that maximizes the bandwidth can be calculated from (4), and it is about one third to one fourth of the gate width of M_1 , depending on the gate width of M_C .

The charge amplifier in Fig. 3 is followed by a 5th order shaper [10] that provides charge to voltage conversion and filtering with a peaking time adjustable to 0.5-, 1-, 2-, and 4- μ s. The output baseline is stabilized with a band-gap-referenced BLH circuit [11]. The overall channel gain can be set to nominal values of about 14-, 28- or 56-mV/fC, thus covering an energy range up to 3.2 MeV. A low-hysteresis comparator with multiple-firing suppressor [12] accommodates event discrimination with a threshold controlled through a 10-bit DAC common to all channels, and a 4-bit DAC per channel for equalization. Above-threshold events are processed by a multi-phase peak detector with analog memory [12, 13].

The acquisition is enabled by setting the external LVDS (Low Voltage Differential Signal) Enable at high; it can be automatically disabled either when a first channel crosses the threshold, or when a first channel finds the peak. An LVDS

Flag, which can be released either at the first peak found or 200 ns later, indicates one or more successful acquisitions. Users can set the delay, during which other channels may be processing events, after which the read out of the measured amplitudes can start. The ChipSelect high sets the ASIC in the readout mode, and at each LVDS Clock, the peak amplitude and the address of those channels that processed the above-threshold events are made sequentially available at dedicated outputs (one analog output for the peak amplitudes, five digital outputs for the address), thus providing sparsification.

Each channel implements a 200 fF test capacitor connected to the input, with another terminal connected to an on-chip pulse generator. The pulse generator is triggered with the LVDS clock TestCk, and has an amplitude adjustable with a dedicated 10-bit DAC. Additional ASIC functions include per channel masking, channel shaper output monitor, and a DACs monitor.

Fabricated in CMOS 0.25 μ m, the ASIC has 80 pads and measures about 5 mm \times 5 mm. The channel itself is 4.2 mm \times 120 μ m and dissipates about 4 mW. The entire ASIC system dispels about 160 mW, yielding an effective power per channel of about 5 mW. Fig. 5 is a picture of the die.

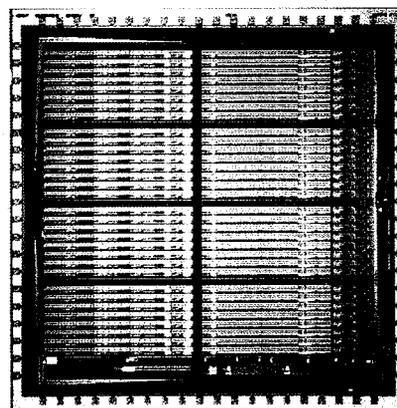


Fig. 5. Picture of the 5 mm \times 5 mm die.

III. FIRST EXPERIMENTAL RESULTS

The ASIC initially was characterized without sensor and then, in preliminary experiments, with a sensor; we report here the most relevant results.

Fig. 6 illustrates the response of the channel to a negative charge of about 25 fC for the four peaking times and three gain settings. The baseline is about 260 mV. We measured an integral linearity error below $\pm 0.25\%$ ($\pm 0.4\%$ at 0.5 μ s peaking time) for amplitudes of output signal up to 2.25 V (including the $\bullet 260$ mV baseline), corresponding to an input charge up to 140 fC at the lowest gain setting. A channel-to-channel dispersion of about 5 mV rms and 1.6 % rms (3.7 % rms at 0.5 μ s peaking time) respectively characterized the baseline and gain.

The ENC versus external input capacitance is shown in Fig. 7 for the four peaking time settings, measured at each of the three gain settings. Fig. 7(a) shows the case of negative charge amplification, while Fig. 7(b) shows the positive. A noise slope from about 4.5 e/pF at 4 μ s to about 12 e/pF at 0.5 μ s was extracted for both.

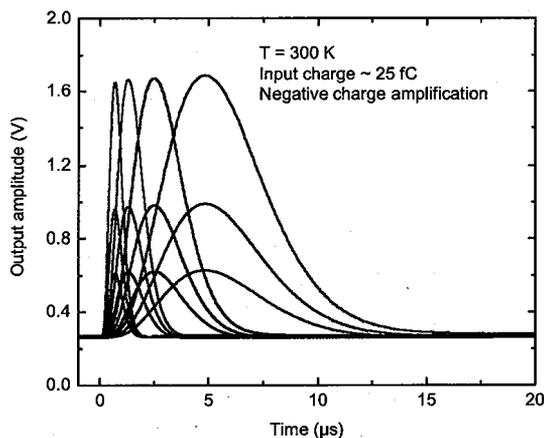


Fig. 6. Measured pulse response to a negative charge of 48 fC.

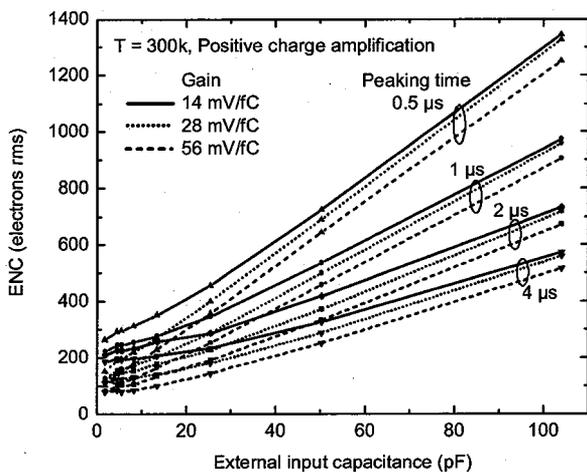
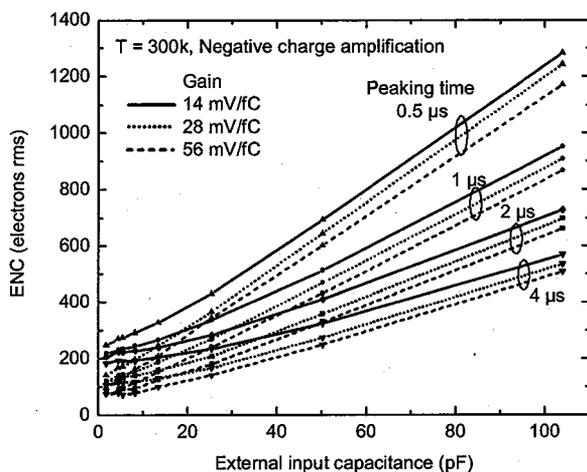


Fig. 7. ENC versus external input capacitance for the four peaking time settings, measured at the three gain settings: (a) negative charge amplification; (b) positive charge amplification.

In Fig. 8 we depict the gain versus external input capacitance for the same settings. We measured a drop in gain from 3%/100pF at 4 μ s to 6%/100pF at 0.5 μ s. The stronger dependence of the gain on the peaking time was apparent in the positive charge amplification. We are investigating this effect; it might be partially attributed to the edge of internal pulse generator, which is non symmetrical with respect to the polarity. A

gain 9% larger than the nominal was measured at the maximum gain setting and at 4 μ s peaking time, but reduced for shorter peaking times.

In Fig. 9, we plot the measured peak amplitude, processed by the discriminator and peak detector circuits, as a function of the injected charge. The error in the peak detected amplitude, compared with the actual shaped pulse amplitude, also is shown. The circuits can discriminate and process for peak detection amplitudes from about 8 mV above baseline (about 0.22 fC at this gain setting), demonstrating a dynamic range of about 400. In this measurement the dynamic range still is limited by the hysteresis (about 10 mV) of the comparator in the discrimination circuit, as it can be evaluated considering the signal-to-noise ratio of about $1400e^-/100e^- = 14$.

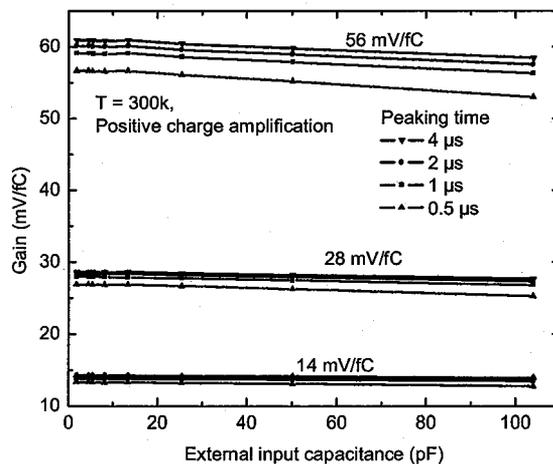
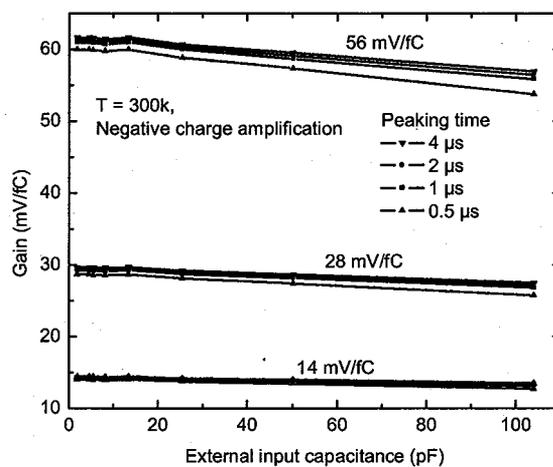


Fig. 8. Gain versus external input capacitance for the four peaking time settings, measured at the three gain settings: (a) negative charge amplification; (b) positive charge amplification.

Fig. 10 shows a preliminary spectrum of ^{241}Am and ^{57}Co acquired at NRL using the ASIC connected to a silicon strip sensor of 1.7 cm \times 1.4 mm \times 500 μ m. At a temperature of -40C, we obtained a resolution of about 1.4 keV at 59.5 keV with a peaking time of 4 μ s and at a temperature of -40°C. The ^{57}Co peak at 122 keV, with a resolution of 1.5 keV, is also visible. The available linear range at this gain setting of 56 mV/fC (2.5 mV/keV) is about 800 keV.

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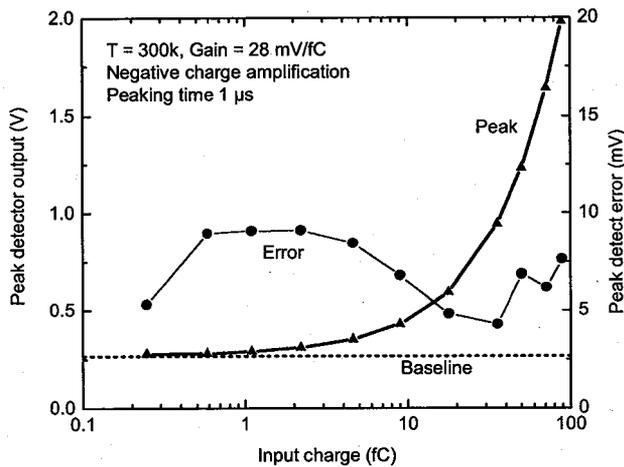


Fig. 9. Measured peak amplitude, processed by the discriminator and peak detector circuits, versus the input charge.

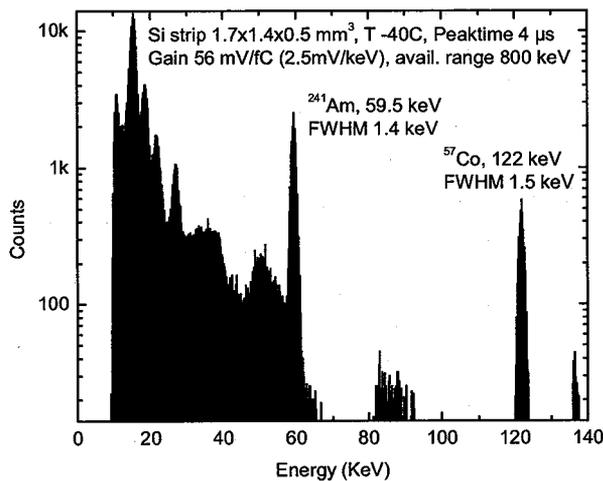


Fig. 10. Spectrum from ^{241}Am and ^{57}Co sources.

IV. CONCLUSIONS AND FUTURE WORK

The performance of the ASIC described here, developed for a Silicon Compton telescope based on 30 cm long silicon strips, is in good agreement with the design. It has relatively small margins for improvement and indeed might be ready for the application. We plan to undertake extensive characterization with the sensors and report our findings soon.

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