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***Low-Level Radio Frequency System Development for  
the National Synchrotron Light Source II***

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# LOW-LEVEL RADIO FREQUENCY SYSTEM DEVELOPMENT FOR THE NATIONAL SYNCHROTRON LIGHT SOURCE II \*

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## Abstract

The National Synchrotron Light Source-II (NSLS-II) is a new ultra-bright 3GeV 3rd generation synchrotron radiation light source. The performance goals require operation with a beam current of 500mA and a bunch current of at least 0.5mA. The position and timing specifications of the ultra-bright photon beam imposes a set of stringent requirements on the performance of radio frequency (RF) control. In addition, commissioning and staged installation of damping wigglers and insertion devices requires the flexibility of handling varying beam conditions. To meet these requirements, a digital implementation of the LLRF is chosen, and digital serial links are planned for the system integration. The first prototype of the controller front-end hardware has been built, and is currently being tested.

## INTRODUCTION

The NSLS II RF system will include four 500 MHz, 2.5 MV/300 kW superconducting cavities in the Storage Ring (SR), two passive 3<sup>rd</sup> harmonic superconducting cavities, also in SR, one 1.2 MV/80 kW normal conducting PETRA cavity in the Booster, and up to four 3 GHz travelling-wave accelerating structures in the LINAC. The performance requirement on the SR RF is derived from the beam stability requirement of user experiments [1], [2], [3]. Some of the directly related items are listed in Table 1. The beam stability requirement translates into a set of general requirements on the RF, among which, the most basic one is the RF phase stability of 0.14 deg, RMS (over 0.5~50 kHz bandwidth). To support certain measurements and compensate the change in the ring circumference, the LLRF is also required to have a RF frequency tuning range of  $\pm 30$  kHz or greater with a resolution of 1 Hz or smaller. The planned LLRF sub-system for each cavity/RF power source has a cavity field controller front-end as its key device for the core

Table 1: RF Phase, Energy Stability Requirements

Parameter \ Tolerance	$\Delta\phi$ (deg)	$d\delta$ ( $\times 10^{-4}$ )
Centroid jitter due to residual dispersion	0.81	3
Vertical divergence (from momentum jitter)	2.4	9
Dipole, TPW(position stability due to momentum jitter)	0.27	1
Timing experiments(5% of 15os bunch@>500Hz)	0.14	0.5

functionalities. It also has some auxiliary, but necessary function devices such as the DSP module for the floating-point computations at higher level, as well as a high-power RF protection module. As an integration method, all the front-end function modules in a LLRF sub-system are connected to a master cell-controller in a star configuration through the dedicated 100Mbps serial links. The cell controller facilitates the inter-module communications and the communication with the upper-level EPICS IOC. This system integration scheme is illustrated in Figure 1. With this scheme, the serial link connections replace the backplanes in legacy parallel bus systems, and therefore eliminating the restriction of the mechanical form factor of the modules, and allowing the use of the packages that are the best suitable for this RF application. The cell controller is being jointly developed by NSLS-II Controls Group and LBNL [4]. The same/or similar LLRF hardware will be used for all SR, Booster and LINAC applications.

## CAVITY FIELD CONTROLLER

The digital hardware in the cavity controller front-end module is implemented on a high-density FPGA device. The primary reason for choosing FPGA over ASIC DSP for this functionality is that the FPGA implementation allows a concurrent processing of many signals, and thus results in shorter data latency. The standard functions of a cavity field controller implemented in FPGA include the input signal filtering, vector signal detection (such as "I/Q"), loop phase correction, P-I feedback control, the digital synthesis of output drive signal, and etc. The standard functions also include the cavity tuning control, and the logic of the necessary protective interlocks. These functions will be implemented as the IP ("intellectual property") cores in FPGA. Figure 2 shows our first development platform for the controller front-end. As recent digital hardware for LLRF application [5],

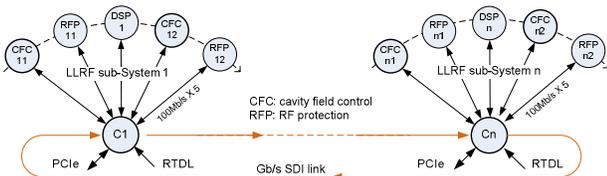
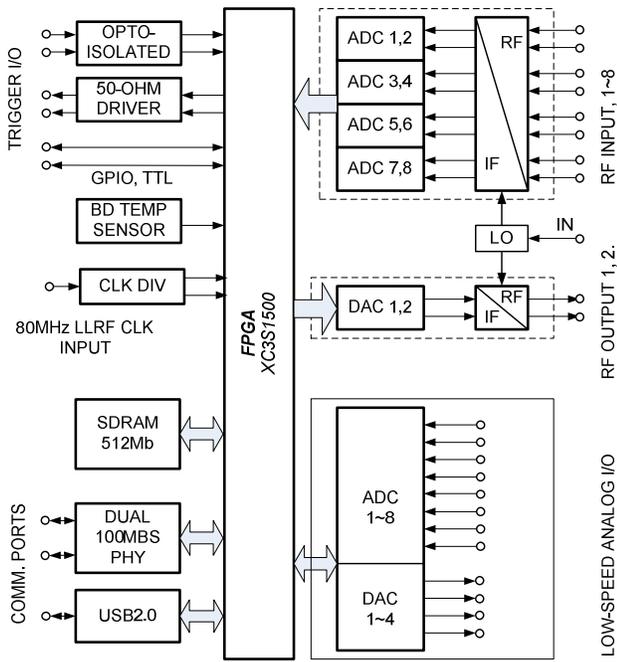


Figure 1 In NSLS-II LLRF, high-speed serial links are planned in place of legacy parallel bus for the system integration and the interface with the accelerator controls infrastructure.

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**Figure 2 The first hardware platform for NSLS-II LLRF development. It has sufficient RF/analog I/Os and communication ports built around the FPGA.**

this platform is also in the form of a general FPGA-based DSP board with RF I/O channels and network connectivity. The LLRF IPs in the FPGA make it LLRF control specific.

### Hardware features

The prototype RF controller board incorporates the following features:

- RF input - 8 channels, 14-bit resolution, simultaneous sampling up to 80 Msps.
- RF output – 2 channels, 14-bit resolution, update rate up to 250 Msps. One channel can be used to output the LLRF controller drive, while the other for generating a test/calibration signal.
- 1.5M gate FPGA (Xilinx Spartan 3 family) with an external memory of 512Mb.
- Trigger I/O, 6 channels
- Low-speed analog I/O, 12-bit, 8 inputs, 4 outputs.
- Dual 100Mbps Ethernet transceiver ports, used as the Physical for implementing the point-to-point serial link between the front-end and the cell controller.
- USB2.0 port. Through this port, the field controller front-end can be directly hosted by a CPU (such as a laptop) without having a cell controller and the upper level IOC.

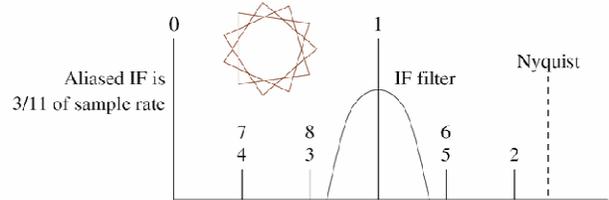
### Choice of IF and LO frequencies

The nominal RF frequency of NSLS-II is 500MHz, and the chosen intermediate frequency (IF) of LLRF is 50MHz. A high-side local oscillator (LO) frequency (550MHz) is also chosen for facilitating the frequency up/down conversions. The choice of 550MHz LO frequency makes it convenient in generating the required

LLRF standard frequencies/clocks for both the “IQ” and “near-IQ” sampling scheme.

### Vector measurement of input IF signals

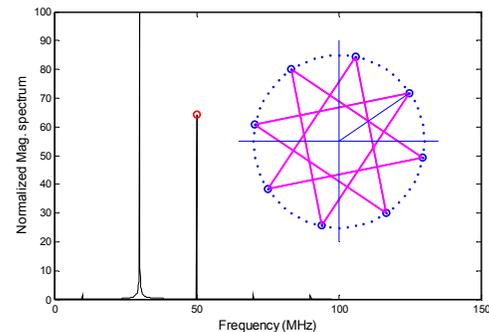
In a digital LLRF controller, the input vector signals (i.e. the cavity field, forward wave etc.) are digitized at a certain rate in order to real-time demodulate the signals for the phase and amplitude data. With the given 500MHz RF and the choice of 550MHz LO, the NSLS-II design can conveniently support both the conventional IQ sampling-based control algorithm as used in SNS LLRF design [5] and the newer near-IQ sampling algorithm developed at LBNL [6]. In the case of IQ sampling, the sampling clock rate is  $4/5 * IF = 40\text{MHz}$ . For near-IQ sampling, the sampling clock rate is  $11/8 * IF = 68.75\text{MHz}$ . While the standard IQ sampling offer simplicity in data sorting, the non-IQ sampling scheme provides a benefit of improved measurement precision as illustrated in Figure 3.



**Figure 3 With a near-IQ sampling rate of  $11/8 * IF$ , the spectral aliasing of the harmonics is avoided, and thus the measurement precision is improved.**

### Synthesis of output IF vector signal

The designed cavity field controller for NSLS-II uses a direct digital synthesis (DDS) technique to produce the 50MHz IF output, and therefore eliminates the use of an analog vector modulator in the output. The principle of this particular DDS is the same as that of a textbook example, and is illustrated in Figure 4 below. Basically, clocking an IQ data stream through the IF output DAC is like having a digital phase wheel with a phase increment size of  $2^N$ ,  $N=3$ . Given the DAC clock  $F_{clk}=80\text{MHz}$ , and

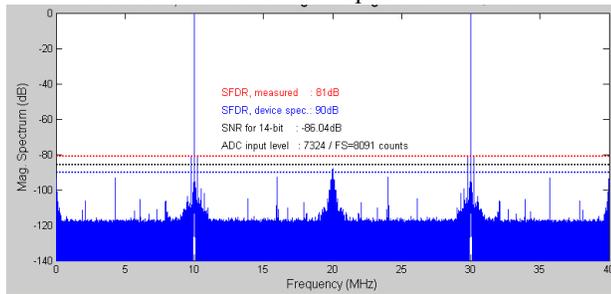


**Figure 4 Spectrum and digital phase wheel of the direct digitally synthesized 50 MHz IF output with a 80MHz DAC clock (for the case of IQ sampling).**

select jump size  $M=5$ , the synthesized frequency is thus  $F_0 = M \times F_{\text{clk}} / 2^N = 50\text{MHz}$ . The unwanted 30MHz harmonic in the spectrum needs to be removed with a filter.

## DEVELOPMENT STATUS

The first prototype of the cavity field controller front-end has been designed and fabricated as shown in Figure 2 and 6. It has passed the basic functionality tests, and the some good results have been produced in the SNR measurements of the RF signal I/O channels as shown in Figure 5. The USB2.0 port communication performs well, which allows the controller to run with a local PC host only, which is necessary for supporting some of the near-term RF development activities. The back-end cell controller is currently under development in NSLS-II Controls Group, and recently a prototype was demonstrated for its real-time Gigabit fibre-optic links. The near-term goals include the IP development for the LLRF functionalities and 100MSPS serial links.



**Figure 5 SNR measurements of the LLRF controller prototype input ADC channels. The 50MHz IF is digitized at 40MHz sampling rate, and the carrier line is folded to 10/30MHz position. A SFDR (Spurious-Free Dynamic Range) of -81dB is measured.**

## SUMMARY

As a mixed-signal system, the development of the NSLS-II LLRF controller hardware has been emphasized on achieving the lowest signal-to-noise ratio (SNR). The preliminary tests on the first prototype of the field controller produced some promising results, and the prototype provides a good starting point for further development. The cell controller plays a key role in the LLRF system integration, and providing a method for merging the LLRF into the accelerator global controls infrastructure.

## ACKNOWLEDGEMENT

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**Figure 6 The first prototype of the cavity field controller hardware currently under tests for its I/O functions and SNR characterization.**

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