FRONT-END ASIC FOR PIXELLATED WIDE BANDGAP DETECTORS

Emerson Vernon, Gianluigi De Geronimo, Jack Fried
Brookhaven National Laboratory
Upton, NY 11973-5000

Cedric Herman, Feng Zhang, and Zhong He
Dept. Nuclear Engineering & Radiological Sciences
University of Michigan, Ann Arbor, MI

August, 2009

This manuscript has been authored by Brookhaven Science Associates, LLC under Contract No. DC-AC02-98CH10886 with the U.S. Department of Energy. The United States Government retains, and the publisher, by accepting the article for publication, acknowledges, a world-wide license to publish or reproduce the published form of this manuscript, or allow others to do so, for the United States Government purposes.
DISCLAIMER

This work was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or any third party's use or the results of such use of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof or its contractors or subcontractors. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.
Front-end ASIC for pixellated wide bandgap detectors

Emerson Vernon¹, Gianluigi De Geronimo¹, Jack Fried¹,
Cedric Herman², Feng Zhang², and Zhong He²

ABSTRACT

A CMOS application specific integrated circuit (ASIC) was developed for 3D Position Sensitive Detectors (PSD). The preamplifiers were optimized for pixellated Cadmium-Zinc-Telluride (CZT) Mercuric-Iodide (HgI₂) and Thallium Bromide (TlBr) sensors. The ASIC responds to an ionizing event in the sensor by measuring both amplitude and timing in the pertinent anode and cathode channels. Each channel is sensitive to events and transients of positive or negative polarity and performs low-noise charge amplification, high-order shaping, peak and timing detection along with analog storage and multiplexing. Three methodologies are implemented to perform timing measurement in the cathode channel. Multiple sparse modes are available for the readout of channel data. The ASIC integrates 130 channels in an area of 12 x 9 mm² and dissipates ~330 mW. With a CZT detector connected and biased, an electronic resolution of ~200 e⁻ rms for charges up to 100 fC was measured. Spectral data from the University of Michigan revealed a cumulative single-pixel resolution of ~0.55 % FWHM at 662 KeV.

Key Words: Readout ASIC; 3D PSD; Bi-parametric; CZT; HgI₂; TlBr; room temperature spectroscopy

I. INTRODUCTION

Pixellated Cadmium Zinc Telluride (CZT) sensors have been the choice detectors in room temperature, large volume gamma-ray spectrometry. Increased interest in other wide-bandgap semiconductor materials has broadened the prospect for Mercuric Iodide (HgI₂) and Thallium Bromide (TlBr). Inherent properties such as high density and mass, photon stopping potential and wider bandgap which minimize the thermal generation of charge carriers (lower noise) has given much attention to TlBr as a promising material for room temperature spectroscopy. Even though state-of-the-art technologies are used to produce these materials with improved homogeneity and relatively low dark current, the spectral resolution is strongly limited by non-uniformities, poor hole mobility, and electron trapping. Consequently, low noise readout electronics in conjunction with event reconstruction methods are required to perform signal correction for improved resolution.

The 3D position-sensitive detection technique (3D PSD) proposed by Zhong He in the late '90, combines the small pixel effect with the acquisition of amplitude and timing of signals at each anode pixel and at the cathode. The bi-parametric information is used to correct the measurement for each volumetric pixel (voxel) and to reconstruct the position of the ionizing interaction. With this technique it is possible to compensate for deficiencies like poor hole mobility, electron trapping, and non-uniformities that typically affect wide bandgap materials. The 3D PSD was successfully applied to Cadmium-Zinc-Telluride (CZT) and, more recently, to Mercuric Iodide (HgI₂), and Thallium Bromide (TlBr) sensors.

This work was founded by the Defense Threat Reduction Agency of the US DoD
1. G. De Geronimo (degeronimo@bnl.gov), E. Vernon, and J. Fried are with the Instrumentation Division, Brookhaven National Laboratory, Upton, NY.
2. Z. He, C. Herman, and F. Zhang are with the Department of Nuclear Engineering and Radiological Sciences, University of Michigan, Ann Arbor, MI.
II. FIRST PROTOTYPE

The first version of the application specific integrated circuit (ASIC) for 3D PSD with CZT was presented. Based on an architecture which supported local threshold discrimination in each anode or cathode channel, we reported a preliminary resolution of 0.72% FWHM at 662 keV from a $^{133}$Cs source in a single pixel with a $20\times20\times5$ mm$^3$ sensor. Recent results from the first version of the ASIC are presented in section III.

III. RESULTS FROM THE FIRST VERSION

The first version of the ASIC was extensively characterized at the University of Michigan using a wide range of CZT sensors. Fig. 1 shows the $^{137}$Cs spectrum measured at room temperature using a $2\times2\times1.5$ cm$^3$ sensor with 11x11 anode pixels. An average single-pixel event resolution throughout the whole sensor of about 0.51% FWHM (3.37 keV) at 662 keV was measured. The contribution from the electronics was about 2 keV. Peak-to-Compton and peak-to-valley ratios of 18.7 and 273 were measured respectively. The FWHM for two-pixel, three-pixel and four-pixel events were measured at 0.89%, 1.26% and 1.75%. Along with these encouraging results, the characterization evidenced three issues.

![BNL-HD ASIC dynamic range = 3 MeV, noise = 2 keV FWHM](image)

Fig. 1 - Single-pixel event spectrum from all 121 pixels measured on a 2$\times$2$\times$1.5 cm$^3$ CZT sensor. The resolution for each individual pixel is also shown.

Although the resolution from the single pixel events compared favorably with the electronic noise of the system, these events only constitute a fraction of the photo peak events from the detector. As a result, the bi-parametric data was used to identify charge sharing events during reconstruction to reduce loss in the photo peak efficiency. While reconstructing multi-pixel events a second line was observed in the $^{137}$Cs spectrum with amplitude higher than the main 662 keV line, as shown in Fig. 2 (a). The reason was found in the inability of the system to distinguish between signals where the charge was induced with collection (true shared events), characterized by a unipolar shaped response, and transient signals induced in neighboring pixels where the charge was induced without collection, characterized by a bipolar response. The timing associated with the detection of the peak, along with a higher software threshold, reduced but could not completely solve the problem. As a result, the architecture was modified to process and readout the amplitude and timing information associated with non-collecting events.
When the system was operated at high rates, a second line was observed in the $^{137}$Cs spectrum with amplitude lower than the main 662 keV line, as shown in Fig. 2 (b). The source of this issue was found to be a board level capacitive coupling between the inputs of a few channels and the analog output lines. During the readout phase when the analog data for collecting channels are multiplexed, an increase in signal level on the analog data line injected a large positive charge on the capacitive coupled analog front-end. The front-end took some time to recover from this abnormal situation and if an event occurred during this recovery period, it was recorded with reduced amplitude. The interposer board was modified to ensure there was adequate shielding and separation between the analog inputs and the analog data lines.

![Energy Spectrum for the Whole Field](a) ![Energy Spectrum for Channel 15, Pixel E, R](b)

Fig. 2 – Issues observed with spectral measurements using the first version of the ASIC: (a) line at amplitude higher than 662 keV in multi-pixel events; (b) line at amplitude lower than 662 keV in a few pixels when operating at high rate.

It was also observed that digital pick-up and poor peak detection stability internal to the ASIC, affected the timing resolution. The peak detect signal served as a trigger to start the timing measurement and in some cases a negative peak detect is used to provide an additional sample of the analog timing data. Consequently, as the peak detector tracks the signal to its peak, instabilities may result in the starting and sampling of the timing measurements on peaks which are not related to the true event. This effect is more pronounced for events of small amplitudes which ultimately increases the time walk and reduces the time resolution of the system. This observation along with other improvements were addressed in the revised ASIC.

**IV. ARCHITECTURE OF THE SECOND VERSION**

The capability of the ASIC to accommodate sensors of different sizes and material composition was improved. Fig.3 shows the block diagram of the ASIC which independently measures the peak amplitude and relative timing on each of 128 anodes while simultaneously capturing the same event data with a cathode channel. With the added channels and retained layout symmetry, it now requires only 2 ASICS to readout a 256-pixel sensor. The shaped analog signal from each channel can be multiplexed to the auxiliary output for monitoring. The unipolar and bipolar timing signals for the cathode and anode-grid channel can also be multiplexed to the auxiliary monitor, while two dedicated outputs are available for monitoring their respective charge amplifier outputs.

The selection of peaking times was expanded from 0.25, 0.5, 1.0 and 2.0 μs to include 1.5, 3.0, 6.0 and 12.0 μs; where the higher values are for pixelated HgI$_2$ and TlBr sensors. In addition, two gain settings of 20 and 120 mV/μC were implemented to cover the ranges of 3.2 MeV and 530 keV in CZT respectively. Likewise, the cathode timing measurements were implemented with the addition of two gain selections (27 and 162 mV/μC) for unipolar shaping and four gain selections (21, 80, 130, and 518 mV/μC) for bipolar shaping. The internal bias circuitry was upgraded to support the new electronics while the multiplexer and configuration readout control logic was modified for different write and readout schemes to speed up the system.
The system was further enhanced by modifying the anode channel’s ability to process events of either polarity. In the first prototype, the anode channels were designed to process collecting events which were characterized by positive unipolar shaped pulses. However, it was observed that transients or events characterized by a bipolar shape impacted the analog front-end and consequently the event count. Therefore, to distinguish between collecting (unipolar) and non-collecting (bipolar) events, each channel now implements a second discrimination and peak/timing detection circuit for processing negative pulses as shown in Fig. 4. In the occurrence of a non-collecting event, the channel discriminates and processes both positive and negative amplitudes and timings. The additional information can also be used to increase the position resolution of the system.

Configuration and readout of the ASIC is accomplished through a fully differential (Low Voltage Differential Signaling, LVDS) digital interface. The ASIC is configured through a total of 1708 bits whereby, the bits for the channel registers can be written independent of the global register. The manipulation of each channel’s local settings such as mask, test and threshold discrimination (5-bit trim DAC with 2mV step) is controlled by the channel registers; while the setting of gain, peaking time, test signal (step or ramp) and thresholds (seven 10-bit DACs) among other functionalities are controlled by the global registers. Fig. 5 shows a micrograph of the ASIC which was realized in an area of 12.9 × 9.3 mm². The chip dissipates 330 mW, which corresponds to about 2.5 mW per channel.
A total of nine ASIC-interposer-detector assemblies\textsuperscript{13} can be plugged directly into the mother board which supplies power and performs analog to digital conversion. When an event crosses a positive threshold in an anode channel, a flag is released, notifying the down stream electronics of a successful acquisition. The ASIC can now be read out in normal, sparse or enhanced sparse mode. In normal mode, all the channels are read sequentially. At the end of the readout cycle, an additional 128 clock cycles will read the data for negative anode pulses. In sparse mode (Fig. 6(a)), a mixed clock is used to pass a token through the channels in a single cycle and a Flag is provided to indicate if the channel exceeded the threshold. The external ADC data acquisition performs analog-to-digital conversion of only those channels with their flags asserted.

In enhanced sparse mode (Fig. 6(b)) the token is passed through the channels in two cycles. That is, in the first cycle only the Flag is provided, and the external data acquisition collects information on which channels exceeded the threshold, while in the second cycle the peak and timing voltages are made available, and the data acquisition converts only those that exceeded the threshold and their neighbors. Since the first cycle does not require ADC, it can be executed in a few microseconds. Depending on the number of above-threshold events and on the speed of the ADC, the ASIC can be read out in very few tens of microseconds. At the end of reading out the collecting events in both sparse and enhanced sparse mode, an additional 128 cycles allow the readout of the negative pulses, which can consist of either the Flag only or the complete peak and timing information associated with the non-collecting events. With the sparse or enhanced sparse mode described above, the system is expected to realize rates in excess of 10kcps.
V. Results from the Revised Version

Fig. 7 shows the measured root mean square (RMS) electron noise charge (ENC) for an anode and cathode channel without sensor. The measurements were taken at the end of the analog signal chain as a function of shaping time and gain. For the anode channel, the noise charge decreased from 138 e\(^{-}\) to 100 e\(^{-}\) at low gain. At high gain the noise from the shaper decreased while at long peaking times the parallel noise dominated.

![Graph showing measured ENC versus shaping time.](image)

Fig. 7 – Measured ENC versus shaping time.

The timing performance of the anode was evaluated from the channel’s response to a step input produced by the internal test pulse generator. Fig. 8(a) shows the time walk which compares favorably to what was previously reported plus the 1fC limit of the dynamic range was realized at low gain. The introduced high gain setting was used to process low charge events as represented by the open symbols. With the improved performance in timewalk and resolution, at high gain the anode channel resolved charges as low as 0.15fC to less than 12 ns at 0.25\(\mu\)s shaping time as shown in Fig 8(b).

Likewise, at 2 fC of injected charge and 0.25\(\mu\)s shaping time, a resolution of 3.5ns was measured. This was approximately half the value that was previously reported. The timing characteristics now realized can be mainly attributed to the stabilization of the peak and time detect circuits in the anode channels. It is also shown that the measured time resolution increased at long shaping times. An increase in the shaping time for a fixed amount of injected charge resulted in a shaped unipolar pulse with reduced slope and increased radius of curvature at the peak even though the amplitude is preserved. To a first order, both the timewalk and time resolution are proportional to the curvature at the peak since the peak detector takes the differential of the unipolar pulse to derive the zero crossing point which serves as the TAC trigger. As a result, the measured timewalk and time resolution were much larger at longer shaping times.
Fig. 8 – Measured anode (a) timewalk and (b) time resolution vs. input charge at low gain (20mV/IC) and high gain (120mV/IC)

Fig. 9 shows the unipolar timing measured in the cathode channel at four peaking times with a fast shaper and a TAC which was sampled at a known time interval. The solid symbols in Fig. 9(a) indicate a timewalk less than 300 ns at low gain while the open symbols correspond to a timewalk less than 370 ns at high gain and low charge injection. At high charge injection, the slope of the shaped pulse is relatively high which is ideal for good threshold crossing that eventually leads to the convergence of the timewalk at all shaping times. However, a combination of low charge injection and long shaping time reduced the slope of the shaped pulse and due to the dependence of the timewalk on the slope; a greater timewalk was measured for low charges. The solid symbols in Fig. 9(b) shows the corresponding time resolution at low gain which was below 20 ns at 0.6 fC of injected charge. At high gain and 0.15 fC of charge, the resolution was contained below 50 ns. Overall the unipolar timing provides good timing resolution but the timewalk is strongly dependent on amplitude.

Fig. 9 – Measured cathode unipolar (a) time walk and (b) time resolution vs. input charge at 27mV/IC and 162 mV/IC
A plot for a single threshold crossing (timewalk can be corrected using the multi-threshold crossings) and the bipolar timewalk (at 80mV/\(\mu\)C and 0.2 \(\mu\)s shaping time) is shown in Fig. 10(a). When compared to the unipolar and multi-threshold methods, the bipolar provided good timewalk characteristics contained below 20 ns. Even though the multi-threshold method provided a comparatively worse timewalk due to slope dependent threshold crossings, Fig 10(b) confirmed that this methodology provided good time resolution. The entire dynamic range could not be realized for the multi-threshold and bipolar measurements due to a design issue in the bias circuitry which will be addressed in the next revision.

![Graph of injected charge vs. timewalk](image1)

![Graph of injected charge vs. time resolution](image2)

Fig. 10 - Measured cathode Single-threshold and Bipolar (a) time walk and (b) time resolution vs. input charge.

A comprehensive knowledge of each timing method necessitates the need to point out that the ASIC can perform timing measurement in the cathode channel via a unipolar method only, or a simultaneous combination of unipolar and multi-threshold or unipolar and bipolar timing. By processing the timing and amplitude data from the anode in collaboration with the timing and amplitude data from the cathode, the event can be reconstructed to the volumetric pixel (voxel) level whereby the overall resolution of the system is improved.

V. CONCLUSIONS

Encouraging results are still being obtained with the first ASIC prototype designed for 3D PSD. The results presented for the revised ASIC were characteristic of the expected performance to meet the improved design objectives. The time measurements from the anode and cathode channels were significantly improved with the realized stability of the peak detectors. Still, there are a few improvements to be made with the most noticeable being the DAC bias circuitry which impacted the cathode timing measurements with the internal test pulse. With the addition of long peaking times and gain selections, the ASIC readout capability was expanded to include TlBr and HgI\(_2\) detectors.

ACKNOWLEDGMENT

The developments here reported were funded by the Defense Threat Reduction Agency (DTRA) of the US Department of Defense. The authors are grateful to Lt Col Mark C. Wrobel and Dr. Marc A. Black for their encouragement and support.

REFERENCES