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A HIGH PERFORMANCE DAC/DDS DAUGTHER MODULE FOR THE RHIC LLRF PLATFORM *

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Abstract

The RHIC LLRF upgrade is a flexible, modular system. Output signals are generated by a custom designed XMC card with 4 high speed digital to analog (DAC) converters interfaced to a high performance field programmable gate array (FPGA). This paper discusses the hardware details of the XMC DAC board as well as the implementation of a low noise rf synthesizer with digital IQ modulation. This synthesizer also provides injection phase cogging and frequency hop rebucketing capabilities.

INTRODUCTION

A new modular RHIC LLRF system was recently designed and commissioned based on custom designed XMC cards. As part of that effort a high speed, four channel DAC board was designed. The board uses Maxim MAX5891 16 bit DACs with a maximum update rate of 600 Msps. Since this module is intended to be used for many different systems throughout the Collider Accelerator complex, it was designed to be as generic as possible.

One major application of this DAC card is to implement digital synthesizers to provide drive signals to the various cavities at RHIC. Since RHIC is a storage ring with stores that typically last many hours, extremely low RF noise is a critical requirement. Synchrotron frequencies at RHIC range from a few hertz to several hundred hertz depending on the species and point in the acceleration cycle so close in phase noise is a major concern.

The RHIC LLRF system uses the Update Link, a deterministic, high speed data link that broadcasts the revolution frequency and the synchronous phase angle [1]. The digital synthesizers use this data to generate a properly phased analog drive signal. The synthesizers must also provide smooth phase shifts for cogging and support frequency shift rebucketing [2]. One additional feature implemented in the FPGA is a digital waveform generator (WFG) that generates I and Q data pairs based on a user selected amplitude and phase profile as a function of time.

HARDWARE

The DAC card is split into two main functions. A digital "back end" contains a core set of functionality common to all modules in the RHIC LLRF Platform based in a large Xilinx V5FX70T field programmable gate array (FPGA) [3]. The function specific "front end" in this case includes the DAC chips, the clock multiplier and buffer and the output drivers.

In normal operation, the DAC card is supplied with an ultralow phase noise 100 MHz clock from the carrier it is mounted on. This clock is used as the reference to an Analog Devices AD9510 PLL/clock distribution IC which generates the 400 MHz signals that clock the individual DACs.

In keeping with the concept of being generic, the DAC outputs are not filtered. All filtering is done on custom designed analog filter boards. DAC outputs can be either AC or DC coupled based on how the board is populated. Output gain can be adjusted on the DC coupled outputs by means of gain setting resistors. The nominal output level is +10 dBm.

FIRMWARE

As with the hardware, there is some commonality with the firmware of other modules in the LLRF system. A Xilinx MicroBlaze soft processor core controls all communication with the carrier. Other common features include an interface to allow remote reconfiguration of the FPGA and a connection to a 1 GB DDR2 RAM that can be used to store diagnostic data. An "Update Link Receiver" (ULR) decodes the deterministic data and timing events from the "Update Link" .

The WFG is implemented as interrupt driven code running in the embedded Power PC 440. The WFG generates 16 bit I and Q data pairs for all four synthesizers at a 10 kHz rate.

A simplified block diagram of the Direct Digital Synthesizer (DDS) code is shown in figure 1. There are four copies of DDS core instantiated in the FPGA, one for each of the DACs.

A 32 bit word representing the revolution frequency of the particles is received, either from the "Update Link" or manually entered on a terminal. This is multiplied by a 16 bit harmonic number yielding a 48 bit frequency tuning word (ftw). An optional offset frequency is added to form the ftw that is them applied to a 48 bit phase accumulator clocked at 400 MHz that makes up the Numerically Controlled Oscillator (NCO). A 48 bit phase accumulator clocked at 400 MHz yields a frequency resolution of 142 μHz at the revolution frequency and 0.511 mHz at harmonic 360 where the accelerating cavities operate.

Changes to the revolution frequency data is latched on a pulse delivered via the "Update Link". This allows all DDSs across the system to remain locked in phase.

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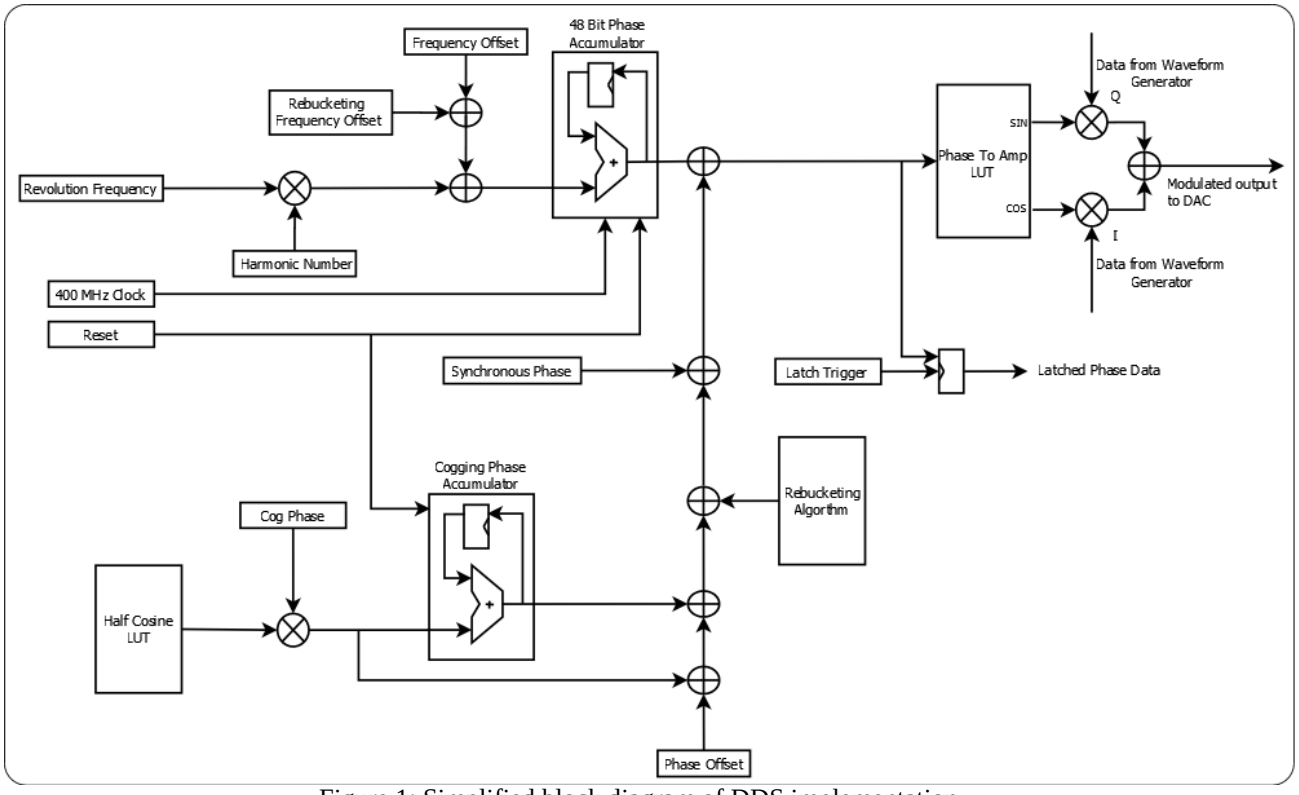

Figure 1: Simplified block diagram of DDS implementation.

The output of the phase accumulator has several additional terms added to it. The offset phase sets the starting phase of the DDS after a reset. Optionally, the synchronous phase, received from the "Update Link" can also be added.

There is also a provision for smoothly shifting the phase. The desired phase shift (the "cog phase") is digitally multiplied by raised cosine data from a look up table so that the scale factor moves smoothly from zero to one. Once the total phase shift has been applied, it is simultaneously latched in the cogging phase accumulator while the "cog phase" parameter is cleared. Latching the phase in this manner allows the cogging mechanism to be used repeatedly without losing any of the previous phase shifts. The rate at which the look up table is accessed is a user controlled parameter that allows setting the time for the total phase shift to be completed. The "cog phase" is a 16 bit value that gives a minimum phase step size of five millidegrees.

One final phase term involves the gymnastic used for frequency hop rebucketing. This is a complex function that allows the synthesizer to jump from an offset frequency to lock to a reference synthesizer with a specific phase relationship. Briefly, an offset frequency is applied to the ftw. On a trigger, the current phase of the DDS is compared to the phase of reference that does not have the offset frequency. A smooth phase shift is applied so that when the offset frequency is removed a fixed time later, the DDS has a specified phase relationship with respect to the reference.

The sum of the NCO output and all of the various phase corrections is truncated to 16 bits that are used to address a phase to amplitude look up table that provides 16 bit sine and cosine values. Due to constraints on the available RAM in the FPGA for the table, it is implemented as a quarter wave table. The lower 14 bits of the truncated phase directly address the table and the upper two bits are used to determine the quadrant and make the appropriate correction. The outputs from the look up table are modulated by the I and Q data from the WFG to form the final 16 bit data word that is sent to the DAC via parallel LVDS signals.

One very important feature of this architecture is the ability to latch the phase data applied to the look up table [4]. Since this latch is controlled by a deterministic trigger received from the "Update Link", this provides a means of making digital phase measurements between any synthesizers in the system.

Another feature not shown in the block diagram includes the ability to set the DAC drive to zero on a trigger. This is used as part of a protection circuit to shut down the drive to a cavity under fault conditions.

RESULTS

Implementing four instances of the DDS core, along with all the other basic functionality, takes up a significant fraction of the total resources available in the FPGA. The design utilizes 70% of the slice registers, 47% of the slice look up tables and 91% of the available

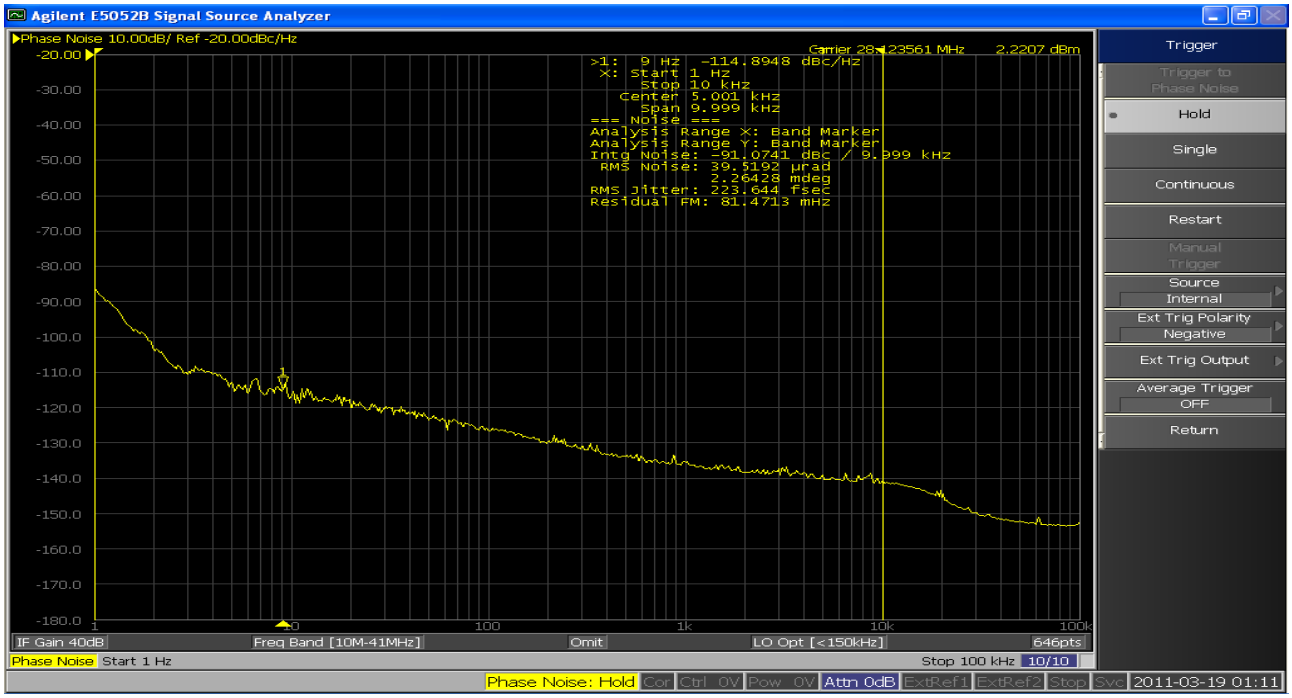

Figure 2: Measured phase noise of DDS with 28 MHz output

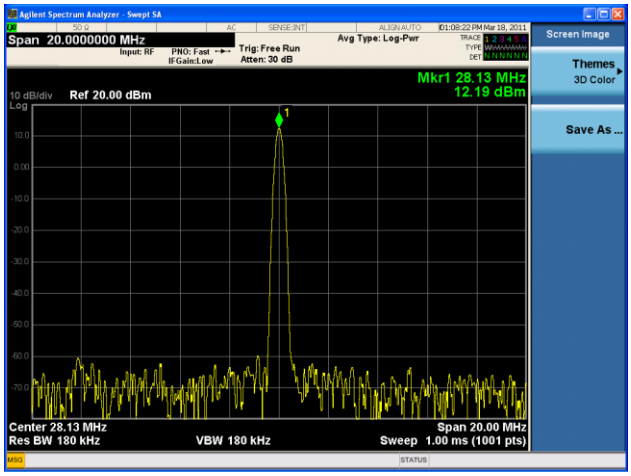

Figure 3: Broad band spectrum of DDS output at 28 MHz

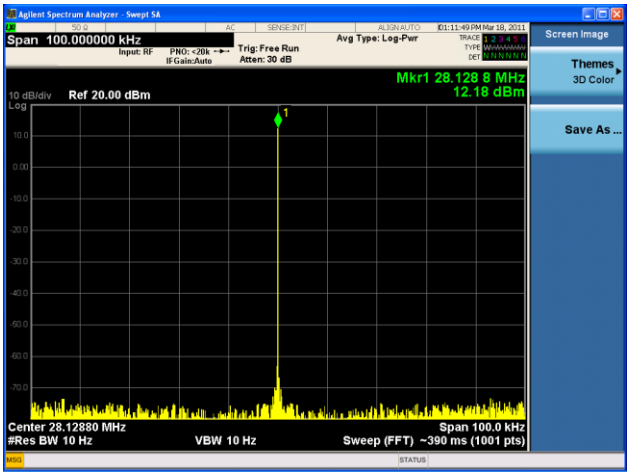

Figure 4: Narrow band spectrum of DDS output at 28 MHz

BlockRAM. Meeting timing in the FPGA at 400 MHz was extremely challenging.

The close in phase noise is extremely good. Figure 2 shows the measured phase noise of the DDS generating the signal used to drive the RHIC 28MHz accelerating cavities. The analog outputs from the DDS are extremely clean. Figures 3 and 4 show the broad band and close in spectrum of the DDS output at 28 MHz.

The ability to measure phases digitally and to smoothly shift phase has been used to implement a "soft" reset feature. In the past, on a reset all DDS NCOs would be cleared, causing the output phase to jump to the starting phase offset. These discontinuous jumps caused problems for some downstream timing systems that were locked to the rf system. Using the flexibility of this system, when a reset is received, all DDSs in the system make a digital measurement of their phase with respect to a common reference. This value is then compared to the nominal reset phase and the phase is smoothly walked in to the correct location.

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