Development of COTS ADC SEE Test System for the ATLAS 

LAr Calorimeter Upgrade

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Abstract: Radiation-tolerant, high speed, high density and low power commercial off-the-shelf (COTS) analog-to-digital converters (ADCs) are planned to be used in the upgrade to the Liquid Argon (LAr) calorimeter front end (FE) trigger readout electronics. Total ionization dose (TID) and single event effect (SEE) are two important radiation effects which need to be characterized on COTS ADCs. In our initial TID test, Texas Instruments (TI) ADS5272 was identified to be the top performer after screening a total 17 COTS ADCs from different manufacturers with dynamic range and sampling rate meeting the requirements of the FE electronics. Another interesting feature of ADS5272 is its 6.5 clock cycles latency, which is the shortest among the 17 candidates. Based on the TID performance, we have designed a SEE evaluation system for ADS5272, which allows us to further assess its radiation tolerance. In this paper, we present a detailed design of ADS5272 SEE evaluation system and show the effectiveness of this system while evaluating ADS5272 SEE characteristics in multiple irradiation tests. According to TID and SEE test results, ADS5272 was chosen to be implemented in the full-size LAr Trigger Digitizer Board (LTDB) demonstrator, which will be installed on ATLAS calorimeter during the 2014 Long Shutdown 1 (LS1).

Key words: COTS ADC, Total Ionization Dose (TID), Single Event Effect (SEE), Single Event Upset (SEU), Single Event Functional Interrupt (SEFI)

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1 Introduction

The ATLAS LAr Calorimeter upgrade project is proposed to enhance the physics reach of the experiment in the high-luminosity environment foreseen in the next 10 years [1]. In order to provide higher-granularity, higher-resolution and longitudinal shower information from the calorimeter to level-1 trigger processors in this upgrade, new LAr calorimeter trigger readout electronics need to be designed, built and installed. Compared to the existing readout cell “trigger tower”, the new readout element called Super Cell [1], which is a 10-fold finer granularity scheme, also provides additional information and more powerful tools to the Level-1 trigger feature extraction. Also, the digitization precision of the Super Cell signals is improved by at least a factor of 4 compared to the existing Level-1 system by optimizing the quantization scale and the dynamic range of the digitizers. These upgrades will be essential to extend the physics potential at higher instantaneous luminosities and the more severe pileup conditions expected after Phase-I and Phase-II upgrades of the LHC.

In the Phase-I upgrade, ~40,000 channels of super cell signals will be digitized at the front end LTDB, and data will be streamed out to the back end DPS (digital processing system). A radiation tolerant ADC is required for signal digitization in the front end electronics. The LAr collaboration has prepared two different technological routes: custom ASIC ADC development and COTS ADC evaluation. Two custom ASIC ADCs are under different stages of prototyping developments. However, given the uncertainty in the development cycle and costs associated with a custom chip design, an extensive study has been conducted for a COTS option that meets both electrical and radiation requirements. Previous studies on the radiation sensitivity to many COTS parts can inform component decisions appropriate for our design. Good experience can be found in Reference [2]-[5].

In this paper, we present ADS5272 [6], a TI COTS ADC as a good candidate for use in the LAr calorimeter electronics upgrade. The electrical features of the ADS5272 include: 65MSPS maximum sampling rate, 12 bit dynamic range, 11.5 resolution (ENOB), 162.5ns (6.5 clock cycles) latency, 113mW power consumption per channel. These parameters meet the digitization requirements [1] of the LAr calorimeter upgrade, and therefore a test program was developed to study the ADS5272 radiation characteristics. The outline of this paper is organized as follows. In Section 2, we discuss the TID radiation effects and their tolerance to an ionizing dose of 17 COTS ADCs. In Section 3, we show the detailed development of the ADS5272 SEE evaluation system, consisting of hardware preparation, firmware development and software application. In section 4, we use our evaluation system to characterize the ADS5272 SEE radiation tolerance in irradiation tests. In Section 5, we conclude this paper, and summarize what we achieved.

2 Total Ionization Dose (TID) Irradiation Test

Long-term exposure to ionizing radiation can cause parametric degradation and ultimately functional failure in electronic devices. The damage occurs via electron-hole pair production, transport and trapping in the dielectric and

![Fig. 1. Diagram of TID test flow](image-url)
interface regions.

To examine the effect of this issue on our COTS ADC, we performed TID tests with a Co-60 solid state gamma irradiation facility at Brookhaven National Laboratory (BNL). We have followed the test flow shown in Fig.1 and the results are shown in Table 1 [7].

Of the six ADCs which withstood doses larger than 1MRad (Si) (showed in the bottom six rows in Table 1), the ADS5272 is the top performer - surviving 8.8 MRad (Si), see Fig.2

Two ADS5272 samples have also been annealed by operating at ~85 degree after more than 2MRad (Si) TID test. After annealing, both ADCs recover to their original characteristics. Fig.3 shows the analog and digital power consumption of sample 2 before and after annealing.

### 3 Single event radiation effects

Since the TID irradiation test results of

<table>
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<tr>
<th>COTS ADC</th>
<th>Dynamic Range [bit]</th>
<th>Max Sampling Frequency [MSPS]</th>
<th>Analog Input Span [V p-p]</th>
<th>Number of Channels per Chip</th>
<th>Power per Channel [mW]</th>
<th>Technology</th>
<th>Vendor</th>
<th>TID [kRad(Si)]</th>
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<td>~220</td>
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<td>Hittite</td>
<td>~1730</td>
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Table 1. Diagram TID test results of COTS ADCs by June, 2012

Fig. 2. Power consumption of ADS5272 #2 during the ~8.8MRad (Si) TID test

Fig. 3. Power consumption of ADS5272 #2 before and after annealing

Fig. 4. A picture of ADS5272 test board
ADS5272 are very promising, we decide to set up an evaluation system for ADS5272 to characterize its single event effects. This system consists of three parts: 1) Hardware - an ADS5272 test board is custom built for SEE test, shown in Fig.4. 2) Firmware - we implement firmware in Virtex-6 FPGA on ML605 [8]-[9], which is generally responsible for acquiring data from the ADC, and controlling and monitoring it. 3) Software - it is developed in MATLAB GUI, which takes care of communication with ML605 through an Ethernet connection, sending configuration information and saving data for analysis in the case of a SEE.

3.1 Design of ADS5272 test board

We have chosen SMA connectors as the input connectors for the ADS5272 test board. The output connector is a Samtec FMC (FPGA Mezzanine Card) HPC connector. This makes the ADS5272 test board easy to attach to the ML605. In order to make the input signals match with the ADS5272 differential full-scale input voltage range, we add an ADC driver in the analog signal chain. The ADC driver is ADI AD8138, which has been qualified up to 500krad TID. The AD8138 output and ADS5272 input are DC coupled with RC low pass filtering to improve the signal-to-noise ratio (SNR). Fig.5 shows the simulation of AD8138 circuit.

The clock scheme for the ADS5272 has three options: SMA input clock, FPGA differential output clock and on board oscillator. ADS5272 needs a LVTTL clock, so we have chosen a Maxim MAX9160 to be a clock fan out driver for all clock input options, which has survived ~15MRad TID.

There are two options for the power supply: an external supply and an on board POL (Point-of-Load) DC-DC converter LTM4616 from Linear Technology. The external power supply is responsible for AD8138 power ±3.3V, ADS5272 analog power +3.3V and digital power +3.3V (contingency), ADS5272 reference voltage REFT +1.95V and REFB +0.95V, ADS5272 common-mode voltage +1.45V, and LTM4616 input +5V. The DC-DC converter LTM4616 can also provide analog and digital power to the ADS5272. A detailed block diagram of the ADS5272 test board is depicted in Fig. 6. It is worth mentioning that we keep a clearance red circle with 3 inches diameter (Fig. 4) around ADS5272 for the requirement of the irradiation test. No other active component is placed in this circle.

3.2 Development of firmware in Virtex-6

Fig. 5. Simulation of AD8138 circuit

Fig. 6. Diagram of hardware development of SEE test system
The firmware of the ADS5272 SEE test system is developed in a Virtex-6 FPGA, which mainly consists of a MicroBlaze (UBLZ) core system and the FPGA fabric logic. The block diagram is illustrated in Fig. 7. UBLZ is a 32 bit RISC (Reduced Instruction Set Computer) embedded processor soft core, which is generated to acquire data from the ADC and compare it with a LUT (Look-Up Table), then buffer the data to DDR3 SDRAM which can be read out through Gigabit Ethernet or USB. The FPGA fabric logic is comprised of five sub-function blocks: ADC logic block, LUT generator block, comparison & SEE detection block, NPI (Native Port Interface) data generator block and UBLZ IO bus interface (IF) block.

The purpose of ADC logic block is to de-serialize ADC raw serial data from serial to parallel (S2P), control and program ADC settings through a serial peripheral interface (SPI) and keep ADC bit clock 90° out-of-phase with respect to the data and frame clock through ADC sampling clock alignment (SCA). SCA function is realized through the adjustment of IODELAYE1 primitive of the FPGA according to associated SNR and noise floor plots.

The LUT generator basically aims to generate a programmable look up table via FPGA embedded block RAM resources. This look up table will be aligned and locked with the ADC waveform before the beam test starts. It is a critical preparation for comparison & SEE detection block.

Real time comparison of ADC data vs. LUT is done in the comparison & SEE detection block. This block can continuously check the difference between the ADC and LUT. When the difference is larger than the preset threshold which is programmable, we will deem the case as an SEE event. An error flag will then be polled to initiate DDR3 transfer and an error counter will start counting.

The NPI data generator block provides logic to compose ADC & LUT data according to PLB (IBM CoreConnect® Tookit Processor Local Bus) timing and data structure rules. The NPI block then sends data to the MPMC (Multi-Port Memory Controller) NPI interface. It also has a verification function to send user test patterns which is permitted by an enable signal (Verif_en) generated from UBLZ IO bus IF block.

The UBLZ IO bus IF block provides a read-write register interface, which is connected as a bridge to a UBLZ processor. It just leverages a simple user logic bus to decode a bunch of transactions. Write operations include transporting configuration information and delay tap values from MATLAB to ADC logic block, and updating the LUT according to the mean value of 100 samples calculated by MATLAB. It
also sets the threshold to detect an SEE event and triggers the DDR3 test transfer as well. Read operations consist of getting values of the ADC registers and SEE error counter, examining SEE error flags and reviewing test patterns.

3.3 Software realized in MATLAB GUIDE

MATLAB can plot the ADC data vs. LUT in real time and display ADC register values on the GUI. It can also monitor the voltage of the power supply and the amplitude of signal generator through Ethernet. This service is very convenient for debugging and testing.

4 SEE Test Results

The ADS5272 SEE evaluation system has been successfully used in multiple irradiation tests. In October 2012, an initial neutron beam test was performed at LANSCE WNR (Los Alamos, NM) with the maximum energy of about 800MeV. The neutron spectrum here is matched to that expected at the position of ATLAS LAr electronics crate. The second test was done in IUCF (Bloomington, IN), which will be presented in Part 4.2, to illustrate the correctness and practicality of the ADS5272 SEE test system. Another test is conducted in Mass General Hospital (Boston, MA) with 216MeV protons. The total SEU cross section observed in these tests are consistent with each other.

4.1 Test setup

The beam tests described above share very similar test set up. We utilize a signal generator to inject a sine wave into ADS5272, which is running at $f_{\text{sample}} = 40\text{MSPS}$. The frequency of the sine wave is about $40\text{kHz}$ ($f_{\text{sample}}/2$).
to ensure enough samples are acquired for each cycle. The FPGA acquires ADC data and compares samples with the LUT in real time. Any deviation larger than a preset threshold will be flagged as an SEE event, and a record of ~4k samples is saved for posterior analysis. The system is synchronized by a 10MHz clock, which is generated by the ML605 board. The test setup diagram is shown in Fig.9 [7].

4.2 Proton Beam Test at IUCF

One SEE test was performed at IUCF with high-flux proton beams on November 30th, 2012. A photograph of the IUCF test is shown in Fig. 10. A total of three ADCs were irradiated with ~200MeV protons to measure both SEU (Single Event Upset) and SEFI (Single Event Function Interrupt) cross sections.

For the SEU (bit flip), ADCs were characterized in no external intervention mode, i.e., a single bit or multiple bits in the data stream flips but ADCs continue to operate normally. Its impact can be examined by the measurement of cross sections. For SEFI, it was recorded when ADCs cease operation - the ADC output remains constant, requiring an external reset to bring it back to normal mode. We should notice that the SEFI here is not equal to a latch up as it doesn’t need a power cycle for the ADC to recover. The ADS5272 can be reset in 200ns without a power cycle.

The first two samples were tested for cross section measurements without any special test conditions. The third sample was tested to evaluate the effectiveness of a mitigation

<table>
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<th>Sample No.</th>
<th>1</th>
<th>2</th>
<th>3</th>
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<tr>
<td>Fluence [×10^{12} p/cm^2]</td>
<td>5.01</td>
<td>4.7</td>
<td>3.02</td>
</tr>
<tr>
<td>No. of SEE Events (SEFI+SEU)</td>
<td>17</td>
<td>19</td>
<td>3</td>
</tr>
<tr>
<td>No. of SEFI Events</td>
<td>4</td>
<td>6</td>
<td>1</td>
</tr>
<tr>
<td>No. of SEU Events (with Single Sample Upset)</td>
<td>13</td>
<td>11</td>
<td>2</td>
</tr>
<tr>
<td>No. of SEU Events (with Multiple Sample Upset)</td>
<td>0</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>Total Beam On Time [s]</td>
<td>1848</td>
<td>1707</td>
<td>1117</td>
</tr>
<tr>
<td>TID [kRad(Si)]</td>
<td>300</td>
<td>281</td>
<td>181</td>
</tr>
</tbody>
</table>

Table. 2. SEE test results of three ADS5272 samples with proton beam at IUCF.
strategy for SEFI and conditions modified to favor SEFI rather than detecting SEUs. A \( \sim 1 \text{Hz} \) hardware reset was issued to clear any register that might be corrupted by SEU outside of the data stream. Test results are listed in Table 2.

The total SEU cross section is \( \sigma_{\text{SEU}} = (4.0 \pm 0.7) \times 10^{-12} \text{cm}^2 \). Although with poor statistics we observe that the upset probability is independent of the bit position in one ADC word (12bits). Therefore we specified SEU cross section in units of area per bit \( \sigma_{\text{SEU}}/\text{bit} = (3.3 \pm 0.6) \times 10^{-13} \text{cm}^2 \). Graphical examples of SEU and SEFI are showed in Fig. 12, Fig. 13 and Fig. 14.

![Fig. 14. SEFI event of ADC, output is a constant value. The ADC recovered to normal working mode after hardware reset](image)

5 **Conclusion**

In this paper, an evaluation system of ADS5272 has been established and its radiation performance has been characterized. From the irradiation test results, the ADS5272 performs very well up to 300 kilorads (Si) TID and up to \( 5 \times 10^{12} \text{p/cm}^2 \) fluence without significant performance degradation. These characteristics meet the radiation tolerance criteria of the COTS component for the LAr calorimeter front end electronics [1]. Therefore, the ADS5272 has been identified as a good candidate to be used in the future LAr calorimeter electronics upgrade, and a demonstrator LTDB is now being designed with this ADC. Valuable experience and information will be obtained from this demonstrator system after installing and running it at the high-luminosity of \( \mathcal{L} = 10^{34} \text{cm}^{-2} \text{s}^{-1} \) on the ATLAS LAr calorimeter.

**Acknowledgment**

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