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Radiation testing campaign results for understanding the suitability of FPGAs in detector electronics.

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Abstract

SRAM based Field Programmable Gate Arrays (FPGAs) have been rarely used in High Energy Physics (HEP) due to their sensitivity to radiation. The last generation of commercial FPGAs based on 28 nm feature size and on Silicon On Insulator (SOI) technologies are more tolerant to radiation to the level that their use in front-end electronics is now feasible. FPGAs provide re-programmability, high-speed computation and fast data transmission through the embedded serial transceivers. They could replace custom application specific integrated circuits in front end electronics in locations with moderate radiation field. The use of a FPGA in HEP experiments is only limited by our ability to mitigate single event effects induced by the high energy hadrons present in the radiation field.

Keywords: FPGA, Radiation, High Energy Physics Experiment

PACS: ??, ??

1. Introduction

In this paper, we summarize results of a two-year study of Xilinx 7-series devices on their susceptibility to a HEP experiment radiation field. Experimental results from irradiation campaigns in the USA and Europe on ionizing dose studies up to 300 krad, and single event effects measurements performed with high-energy neutrons up to $0.6 \cdot 10^{11}$ n/cm² and protons up to $1.5 \cdot 10^{13}$ p/cm², are presented.

To mitigate single event upsets we have implemented techniques such as Triple Module Redundancy (TMR) and soft error scrubbing. The effectiveness of these implementations will be presented in detail.

The paper also gives a preliminary quantification of the errors detected in the FPGA Multi Gigabit Transceivers (MGT). The estimated lane error rate suggests that the configurable logic that interfaces with the MGT is a sensitive part of the FPGA.

1.1. Radiation environment in HEP experiments

In HEP experiments the radiation background is due to a mixed-field of hadrons, electrons and photons. In particular, the expected background for the ATLAS Liquid Argon (LAr) calorimeter electronics is shown in Table 1 for Phase II run [1].

Radiation induced failures on electronics are tested in facilities with particle energy spectra similar to the expected HEP environment and at high rates to find Single Event Effects (SEE)

Table 1: The radiation background in the ATLAS LAr Barrel electronics

	Simulation (one year)	Safety Factor	Test Target* (10 years)
Ionizing Dose	3.0 rad	10	100 krad
1 MeV eq. neutron	$6.0 \cdot 10^{11}$ cm ⁻²	2	$1.2 \cdot 10^{13}$ cm ⁻²
Hadron (> 20 MeV)	$8.5 \cdot 10^{13}$ cm ⁻²	2	$2.0 \cdot 10^{12}$ cm ⁻²

*1 LHC year = 10^7 s, $\sigma_{pp} = 80$ mb, Luminosity = $5 \cdot 10^{34}$ cm⁻²s⁻¹

with small cross sections. Electronic devices will be simultaneously effected by single event effects, total ionizing dose and displacement damages.

1.2. How to provide radiation hardness

FPGAs are sensitive to Single Event Upset (SEU), that is a non-destructive SEE, defined as a change in the logic state of a cell. To avoid this type of error two mitigation techniques are usually adopted: the Triple Modular Redundancy (TMR) and the scrubbing.

TMR is a form of modular redundancy where the hardware resources are triplicated and the result is processed by a majority-voting system. TMR tolerates single faults and many multiple fault combinations and almost always is coupled with scrubbing. The scrubbing architecture performs fault repair, continuously monitoring the configuration memory and repairing SEU within the memory in real-time.

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1.3. Kintex 7 FPGA parameters

Our experiments evaluate Xilinx Kintex-7 XCK7325T chip performance under radiation. Kintex 7 FPGA delivers high signal processing capability and low power consumption. These devices contain 326K of logic cells, 16 Mb of BRAM, 400K User FFs, 840 DSP Slices, BRAM Built in Error Correcting Code (ECC), 1.0 V core voltage, 16 GTX transceivers (MGTs).

The rad-hard techniques adopted during the experiments must prevent build up of errors in different FPGA parts.

For this reason different parameters were measured: FPGA supply voltages and currents, configuration RAM (CRAM) cross section, block RAM (BRAM) cross section and data link failure rates. During the experiments, CRAM and BRAM data were continuously read through JTAG interface. New data file were compared with the previous data file and the number of differences between the two files were recorded.

2. Experiments

Experiments with different radiation sources were performed on Kintex 7 FPGAs. The first test was done with a mixed-field source (H4IRRAD) at CERN, where the energy spectrum is similar the LHC radiation environment. Then tests with neutrons (LANSCE - WNR, Los Alamos) and protons (The Svedberg Laboratory (TSL) in Uppsala, Sweden) sources were done to better understand the differences between displacement and ionizing damages. Table 2 summarizes all the results:

Table 2: Cross section comparison

	CRAM (cm ² /bit)	BRAM (cm ² /bit)	Fluence (particle/cm ²)
H4IRRAD* (Hadron)	$1.50 \cdot 10^{-14}$	$1.40 \cdot 10^{-14}$	$1.8 \cdot 10^9$
LANSCE** (Neutron)	$6.89 \cdot 10^{-15}$	$6.15 \cdot 10^{-15}$	$5.7 \cdot 10^{10}$
TSL (Neutron)	$6.55 \cdot 10^{-15}$	-	$> 5.7 \cdot 10^{10}$
TSL*** (Proton)	$8.29 \cdot 10^{-15}$	$8.19 \cdot 10^{-15}$	$1.3 \cdot 10^{13}$

*H4 normalization has an error of 50%.

**LANSCE normalization has an error of 18%.

***Ionizing dose deposited on the DUT > 300 krad.

2.1. H4IRRAD results

H4IRRAD is one of the few mixed-field (hadrons and neutrons) test area available and could deliver an attenuated primary 400 GeV/c proton beam from CERN SPS or secondary beam of 280 GeV/c proton beam over Cu target.

Unfortunately, there is a large uncertainty on the total particle fluence at DUT position because of the not well known ionization dose deposited by hadrons. CRAM and BRAM static cross section were measured during the test, as shown in Table 2, while current monitoring and MGTs testing were not performed.

2.2. Neutron results

Two tests were performed with a neutron source. The first test at LANSCE has maximum energy of 800 MeV and the second test at TSL has maximum energy of 200 MeV. Both experiment allowed to simulate neutrons spectrum similar to cosmic ray background.

The mitigation strategies implemented on the DUT are the TMR and the multi-level (internal and external) scrubbing. Parameters under test were BRAM and CRAM cross sections and results are shown in Table 2. Some preliminary tests were also done on MGT data transmission. Approximately, 6 links failures were observed not correlated with error types. More details on MGT failures are studied with proton tests.

2.3. Proton results

Two different experiments were performed at TSL laboratory with 180 MeV protons to re-measure the CRAM and BRAM cross section and evaluate the performance of the GTX transceivers of a Kintex 7 FPGAs. Proton beam is useful to simulate the complex radiation environment expected at the LHC accelerator. Protons deposit ionization dose and induce displacement damage.

In the first experiment, the parameters under test were BRAM and CRAM. Results shown in Table 2 confirm the cross sections obtained with neutrons. In the second experiment several bidirectional lane were tested with configuration scrubbing without TMR. A lane error cross section of $7.27 \cdot 10^{12}$ errors/lane/p/cm² was estimated. Some MGT errors could probably be prevented by applying mitigation techniques, such as TMR. More experiments are planned to quantify this assumption. No significant functional errors were observed after exposing the board to $1.3 \cdot 10^{13}$ proton/cm² of fluence. Ionization dose deposited during the experiment exceeded 300 krad.

3. Conclusion and outlook

The results presented summarize a two years long study which is still on going. Permanent operational failures were never observed up to the level of radiation to which the FPGA was exposed. CRAM and BRAM cross section results indicate that TMR plus multi-level scrubbing are essential to mitigate SEU in Kintex 7 FPGAs. The estimated MGT lane error rate is probably related to errors in the configurable logic which interfaces with MGT. Application of mitigation methods, not applied during our tests, could reduce this sensitivity. Future experiments are planned with improved TMR and scrubbing mitigation strategies to further reduce the present error rates. We are working towards also implementing a test board in ATLAS to gather more realistic data.

Bibliography

- [1] M. J. Wirthlin, H. Takai, and A. Harding, "Soft error rate estimations of the Kintex-7 FPGA within the ATLAS Liquid Argon (LAr) Calorimeter", Journal of Instrumentation (JINST), vol. 9, no. C01025, 2014.
- [2] Xilinx Corporation, 7 Series FPGAs GTX/GTH Transceivers: User Guide, February 11 2014, UG476 (v1.10).