



Modeling and Simulation Challenges of Neuromorphic Architectures







Suma George Cardwell

Cognitive and Emerging Computing

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FUNDAMENTAL CHALLENGES IN COMPUTING

- Limits of scaling have ushered in the "Golden Age of Computer Architecture" Hennessy & Patterson 2019
- Inefficiency of generality

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- Performance saturation
- Growing demands for HPC and SWaPconstrained edge computing



Neuromorphic Computing gives a path forward for power efficiency scaling and meeting future computing needs. GD

COMPUTING LANDSCAPE





Intel Loihi Davies 2018

SpiNNaker Furber 2016



GT Neuron Brink 2013



DAVIS 240C, DYNAPSEL



NeuroGrid Benjamin 2014



Marinella et al., 2016



Mott- Memristor Kumar et al., 2020



NEUROMORPHIC COMPUTING: INSPIRED BY THE BRAIN



Neuromorphic techniques

1MMAC/(s)/mW

1MMAC/(s)/uW

1MMAC/(s)/p

Analog/ Compute-inmemory techniques Hasler 2016

Neuromorphic techniques will be disruptive to how we develop our computing systems

MMAC: Million Multiply Accumulates

components

Online learning

Transfer learning

computation

Self-organizing system

NEUROMORPHIC COMPUTING: DIVERSE SOLUTIONS

Digital Neuromorphic



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Intel Loihi/ Loihi 2.0



SpiNNaker/ SpiNNaker 2



IBM TrueNorth ODIN (Open-source)

Analog/Mixed-Signal



GT supercomputer Neuron

million neural

neurons



Stanford Neurogrid





NeuRRAM UCSD/Tsinghua





Beyond CMOS Devices



ECRAM



Neuron Biological Dentrite Soma Axon Brink et al., 2013

6 NEUROMORPHIC BUILDING BLOCKS



Learning Synapses



Many different models for neurons, synapses, online learning and dendrites. Neuromorphic offers computational richness we can leverage, to move beyond today's computational limitations.

Neural Path

Planning

Koziol et al.

2013

Dendritic Processing



George Cardwell et al. 2013



Liu et al. 2020

Silicon Retina/ Event Sensor



Delbruck et al.

Nie in

Winner-Take-All

Lazzaro et al.

Random Walks

Smith et al. 2021

Fig. 1 Lazzaro WTA circuit

1988

APPLICATIONS

F



AI/ML (ANN, SNN)



Brain-inspired algorithms



Scientific Computing



CHALLENGE: SCALABILITY VS. COMPLEXITY



However, to achieve brain-like complexity we need both scaling and rich dynamics.

Solving ill-structured problems

- Online learning
- Transfer learning

Understanding fundamental mechanisms in neuroscience, translated to algorithms and models will influence next-generation devices, architectures and intelligent computing systems

Scalability (# of Neurons, Synapses)

INCREASING "BIOLOGICAL COMPLEXITY"

Increase computational efficiency and Increase computational density

Novel devices and materials can help bridge this gap.

LIF neuron

- Single passive compartment
- Spikes

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- Limited dynamics
- Relatively easy to scale

LIF: leaky Integrate and Fire

Biological neuron

- Dendrites = intricate structure and dense connectivity
- Complex pattern of active conductances
- Rich dynamics , multiple patterns of spiking, subthreshold computation
- More computational power, not compact



Dendrites are tree-like structures that connect neurons synapses to its soma.

Dendrites are not *just* **wires**!

They can perform interesting computation like:

- Coincidence Detection
- Current Summation

g

- Directional selectivity
- Non-linear filtering
- Amplification of Synaptic inputs

London 2005, Poirazi 2020





SINGLE NEURON MULTIPLICATION



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Groschner et al., Nature 2022

Leveraging Inhibition

Shunting Inhibition/ Leveraging Leakage Conductance





Lobula giant movement detector (LGMD) of locusts Gabbiani et al., Nature 2002

Multiplication based on dendritic subtraction of two converging inputs encoded logarithmically, followed by exponentiation through active membrane conductances.

SINGLE NEURON MULTIPLICATION





Physics of

ms Devices & Circuits Physics of Computing

(in)



Lu et al. 2022

Chance & Cardwell NICE 2023 Shunting Inhibition in Neuromorphic Dendrite

NEUROMORPHIC CODESIGN 12



Intel's Loihi

Coordinate transformations from Dragonflies to Neuromorphic Hardware

Lead PI: Frances Chance, SNL





Gonzalez-Bellido, UMN

DRAGONFLY **EXPERIMENTS**



Increased collaboration between neuroscience and neuromorphic engineering will facilitate development of novel neural-inspired architectures.



SNL, Baylor

NEUROMORPHIC

IMPLEMENTATION

Davies 2018

George



DOE ASCR (FY21-24)

Department of Energy Advanced Scientific Computing Research



DRAGONFLY INTERCEPTION WITH DENDRITES







ORD

16 DIRECTION-SELECTIVE CELLS FOR COMPLEX PATTERNS





V1

Optic Flow Estimation





MT (Middle Temporal)

dorsal medial superior temporal MSTd 

Steinmetz et al. 2022

7 CHALLENGE: CODESIGN TOOLS

Co-Design Tools for Novel Architectures

Next-generation Neuromorphic Architectures











ATHENA SANA-FE **AI-Enhanced COINFLIPS Probabilistic Neural** Analytical Tool for Neuromorphic Codesign analog and Architecture Reinforcement Computing, neuromorphic Exploration Learning/Evolution Leverage stochasticity in ML accelerator ary for Circuit and beyond-CMOS devices System design

DRAGONFLY Dendritic processing, Coordinate transformation from Dragonflies to Neuromorphic hardware,

ASC-AML (FY20-22)

SNL LDRDs (FY21-24)

SNL LDRDs (FY21-23)

DOE ASCR/BES (FY21-24)

DOE ASCR (FY21-24)

External Collaborators: UT Austin, Intel, NCSU, Infineon Memory Solutions, Georgia Tech, UMN, Baylor University, UT Knoxville, Temple University, NYU, ORNL

ATHENA : ANALYTICAL TOOL TO EVALUATE HETEROGENEOUS NEUROMORPHIC ARCHITECTURES



- ATHENA will quickly evaluate performance metrics of analog architectures
- Developed as part of a larger ecosystem
 - Tools to enable nextgeneration hardware design prototyping.

Plagge et al., International Conference on Rebooting Computing (ICRC) 2022



ATHENA – HARDWARE PERFORMANCE





Plagge et al., International Conference on Rebooting Computing (ICRC) 2022

- ATHENA was used to compare the performance of multiple hardware devices against various deep learning networks
- The SONOS tile-based architecture performed well across networks, with one notable exception: the Inception v3 network
- This performance difference could be explored – showing ATHENA's potential for codesign work.
- In the process of making ATHENA open-source.

SANA-FE: Simulating Advanced Neuromorphic Architectures for **Fast Exploration**

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SANA-FE



Boyle et al., ICONS 2023

SPIKING ARCHITECTURE TEMPLATE

Tile-based architecture

Network-on-chip connecting neural cores

Many cores per tile

- Cores simulate group of mapped neurons
- Local shared memory

Core pipeline

- Axon stage
- Synapse stage
- Dendrite stage
- Soma stage



CHALLENGE: ARCHITECTURE DESCRIPTION

Describes different H/W architectures

- Represents different existing & future spiking designs based on common features
- Defines compute elements of chip
- YAML-based, flexible & extensible



```
architecture:
name: demo
tile:
  name: demo tile[0..7]
   attributes:
    energy east west: 1e-12
    latency east west: 2e-9
    . . .
   core:
    - name: demo core[0..3]
      soma:
       - name: core lif
         attributes:
          energy spiking: 68e-12
          latency spiking: 30e-9
```

PERFORMANCE MODELING RESULTS

For randomized spiking inputs on the application SNN



- Detailed breakdown of on-chip activity on Loihi
- Captures dynamic energy and latency trends

Detailed insight into H/W behavior

Boyle et al., ICONS 2023

RESULTS FOR OTHER NEUROMORPHIC BENCHMARKS

Predict performance & energy for larger real-world neuromorphic applications

- SNN trained on DVS gesture data-set
- 18,678 neurons across 6 layers

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Mapped to 45 Loihi cores out of 128



Image reproduced from [Massa,'20]



SIMULATOR SPEED RESULTS

• Compared to existing spiking simulator (NeMo)



- Simulating IBM TrueNorth architecture
- Randomized SNN with 80% of spikes intra-core, 20% spikes between cores
- Over 10x faster than NeMo for 1024 cores

SANA-FE 26

- User-defined architecture & SNN
- Supports range of spiking architectures

Fast & accurate

- Time-step based approach
- Detailed hardware activity for each time-step
- Accurately estimates performance & energy

Future work

- Support other existing architectures & scale to larger designs
- Adapt other neuromorphic benchmark applications
- Model analog architectures & novel devices
- Integrate with other frameworks e.g., SST, Fugu & Lava

Access at: <u>https://github.com/SLAM-Lab/sana-fe</u>

Prof. Andreas Gerstlauer's SLAM Lab @ UT Austin





Boyle et al., ICONS 2023



Collaborators: NYU, ORNL, Temple University, UT-Austin and UT-Knoxville

https://coinflipscomputing.org/

U.S. DEPARTMENT OF

AI-GUIDED CODESIGN OF PROBABILSITIC CIRCUITS 🛛 🔛 🐺 🛅



Unfair coins can be combined with Al-designed neural circuits to allow sampling of application desired probability distributions, avoiding accept/reject steps.

We leveraged evolutionary algorithms for circuit design and optimization

- LEAP (Library of Evolutionary Algorithms in Python)
- EONS (Evolutionary Optimization for Neuromorphic Systems)- Schuman et al., 2020

We used abstracted device models for TD and MTJ to capture functionality and energy usage.

Cardwell et al., International Conference on Rebooting Computing (ICRC) 2022

29 AI-GUIDED CODESIGN OF PROBABILSITIC CIRCUITS





Probabilistic Mixing Algorithm

Optimized weight values for each device



Multi-objective optimization of weights of fitness function for optimal KL divergence, biased weight and energy usage.

Cardwell et al., International Conference on Rebooting Computing (ICRC) 2022 Weights are customized for the device's behavior to target the best performance in terms of KL divergence and energy usage.

One of the challenges in optimizing for both algorithms and devices was appropriately abstracting the device models and algorithmic constraints.

The functional models developed will also be evolved in time as new device data and research emerges.

Our framework can accommodate any emerging device type.

We developed an RL algorithm approach which is capable of building very simple circuits.



Algorithms

Pattern

Detection

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In 4

Tap 4

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Physics of Computing





CHALLENGES FOR NEXT-GENERATION OF NEUROMORPHIC SYSTEMS

- Algorithms are cognizant of architecture and device constraints.
- Leverage the complex dynamics of devices.
- Bio-inspired techniques, adoption in computing
- Software tools to support design and development

- Integration with AI-enhanced techniques?
- Leverage the physics of devices to do computation (analog)
- Embrace stochasticity of devices
- Analog devices are noisy. How can we incorporate this into algorithms?



- Heterogeneous architectures
- CoDesign to optimize communication and memory bottlenecks
- 3D architectures, Photonics
 - How can Al-enhanced techniques accelerate scientific discovery?
 - Different AI techniques at the device, circuit, system design and architecture level.
 - Enable encoding of domain knowledge
 - Enable concurrent contribution
 from researchers
 - Novel devices with complex dynamics
 - Radiation-hardened devices
 - Reconfigurable devices
 - Computational efficiency and computational density









Careers

Neural Exploration and Research Lab

careers.sandia.gov https://neuroscience.sandia.gov/

Suma G. Cardwell <u>sgcardw@sandia.gov</u>

FUTURE OF COMPUTING: HETEROGENEOUS ARCHITECTURES





Co-Design is critical to build the next-generation heterogeneous systems



'Truly Heterogeneous Computing', Cardwell et al., SMC 2020

DENDRITES



Resistor-Capacitor Circuit



Rall's Cable Model







For a particular collider physics simulation [Pierog et al., Phy Rev. 2022], ~ 270K pseudo- random numbers needed for a single event, with billions of events needing to be simulated.

CPU time is ~ 30-50% of the total compute time

Direct random number generation leveraging stochastic devices can promise significant energy savings for such applications

Misra et al., Advanced Materials 2022

Random numbers are a limiting computational cost for some nuclear physics applications