

# **Enabling Systematic Deep-Learning Architecture Evaluation via Full-Stack Integration**

### **Motivation**

- DNN accelerators are often developed in isolation, without considering the crossstack, system-level effects in real workloads.
- DNN accelerators must cope with
  - SoC resource contention
  - Data movement across cores/accelerators
  - OS overheads
  - Programming stack inefficiencies
- At the SoC level:
  - Memory hierarchy: resource contention, cache coherence
  - Virtual Address Translation: page faults, TLB latency
  - Host CPUs: unaccelerated kernels



Across the programming stack:



Enable full-system evaluation and designspace exploration

## The Gemmini Infrastructure

- Flexible hardware template
  - Spatial array: dataflow, dimensions, pipelining

  - Scratchpad: capacity, banks, single- or dual-port
  - Virtual address translation
  - Host CPU
  - Memory Hierarchy





# **Measured Performance**

- Using cloud-based FPGA
  - ResNet50: 40.3 FPS
  - AlexNet: 79.3 FPS
  - MobileNet: 18.7 FPS
  - BERT: 167x speedup



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Non-GEMM functionality: transpose, im2col, ReLU...

# Gemmini

### **Case Study: Virtual Memory**

- Gemmini enables researchers to investigate virtual memory in accelerators.
- We can configure Gemmini to include a two-level TLB hierarchy, with one private TLB for the accelerator and one larger shared L2 TLB.
- Accelerator's TLB miss rate can be ordersof-magnitude higher than the one in CPUs for non-DNN benchmarks.



- Small, private TLB is much more impactful.
- Low-cost optimization:
  - Single-entry L0 TLB filters out consecutive TLB requests to the same page





SoC

Private

CPU TLB

Shared L2 TLB



## **Case Study: Memory Partition**

Gemmini enables application-system codesign for real-world deployment Memory partition strategies in SoCs



Config	Scratchpad	Accumulator	L2
Name	(per core)	(per core)	Cache
Base	256 KB	256 KB	1 MB
BigSP	512 KB	512 KB	1 MB
BigL2	256 KB	256 KB	2 MB



### To appear at DAC 2021 **Best Paper Candidate** https://github.com/ucb-bar/gemmini