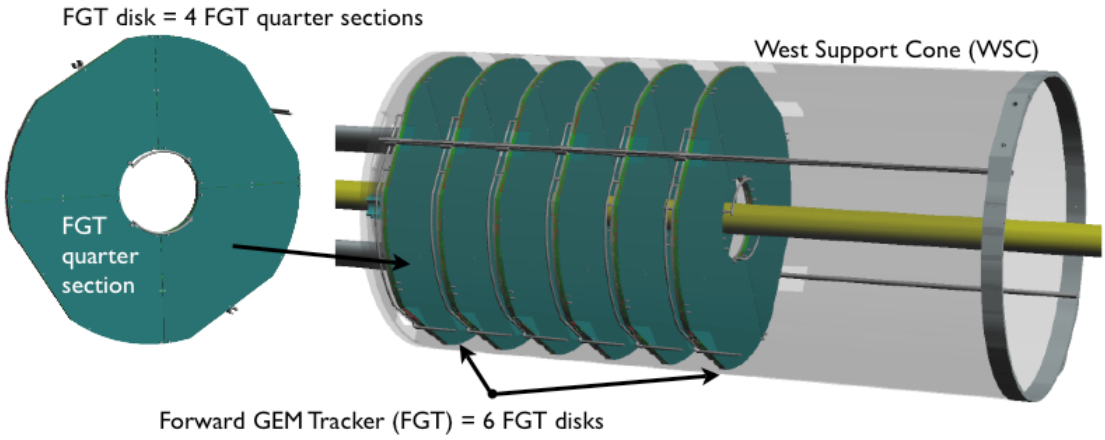
Project Name: STAR-FGT Date: April, 2009
Federal Project Director:
Contract Project Manager: Bernd Surrow, MIT

Reminder of some nomenclature:



The above sketch is taken from the FGT implementation into SolidWorks design and is meant to clarify the basic FGT nomenclature.

Narrative of project highlights:

Milestone: WBS1.1.1.1
Description
Quarter section design complete
Projected completion date: FY08 4th Quarter

Comments: All aspects of the quarter section design are completed. The final layout requires fixing the outer radius of the WSC, which is expected to occur by summer 2009 as part of the STAR integration effort. More details on the quarter section design are provided below in the section on 'Triple-GEM detectors'. The WSC design status is discussed in the section on 'Integration.'

Milestone: WBS1.1.1.7
Description:
Full-size GEM foils tested and meet specifications
Projected completion date: FY09 1st Quarter

Comments: Tech-Etch Inc. has delivered at the end of the FY09 1st Quarter eight full-sized GEM foils according to our design of a full FGT quarter section. Simple quality assurance tests (HV and optical inspection of some regions) were performed by Tech-

Etch. We will perform HV tests and measure inner and outer hole diameters (related to gain uniformity) on a large number of GEM holes.

Brief summary of project status, issues, concerns, successes:

The following summary is separated according to the main WBS categories:

1 Triple-GEM detectors:

We have received eleven (11) GEM foils from Tech-Etch according to the full-size prototype design. Eight (8) of these were identified by Tech-Etch as "good" and three (3) "bad" foils were provided, at our request, testing our jigs and fixtures.

Visual inspection of the GEM foils indicated that the GEM holes in the copper were offset from the holes in the Kapton by up to 10 microns in some areas of the foil. This could be explained by a misalignment between the processes etching the top and bottom copper layers. The misalignment is not a simple translation but also involves a rotation. In discussion with Tech-Etch they explained that the lithography used for the GEM foils is a laser direct imaging technique which has a 0.0005" tolerance consistent with the 10 microns observed. It is not clear whether or not this offset will affect the performance of these foils in a GEM detector. Nevertheless Tech-Etch is investigating better alignment techniques.

Tech-Etch provides the GEM foils centered on a piece of Kapton measuring 18" x 22". In order to retain the extra material for handling (particularly in the stretching and gluing fixture) the HV test box had to be redesigned. This has been completed and testing the GEM foils for continuity, resistance, and dark current has begun. Tech-Etch performed similar tests before shipping the foils and used this to determine "good" foils.

Similarly, a new fixture for the detailed measurements of the GEM hole diameters using a CCD camera had to be designed and fabricated. The GEM hole diameter is critical for the gain of the foil and must be uniform across the large area of these new foils. The new fixture is ready and testing has begun.

The stretching and gluing fixture has been designed and is nearly complete. Frames for the full-size GEM detectors have been made. Tests using the stretching and gluing fixture will begin shortly to verify that the GEM foils can be glued to the frames and that flatness is maintained as the GEM detector is assembled. Initial tests will use plain Kapton before starting the assembly of a real GEM detector.

To determine the correct line width and pitch combinations which yield a 1:1 charge sharing between the top and bottom layers of the 2D readout layer a 10 x 10 cm^2 test board was designed and fabricated. This test board has 16 different combinations of line width and pitch for the top layer and has been assembled into one of the FNAL prototype GEM detectors. The charge sharing 2D readout board was also designed to accept the new APV board design and thus can be used to test these as well. Five (5) APV boards

have been produced recently and the APV chips bonded. Electronics for reading out the APV boards has being developed but this must be integrated with some software to provide a simple data acquisition system. When this is completed the proper combination of line width and pitch for the full-size 2D readout board can be determined and designed. This simple readout system can be used to test the APV boards and, in the future, test completed GEM detectors and be used in a cosmic ray test station.

In order to verify the proposed design for cooling the FGT front end electronics a full-size thermal model has been designed and largely built. Plywood disks simulate the GEM detectors and entrance and exit of the west support cylinder. Simple PCBs with heating resistors generate the heat load of the APV, interconnect, and HV distribution boards. A PVC pipe simulates the enclosure around the beampipe and cooling air input. Plastic sheeting 1/8" thick is used to represent the West Support Cylinder (WSC). Over 120 thermisters will be attached throughout the model and read out via a pair of Keithley multi-channel DVM's. Air flow between disks and the heat load of each disk can be varied individually. Testing should begin in a few weeks. In addition this model reproduces the actual cabling of the FGT and can be used to design the cabling of the SSD which also comes through this volume.

Contact has been made to the photolithographic workshop at CERN and an order of 12 large GEM foils specific to the FGT project has been made. This will allow one to provide an important comparison to large foils produced by Tech-Etch.

2 Front-End Electronics:

All APV25 readout chips on 8 large wafers including a significant number of spares have been purchased and are located in the silicon clean room at the Laboratory for Nuclear Science at MIT. One wafer has been diced by American Precision Dicing in San Jose, CA. Six diced dies were randomly chosen and mounted on a Kapton hybrid. These chips are currently being tested for functionality. If successful, the remaining 7 wafers will also be diced.

A unified front-end board, APV module, has been designed and five boards have been produced by Accent Technologies in North Andover, MA and bonded by Solid State Testing, Inc. in Billerica, MA. This APV module has 5 APV25-S1 readout chips, can read out 640 channels and can be plugged into the actual FGT quarter sections using standard (SAMTEC MEC6) edge connectors. In an effort to reduce the overall cost, the preference was to use industrial printed circuit board techniques (FR4). However, the small bonding-pad pitch of the readout chip and the minimum trace width on FR4 (2mil/2mil) made it necessary to go to a multi-level board design. All passive components were moved into depressions on the backside of the board in order to avoid soldering contamination of the bonding pads on the front side of the board. The board design can be considered challenging, but didn't pose any fabrication or bonding problems. All 5 modules were tested successfully.

The APV modules will be used for both the FGT prototypes and a charge sharing test board. The charge sharing board has already been produced and will be equipped with the tested APV module boards. The read-out system of the APV modules is realized by using existing electronics, which was designed for the FGT test beam experiment at FNAL.

The APV module is the prototype of the final front-end board of which two will be used on each FGT quarter section. The design and production of the final FGT front-end module will start, once the functionality tests of the APV module on the FGT prototypes have been completed successfully. These tests and the charge sharing board tests will take place in the next 3 months.

3 Data-Acquisition System:

In the past four months considerable progress has been made on the FGT readout/DAQ system. Most importantly, a meeting was held between the IUCF and ANL engineers, defining in broad strokes all the interfaces between the readout modules (ARM) and the readout controller (ARC) and the crate. An interface document is in progress to finalize all the details such as pinout, timing, signal protocols, etc. Also at this meeting we discussed the STAR trigger and DAQ interfaces. The second major item of progress was the completion of the "APV long cable test setup" – a pair of printed circuit boards to be used in conjunction with the MIT front end board to demonstrate the successful operation of APV chips over a long cable. These boards are now assembled and being tested – at first using a single APV chip mounted as with the Fermilab test beam setup – then as soon as it is available to us we will switch to using a prototype FGT front end board. Tests are being conducted with a 110 foot cable, about 45% contingency over the most likely proposed run. To date, the voltage regulators and clock and trigger interface has been verified, one of the two alternative analog line receivers has been verified, and the opto-isolated UART-I^2C bridge is now functional. The next step is to connect an APV chip and configure it, and then finally to run the APV chip and verify noise level, crosstalk, etc. The schedule called for this to be complete April 15th, so we are running slightly behind. It is an important milestone, on which both our official request for rack allocation and the readout crate procurement is waiting.

The proposed ISEG high voltage module, which will share the same crate mechanics as the readout crate, was evaluated as to output voltage ripple and it is satisfactory. A decision is needed (outside the scope of DAQ section) whether 4kV or 5kV – at cost of higher ripple and a need to set hardware limit to stay within SHV connector rating – is required for the FGT bias voltage; then the HV modules can be procured together with the crate. Some progress was made in the area of low mass cabling for the FGT and SSD (cables from the latter must route through the west cylinder and contribute mass in the same η regions as the FGT cables and structure). Most importantly, in conjunction with the HFT internal technical review we have a definition of cables for both detectors and are incorporating them into mechanical models. Another outcome of the "APV long cable test setup" will be the final definition of the electrical requirements. Some further

discussion is needed with the cable vendor (Calmont Wire & Cable Co.) to settle the issue of stranded versus solid copper-clad aluminum conductors, and then we will procure the inner cable. A commercial off-the-shelf copper & foam polyethylene signal cable is identified for the external cable run and a similar type is in hand for the long cable tests. In regards to the readout board, the analog line receiver circuit is being prototyped now, a selection table of candidate ADC components is started, the crate clock phase adjustment circuit is designed (intended also for use in a new TCD module for STAR), and FPGA and backplane bus interface components are selected.
Items that will be addressed within the next ½ year include, principally:

- Operate APV's on a long cable, determine tolerable cable length. Make final go/no-go decision for platform mounted readout electronics. Test/optimize the interfaces for readout module (ARM).
- Produce a final prototype "cable connector board" to interface the MIT front end boards to the cable. This will include the voltage regulators and clock buffer and UART-I^2C bridge.
- Enter into final agreement with STAR operations on FGT rack location (tentatively 3A9 to be installed) and cable routing.
- Procure crate and HV modules.
- Final design of custom copper-clad aluminum cable; procure cable.
- Complete the requirements and interface document for the ARC module.
- Final selection of line receiver, ADC, FPGA, and isolated power supply components for the readout module [IUCF]. Procurement.
- Final selection of FPGA, SDRAM, backplane interface components, and PLL / clock phase adjust components for the readout controller [ANL]. Procurement.
- First pass design of readout controller (ARC).
- First pass design and layout of readout module (ARM).

4 Integration:

The west support cone (WSC) has been modified to have a larger inside radius to allow for an enlarged GEM active area. This inner radius has been fixed at 39.63 cm. The support structure will be connected to the TPC wheel using the same mounting flange as is currently installed in STAR, thus allowing the use of existing installation tooling. A second WSC will be assembled as a mirror image and used as the east support cylinder (ESC). Centered between the ESC and WSC will be the outer support cylinder (OSC) which supports both the SSD and IST sensors. The OSC will be connected to the outer cones by means of conical transition plates, which will be bolted at both ends. To reduce the electric field between the WSC and the inner field cage (IFC), a bias voltage of 3-6 kV will be applied to the WSC. Also, a smooth shroud will be installed and biased near these bolted connection. Current work is being done on the detailed design of this support structure. It is still planned to use carbon fiber for the entire structure, with the exception of titanium for the fasteners.

In addition to physically supporting the GEM disks, the WSC will allow routing and mounting of all FGT electrical and cooling services, and a portion of the SSD power and signal cables. The size of each cable and cooling hose has been determined and have been shown to easily fit in the spaces around the GEM disks. Testing with the full-scale thermal model will help determine the optimal routing paths for these services to obtain adequate cooling with a minimum air flow. This thermal model is under construction and is expected to be operational by the end of April 2009.

The proposed method for cooling the SSD requires the passage of ambient temperature air between the WSC and the IFC, which is then exhausted through the east end of STAR. This arrangement has been approved by the SSD group.

Detailed design of the WSC/ESC has been a collaborative effort between MIT and LBNL and is estimated to take an additional 3 months. The construction of the two cylinders will occur at LBNL with the support of MIT engineers. It will require up to one year for manufacture. This will be followed by the installation, testing, and integration of the FGT and HFT components. It is therefore not possible to install the FGT in summer 2010, but rather the summer of 2011.

5 Infrastructure:

The design of a slow-control system for the FGT has been started based on the existing type that the STAR experiment is already using. The cooling system design is the focus of a full thermal model, which has to be finalized in connection with the cooling needs of the STAR SSD detector system as part of the STAR HFT project. The gas system is rather simple for the FGT and the current plan is to have an independent implementation and not use the existing FTPC gas system, since this system might be re-installed at a later stage as part of a dedicated low-energy running request.

Summary of total expenditures:

WBS	Item	Baseline Total Cost (AY$)	Costed & Committed (AY$)	Estimate To Complete (AY$)	Estimated Total Cost (AY$)	Baseline Contingency (AY$)	Remaining Contingency (AY$)
1.1.1	Design and Prototyping	167.4	30.1	69.1	99.2	33.4	101.6
1.1.2	Procurement	270.1	-	270.1	270.1	56.7	56.7
1.1.4	Tooling	2.0	4.1	2.0	6.1	0.4	-4.1
1.1.5	Machining	4.1	-	4.1	4.1	0.8	0.8
1.1.6	Assembly	19.3	-	19.3	19.3	3.9	3.9
1.1 Total	**Triple-GEM Detector**	**462.9**	**34.2**	**364.6**	**398.7**	**95.2**	**158.9**
1.2.1	Design and	90.4	24.8	65.6	90.4	18.1	18.1

	Prototyping						
1.2.2	Procurement	134.2	45.2	84.2	129.4	36.8	41.6
1.2.4	Assembly	62.8	-	62.8	62.8	12.5	12.5
1.2.5	Testing	62.8	-	62.8	62.8	12.6	12.6
1.2 Total	**Front-End Electronics**	**350.2**	**70.0**	**275.4**	**345.4**	**80.0**	**84.8**
1.3	**Data Acquisition**	**299.3**	**-**	**299.3**	**299.3**	**60.3**	**60.3**
1.4.1	Gas system	32.9	-	32.9	32.9	8.6	8.6
1.4.2	Air flow system	27.9	3.6	24.3	27.9	6.5	6.5
1.4.3	Slow controls	20.9	-	20.9	20.9	5.2	5.2
1.4	**Infrastructure**	**81.7**	**3.6**	**78.1**	**81.7**	**20.3**	**20.3**
1.5.1	Design and Prototyping - WSC	82.0	0.1	81.9	82.0	16.4	16.4
1.5.2	Procurement	120.0	-	120.0	120.0	120.0	120.0
1.5.3	Assembly - WSC	20.5	-	20.5	20.5	4.1	4.1
1.5.4	Assembly test Bates	41.0	-	41.0	41.0	8.2	8.2
1.5.5	Transport	8.3	-	8.3	8.3	1.7	1.7
1.5.6	Preparation System Test	12.7	-	12.7	12.7	2.6	2.6
1.5.7	System Test	12.7	-	12.7	12.7	2.5	2.5
1.5	**Integration**	**297.2**	**-**	**297.1**	**297.2**	**155.5**	**155.5**
1.6	**Software**	**0**	**-**	**0**	**0**	**0**	**0**
1.7	**BNL overhead**	**119.0**	**33.0**	**86.0**	**119.0**	**0**	**0**
1.8	**Non-DOE contribution**	**(193.9)**	**-**	**(193.9)**	**(193.9)**		
Totals:		**1,416.4**	**140.8**	**1,206.6**	**1,347.4**	**411.3**	**479.8**

Summary of expenditures by FY:

	FY 2008	FY 2009	FY 2010
a) Funds allocated	$200.0 k	$280.0k	
b) Costs accrued	$51.6 k	$87.8k	
c) Uncosted commitments	$47.4 k	$1.5k	
d) Uncommitted funds (d=a-b-c)	$101.0 k	$190.7	
e) Remaining total contingency	$411.3	$479.8	

Summary of schedule:

	Baseline Start Date mo/year	Baseline Completion Date mo/year	Forecast Start Date mo/year	Forecast Completion mo/year	% Complete Baseline	% Complete Actual
Design						
1.1.1 Triple-GEM	5/08	3/09	8/08	3/09	100%	80%
1.2.1 FEE	9/08	4/09	9/08	4/09	100%	100%
1.3.1 DAQ	10/08	7/09	10/08	7/09	0%	0%
1.4.1.1 Gas syst	7/08	4/09	2/09	10/09	0%	0%
1.4.2.1 Air flow	7/08	4/09	7/08	6/09	0%	0%
1.4.3.1 Slow contr	7/09	10/09	7/09	10/09	0%	0%
1.5.1 WSC	10/08	5/09	10/08	8/09	0%	0%
Procurement						
1.1.2 Triple-GEM	1/09	7/09	1/09	7/09	0%	0%
1.2.2 FEE	9/08	5/09	11/08	10/09	35%	35%
1.3.2 DAQ	5/08	10/09	?/09	10/09	0%	0%
1.4.1.2 Gas syst	9/09	11/09	9/09	11/09	0%	0%
1.4.2.2 Air flow	9/09	11/09	9/09	11/09	0%	0%
1.4.3.2 Slow contr	4/10	6/10	4/10	6/10	0%	0%
1.5.2 WSC	5/09	8/09	5/09	8/09	0%	0%
Component test						
1.1.3 Triple-GEM	2/09	7/09	2/09	7/09	0%	0%
1.2.3.1 FEE chips	10/08	12/08	5/09	8/09	0%	0%
Fabrication						
1.1.5 Triple-GEM	4/09	5/09	4/09	12/09	0%	0%
Assembly						
1.1.6 Triple-GEM	5/09	8/09	5/09	6/10	0%	0%
1.2.4 FEE	5/09	8/09	5/09	12/09	0%	0%
1.3.3 DAQ	2/09	10/09	2/09	10/09	0%	0%
1.4.1.3 Gas syst	2/10	3/10	2/10	3/10	0%	0%
1.4.2.3 Air flow	2/10	3/10	2/10	3/10	0%	0%
1.4.3.3 Slow contr	8/10	9/10	8/10	9/10	0%	0%
1.5.3 WSC	8/09	12/09	8/09	8/10	0%	0%
Testing						
1.1.7 Triple-GEM	6/09	9/09	6/09	7/10	0%	0%
1.2.5 FEE	5/09	9/09	5/09	2/10	0%	0%
1.3.4 DAQ	4/09	12/09	4/09	12/09	0%	0%
1.5.4 WSC	11/09	1/10	11/09	10/10	0%	0%
1.5.7 System	7/10	8/10	7/10	2/11	0%	0%

Summary of control milestones:

WBS Number	Control Milestone Name	Baseline Date	Actual/ Forecast Date
WBS 1.1.1.1	Quarter section design complete	Q4 FY08	Q1 FY09
WBS 1.1.1.4	2D readout board design complete	Q2 FY09	Q2 FY09
WBS 1.1.1.7	Full-size GEM foils tested and meet specifications	Q1 FY09	Q2 FY09
WBS 1.1.1.9	Successful full quarter section test	Q2 FY09	Q3 FY09
WBS 1.1.2.1	All GEM foils delivered by TechEtch that meet specification	Q3 FY09	Q3 FY09
WBS 1.1.6	All detector frames assembled and tested	Q1 FY10	Q3 FY10
WBS 1.2.1	Successful testing of first prototype of front-end electronic readout board	Q3 FY09	Q3 FY09
WBS 1.2.5	All FEE readout boards assembled and tested	Q1 FY10	Q2 FY10
WBS 1.3.1.2	DAQ readout board prototype complete	Q4 FY09	Q4 FY09
WBS 1.3.2.3	DAQ crate master board design complete	Q2 FY09	Q3 FY09
WBS 1.3.4.4	Successful DAQ readout test	Q1 FY10	Q1 FY10
WBS 1. 4.2.1	STAR airflow design and prototype complete	Q3 FY09	Q3 FY09
WBS 1.4.2.4	STAR airflow system installed	Q3 FY10	Q3 FY10
WBS 1.4.3.4	Slow controls installed	Q1 FY10	Q1 FY10
WBS 1.5.1	Design of West Support Cone complete	Q3 FY09	Q4 FY09
WBS 1.5.3	Assembly of West Support Cone complete	Q1 FY10	Q1 FY11
WBS 1.5.7	System test	Q4 FY10	Q2 FY11