

Detector R&D for NSLS-II

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NSLS

Outline

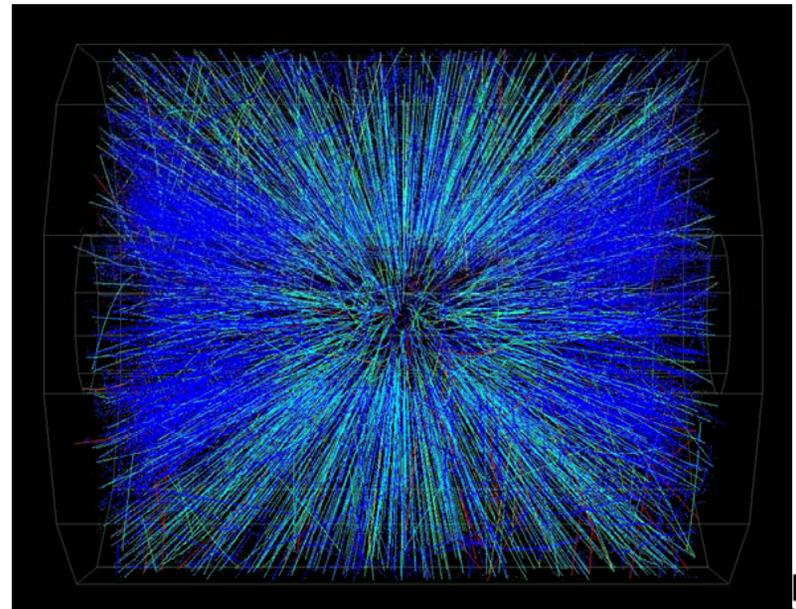
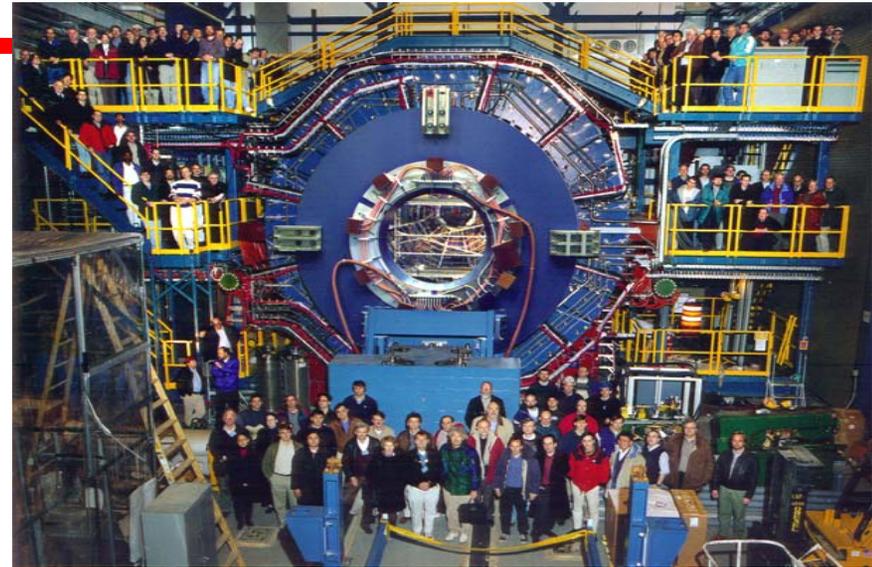
- NSLS-II detector R&D
- Cultural issues
- Silicon detectors
- NSLS Detectors
- LCLS detectors
- Emerging Technologies for Sensor/ASIC Integration
- Requirements for NSLS-II Detectors
- Proposed R&D Plan

Detector R&D for NSLS-II

- NSLS-II does not have a detector R&D program
 - Any R&D will be independently funded
 - FY08 budget will not allow any new R&D this year
 - Need to develop a new, **REVOLUTIONARY** class of detector with significant computation 'on-pixel'
 - Potentially viable technology under development (ILC R&D, IT industry)
- LCLS detectors will be useful for SR applications at millisecond timescales

Culture

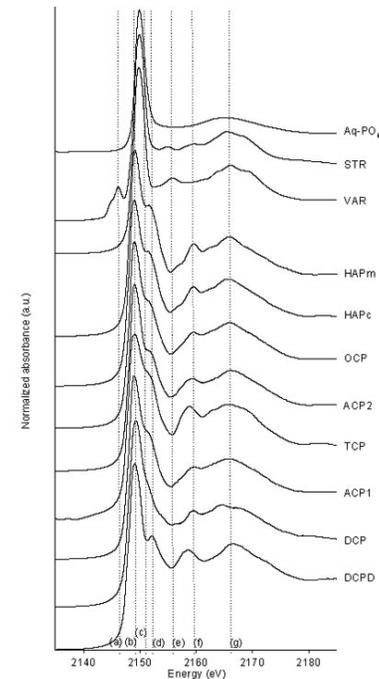
- SR and HEP are cultural opposites
 - HEP: teams of hundreds for one experiment, complex detector system
 - SR: teams of <10 usually, simple apparatus.
 - HEP: Experiment takes years
 - SR: Experiment takes hours or days
 - HEP: Detector IS experiment
 - Scientists closely involved in design
 - SR: SAMPLE is experiment: SR and detector a necessary evil
 - Scientists just want the result



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Sato, Solomon, Hyland, Keterings, Lehmann, Cornell Univ. 2006

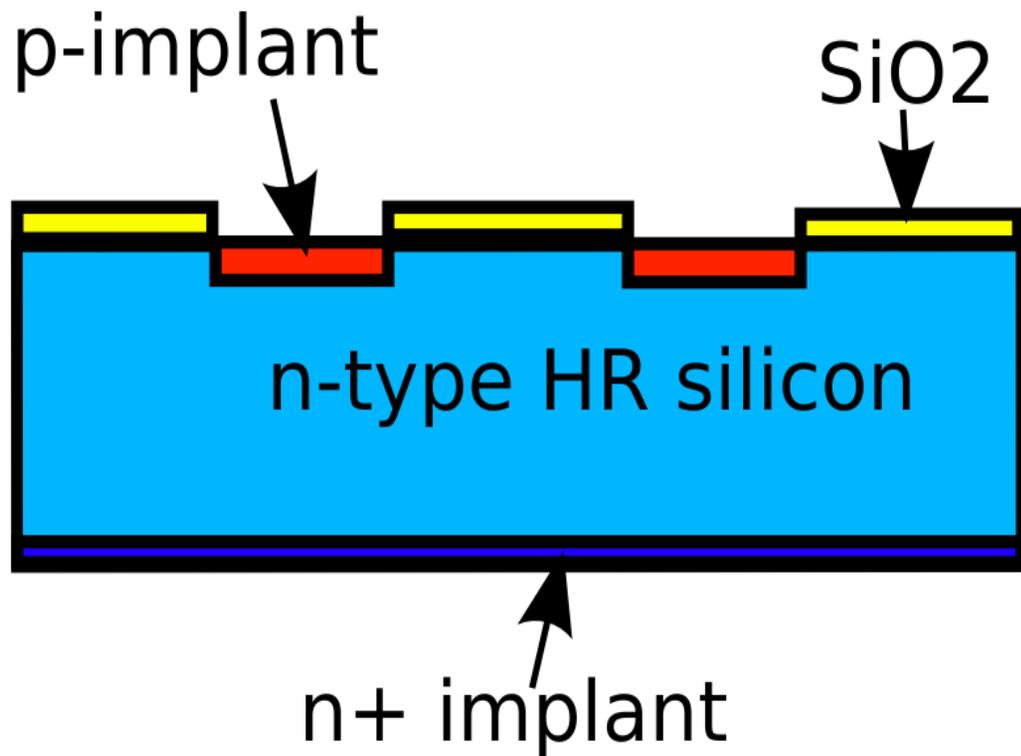


What is the ideal diffraction detector?

- Specifications:
 - 1 micron pixels
 - 1000 megapixels
 - 1ns time resolution
 - 100% efficient at all energies
 - Free
- Various physical and fiscal realities conspire to prevent this being realized.
- Photon-counting provides best S/N.
 - BNL R&D focused on photon-counting
 - LCLS detector necessarily integrating.

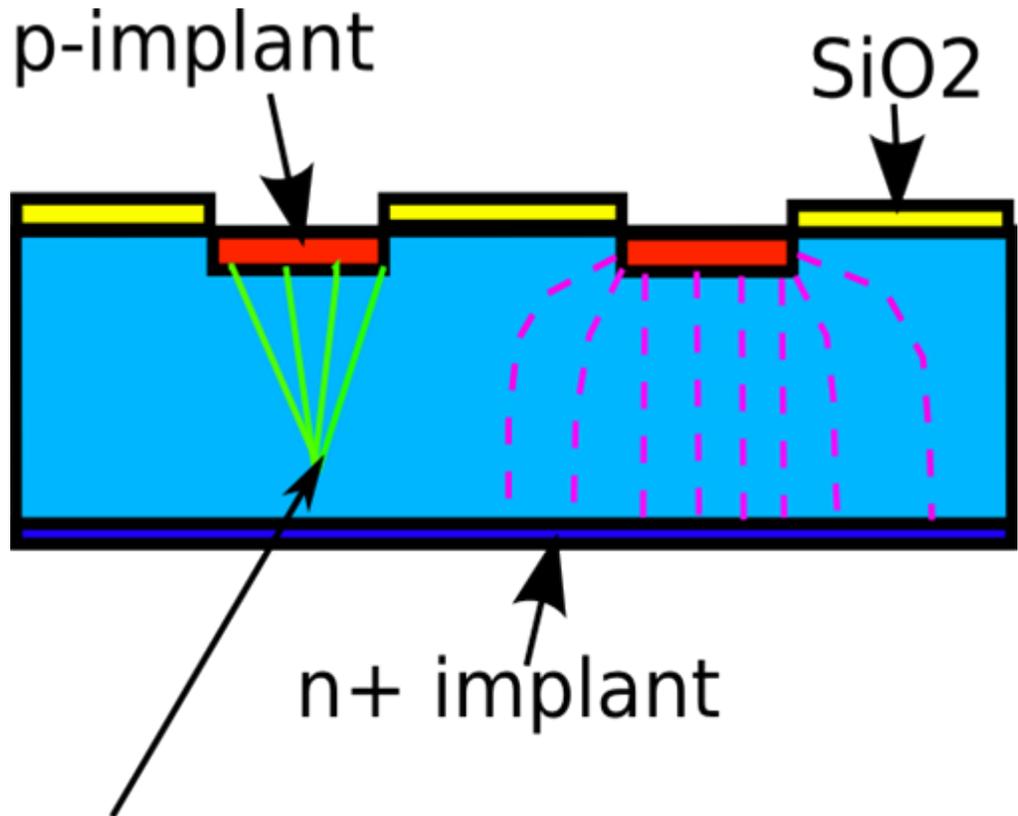
Simplest silicon detector

- vertical P-N Junction
- Wafer bulk is active (unlike commercial CMOS)
- Wafer must be very high resistivity ($>5\text{k}\Omega\text{-cm}$) to allow full depletion at reasonable bias voltage
- SiO_2 provides electrical isolation between adjacent diodes



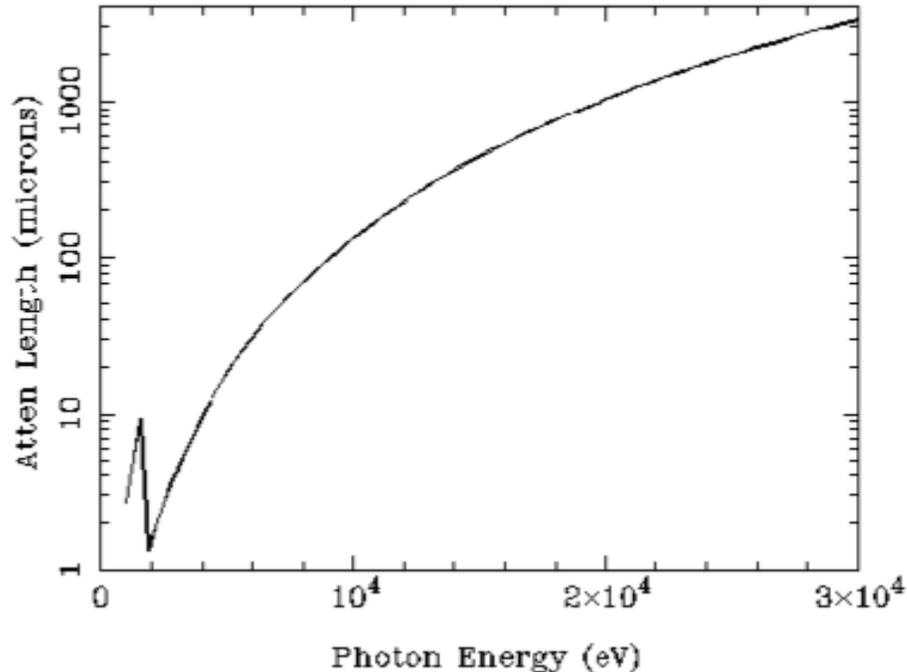
Internal fields and trajectories

- Photon produces e-h pairs.
- charges drift towards surfaces due to bias field (wafer fully depleted). Takes about 20ns for 0.4mm wafer.
- Transverse momentum of charges causes charge spreading
- For 10keV photon, spreading is 20-30um for 0.4mm wafer.
- **SMALL PIXELS WILL PERFORM POORLY** as photon-counting detectors.

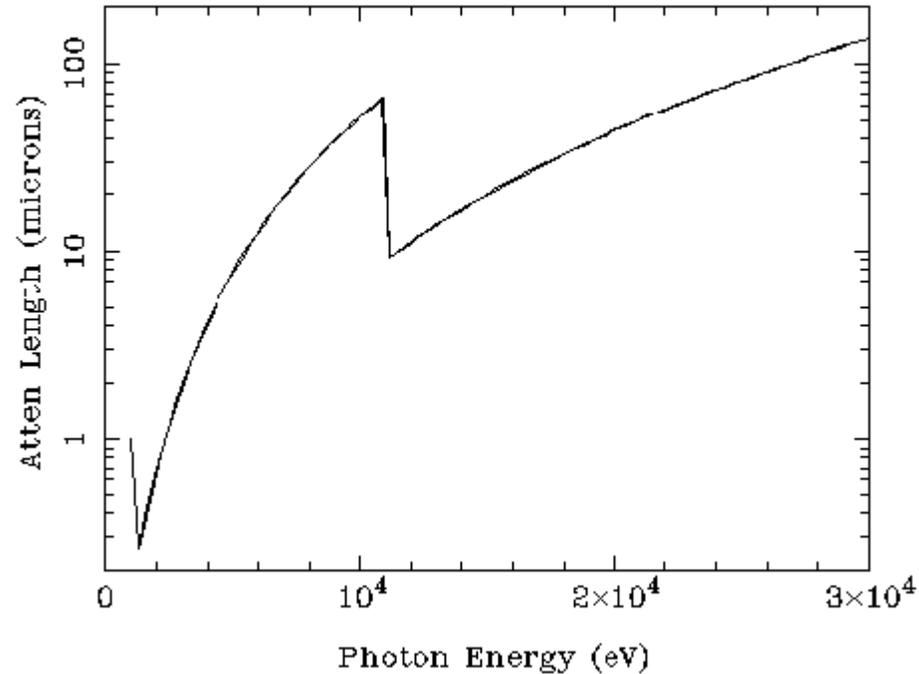


Absorption length for Si & Ge

Si Density=2.33, Angle=90.deg



Ge Density=5.323, Angle=90.deg



- Materials science needs $E > 20\text{keV}$ to penetrate dense materials (alloys, ceramics etc.)
- Biology needs higher E to reduce radiation damage
- Ge is better, but needs to be cryocooled

Ge planar technology

- The simple and efficient planar silicon detector technology does not exist for germanium
- SiO₂ does not provide a good trap-free surface passivation for Ge
- GeO₂ is not stable
- We have LDRD funding to develop such a process
 - Started Nov. 07, for 2 years
 - Will use High-k dielectrics (developed recently for high-speed Ge-based logic) for surface passivation
 - Need to find an N-type ion which is activated at low temperature to allow PN and PIN junction formation.

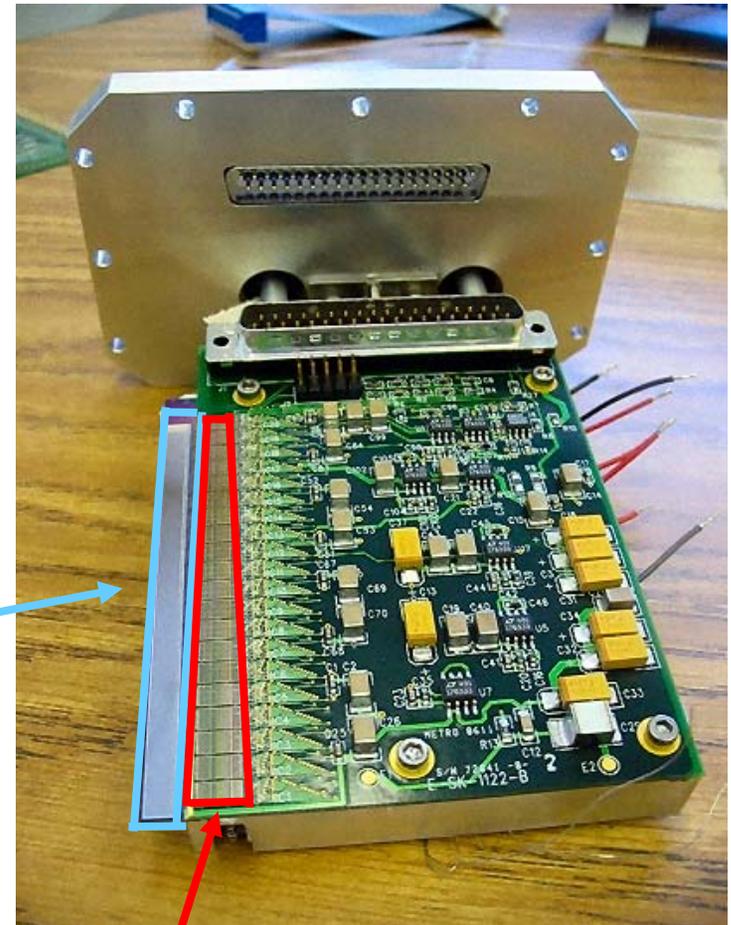
NSLS Detectors

- A series of detectors for selected SR applications has been developed over the past ~5 years
- Key technologies:
 - Silicon pad and strip detectors (Inst. Div.)
 - CMOS ASICs (Inst. Div.)
 - System design, packaging, fixturing, DAQ (NSLS)
- Significant performance advantages due to the ability to utilize highly parallel architectures

Detector for Diffraction Applications

- 80mm long silicon PSD
- 640 channels, ASIC readout
- 125 μ m pitch
- 4mm wide
- 0.4mm thick
- 350eV energy resolution @ 5.9keV

sensor



20 ASICs

Application Examples

Real-time growth / surface modification

- *Beamline X21 in-situ growth endstation*
- *Several high-impact pubs*

Reflectivity / truncation rods / GISAXS

- *Tests at Cornell and APS (COBRA studies)*
- *System delivered for X9 undulator/CFN*

Powder diffraction

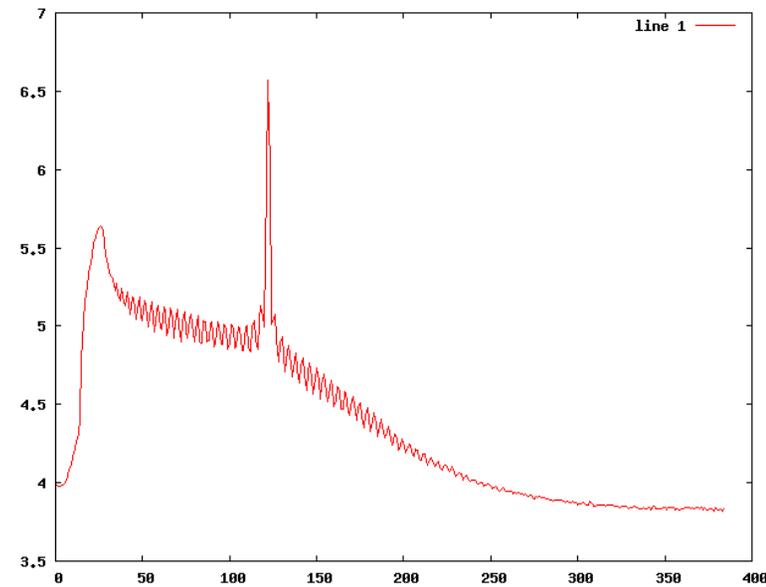
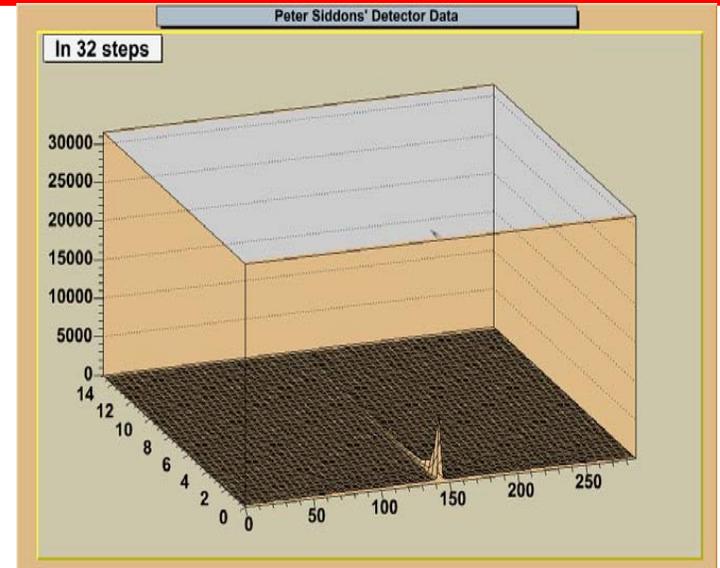
- *Detectors in use at X16C, X14A*

Inelastic scattering

- *System delivered to Argonne*
- *x10 intensity, x2 resolution on MERIX*
- *Collaboration with Taiwan NSRRC*

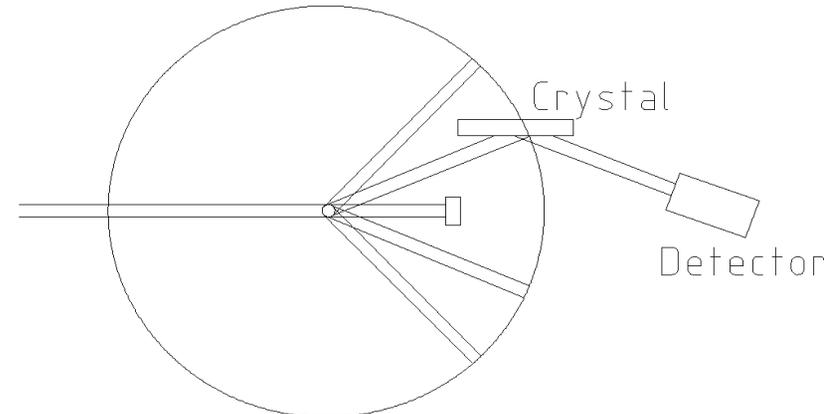
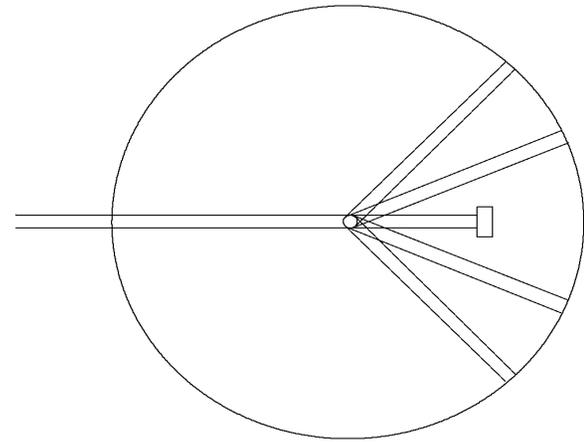
Lots of interest

- *Cornell*
- *Other APS*
- *SSRL*

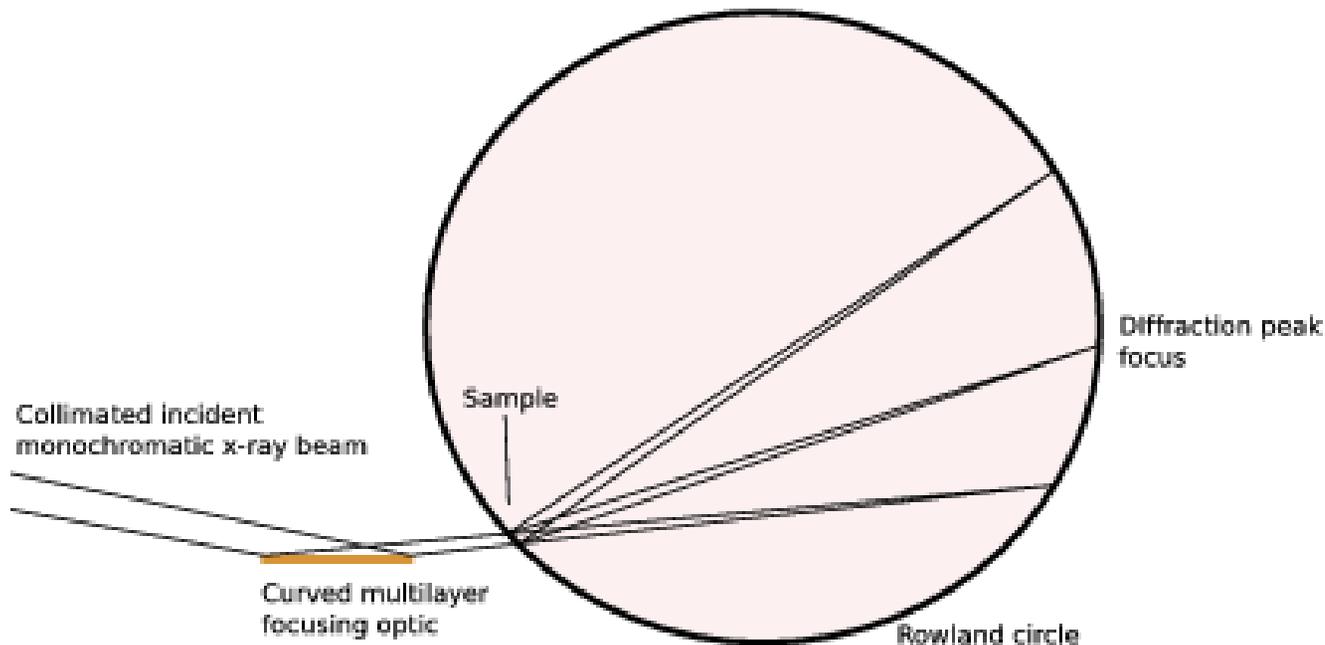


Powder diffractometers

- Two common designs
 - Debye-Scherrer
 - Position-sensitive detector -> high throughput
 - Modest resolution
 - Crystal analyzer
 - Highest resolution
 - Low systematic errors
 - Slow!

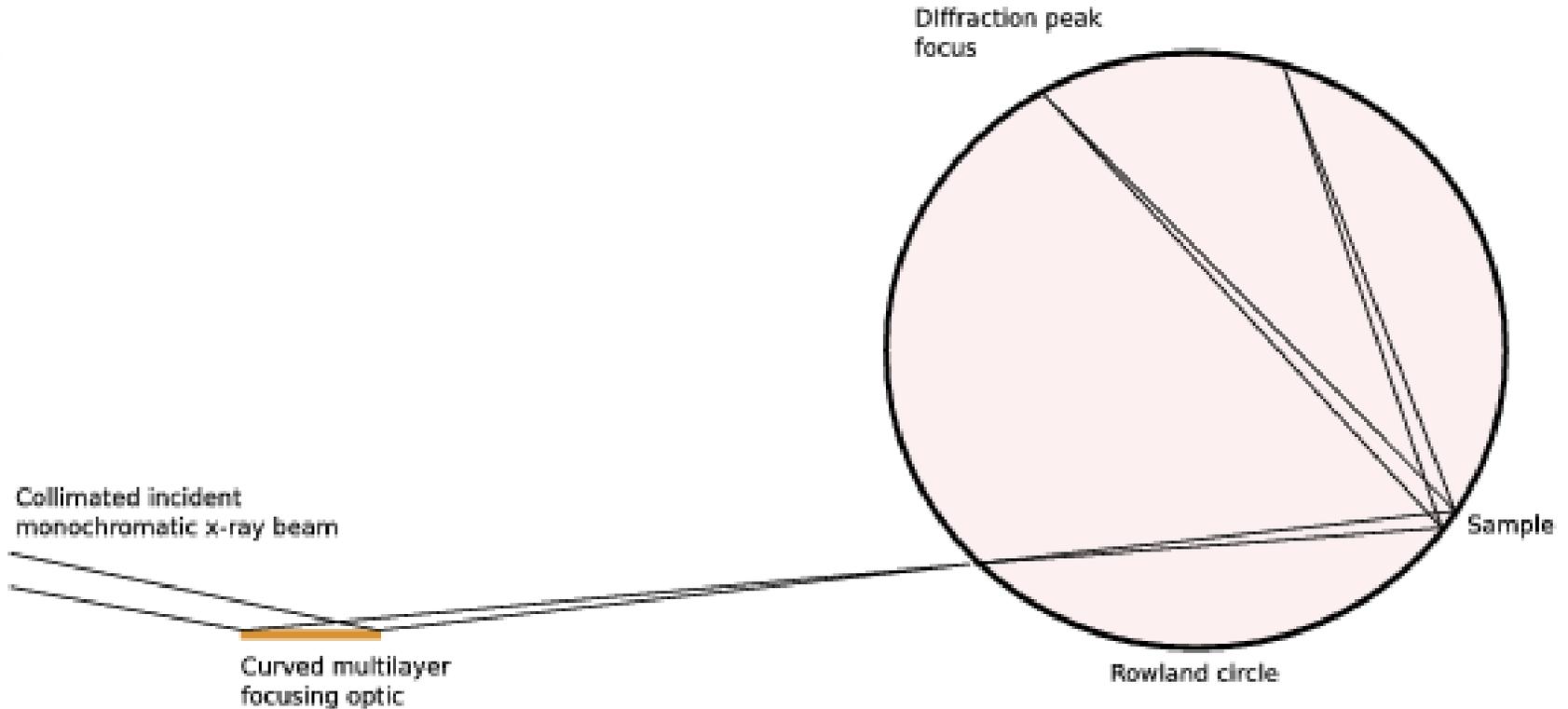


Guinier geometry



- Uses focusing to give line profile independent of sample or beam size
- Large sample size improves particle statistics
- Rowland circle construct
- Usual designs ~10cm diameter

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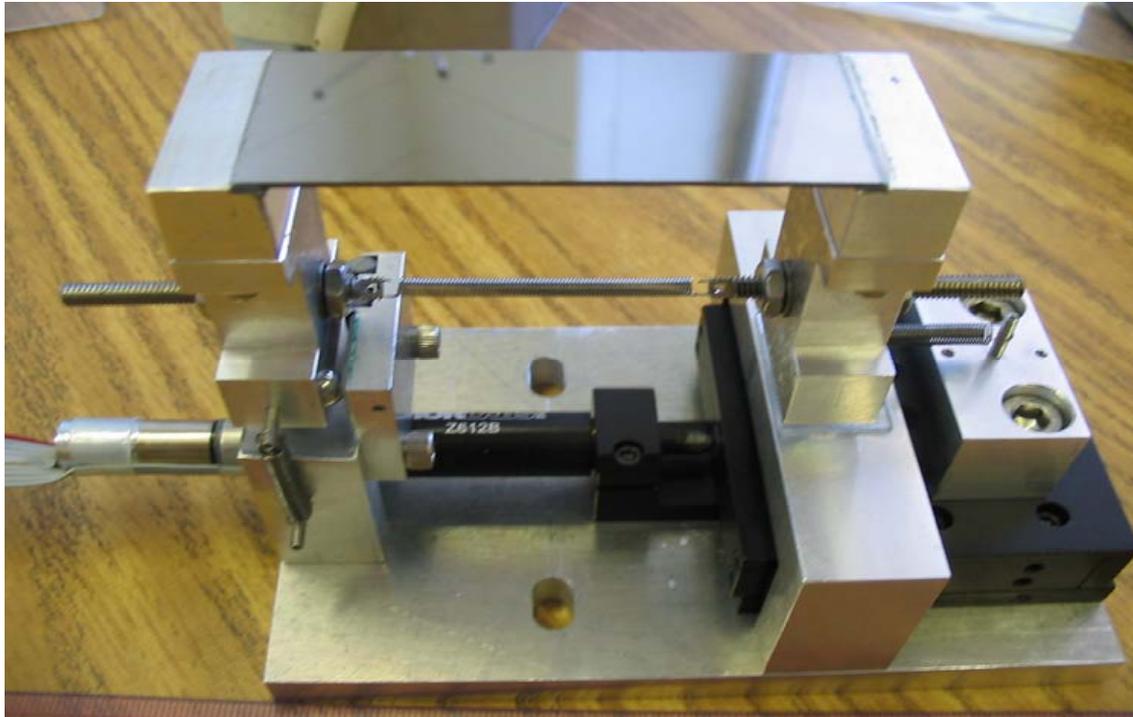
Synchrotron version

- Large Rowland circle diameter (we use 1 meter)
 - Greater depth of focus minimizes aberrations
 - Better angular resolution for same spatial resolution
- Need 'strong' focusing optic to turn parallel beam into strongly converging beam
 - Curved multilayer
 - Compact (large incidence angle)
 - Efficient (>80% for good optic)
- Need electronic detector with ~90 degrees coverage, good efficiency, low noise, good spatial resolution and fast readout
 - Silicon microstrip photon-counting detector
 - Low noise (~350eV resolution)
 - Fast readout (1ms, highly parallel FPGA-based readout)
 - Custom made, ~10,000 channels.

Proof of principle experiment

- Use existing bendable multilayer for focusing
- Use existing 384-channel microstrip detector
- Mount it on goniometer 2-theta
- Step-scan it to cover desired range
- Not ultimate speed but still significantly faster than scanning crystal analyzer.

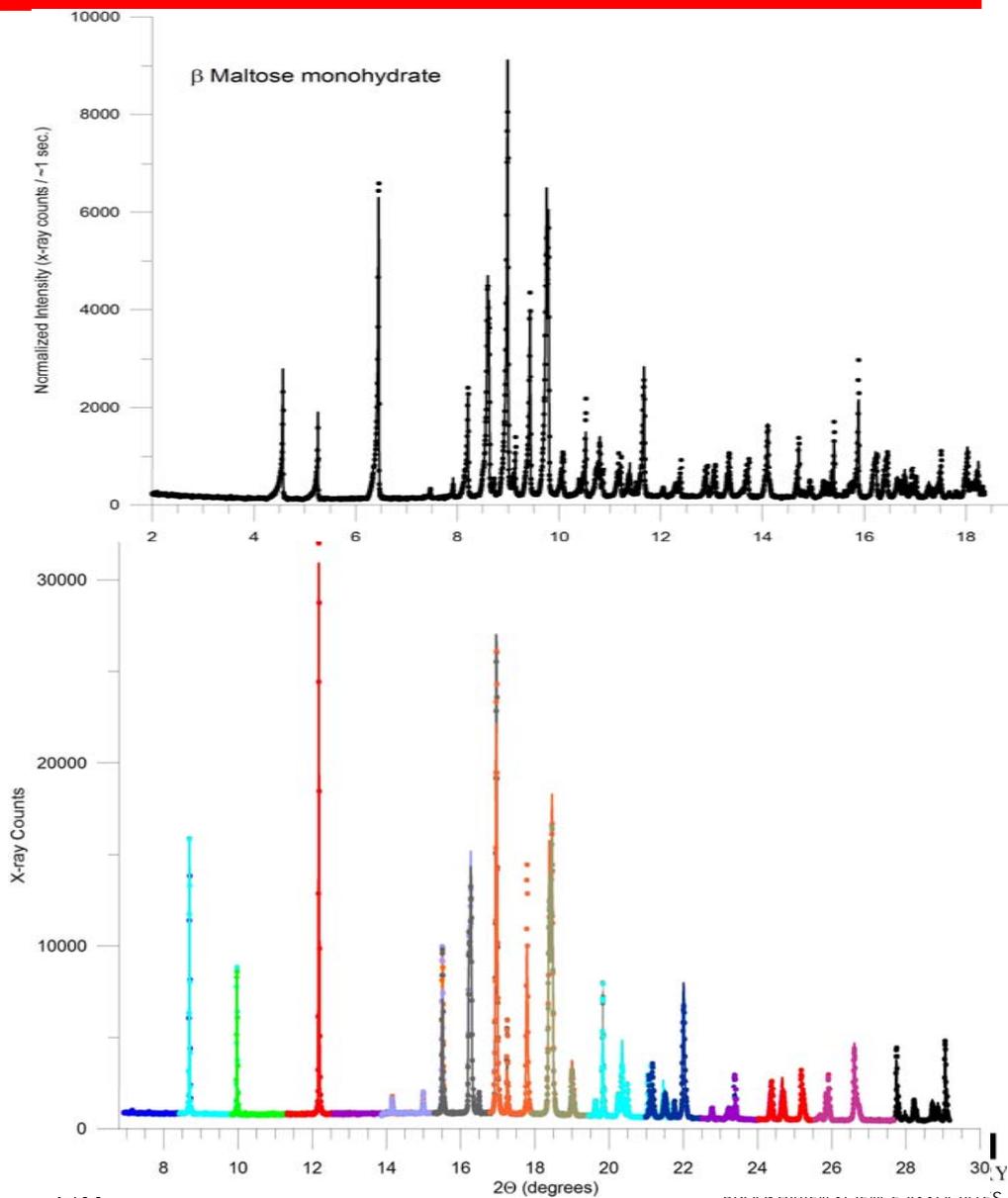
Bendable multilayer mirror



- Thin silicon substrate
- W/Si coating, 100 pairs
- ~1mrad reflection width
- Can produce convergent beam of 2mrad
- U-bender, spring-loaded.

Test data: Maltose

- Data on same material collected at X16C using flat crystal setup and at X12A using Guinier camera
- 1 sec /point for crystal instrument, 3274 points
- 50 sec /point for Guinier instrument (get 5 x counts)
- So full detector of this design would have 300 x speed advantage
- Simple improvements could provide higher intensity for Guinier instrument, easily x3, pushing advantage to 1000 x.



Large strip detector

- Current NSLS project
- Curved aluminum frame
- 120 degree coverage
- 13 modules
 - 80mm per module
 - 640 strips/module
 - 8320 total
 - 0.014 deg/strip
 - 1ms readout time

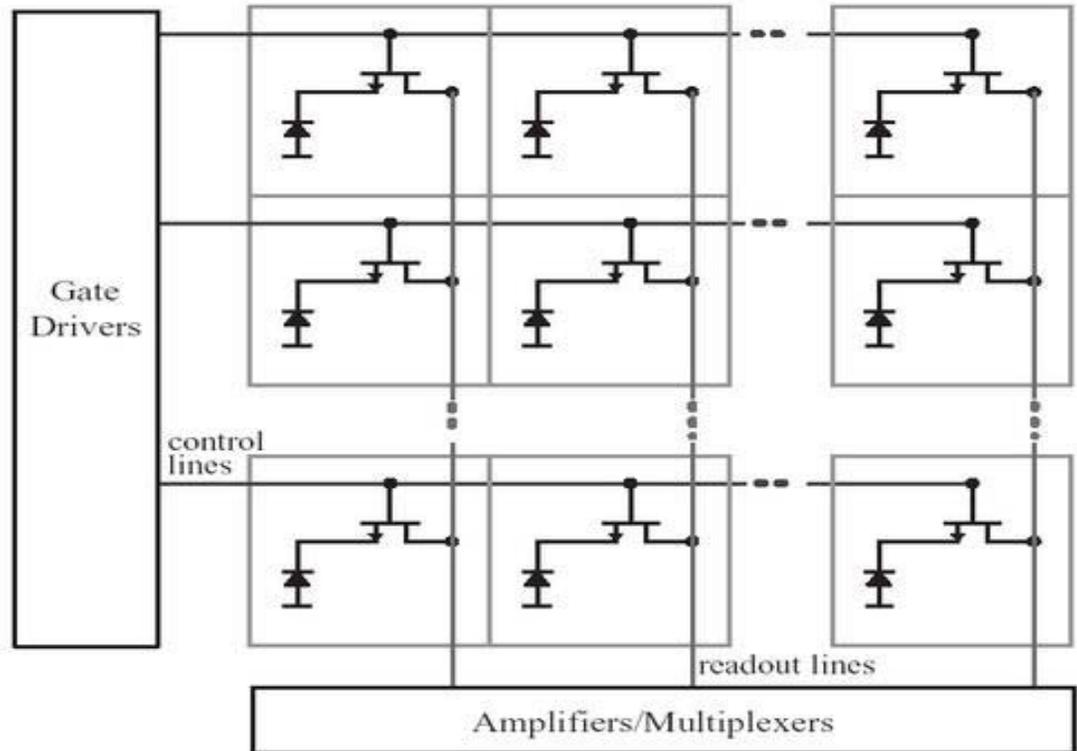


LCLS detectors

- LCLS is a Free-Electron Laser x-ray source being built at SLAC (Stanford). It will produce $<100\text{fs}$ long x-ray pulses at 120Hz .
- BNL is contracted to supply fast readout Imaging detectors
- They must:
 - Be integrating detectors because of LCLS time structure
 - Have large dynamic range for single-shot experiments
 - Have low noise
 - Have $< 8\text{ms}$ readout time
- These detectors will also be valuable at a storage ring
- They will be useful for time-resolved diffraction at millisecond timescales

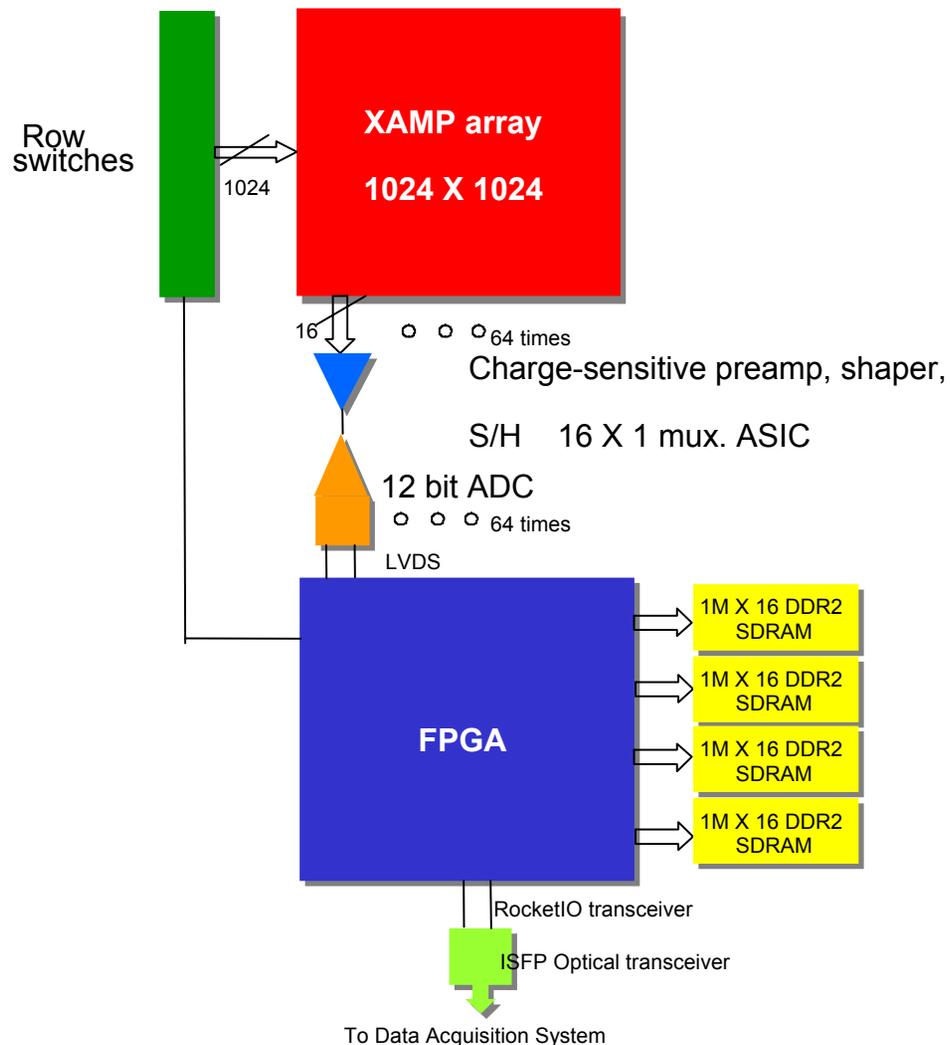
Active matrix readout

- Charge stored in diode capacitance (switches off)
- Readout amplifier on each column
- Each ADC reads 16 columns (multiplexed)
- Switches turned on sequentially row-by-row
- Charge read out and digitized
- 1 μ s per row => 1ms for 1000 rows.
 - 8-channel 40MHz/channel ADC chip
 - 8 chips, each ADC multiplexed among 16 columns
- 2Gb/s data rate



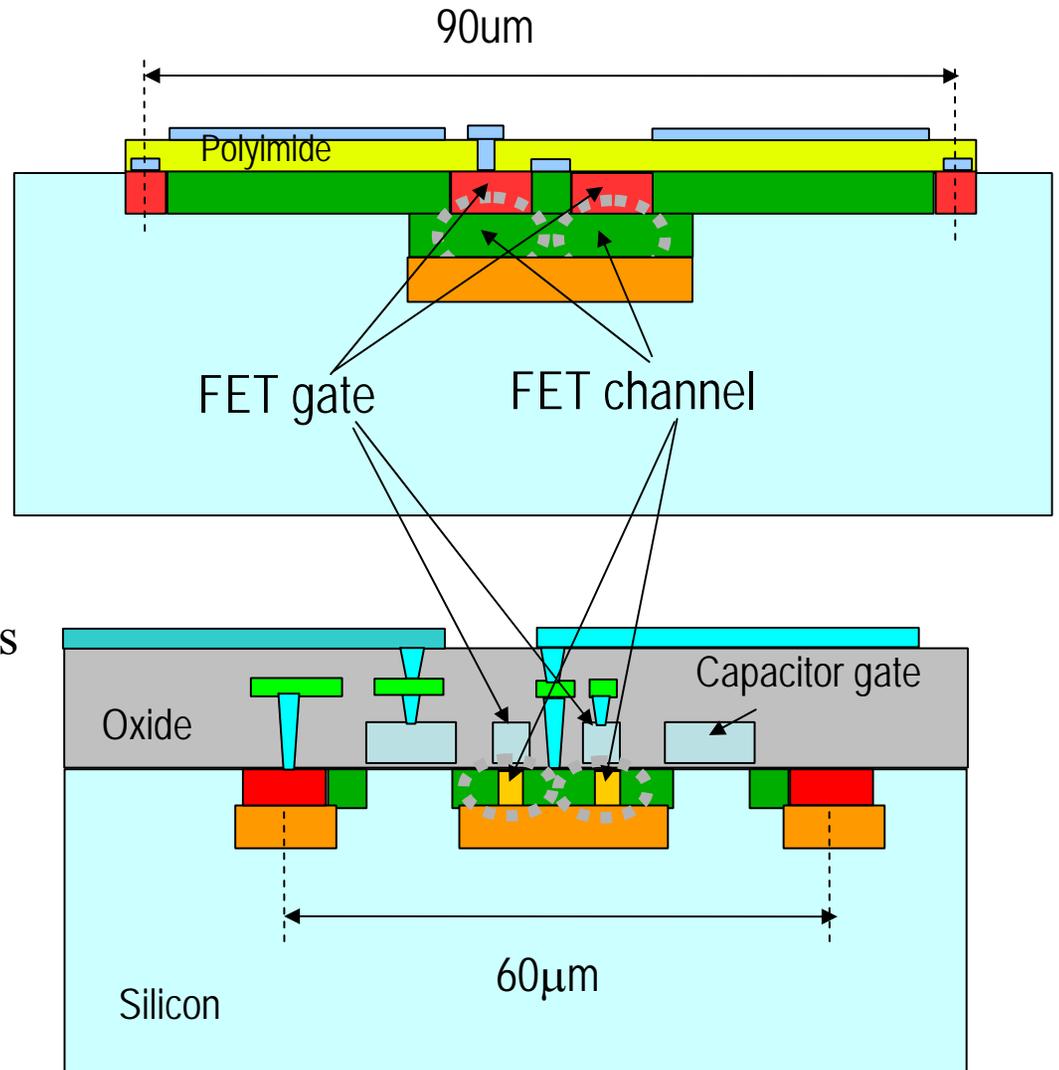
Readout system

- Row-by-row readout, 1 μ s/row
- 8 Fast (>20MHz) 8-channel ADC's multiplexed e.g. x16 columns = 1024
- 2GB/s instantaneous raw data from ADCs
- 250MB/s averaged, i.e. to be stored, based on 120Hz cycle. More if rep. rate is upgraded.
- Data streamed through FPGA to fast memory and terabyte disk store.
 - FPGA does background correction



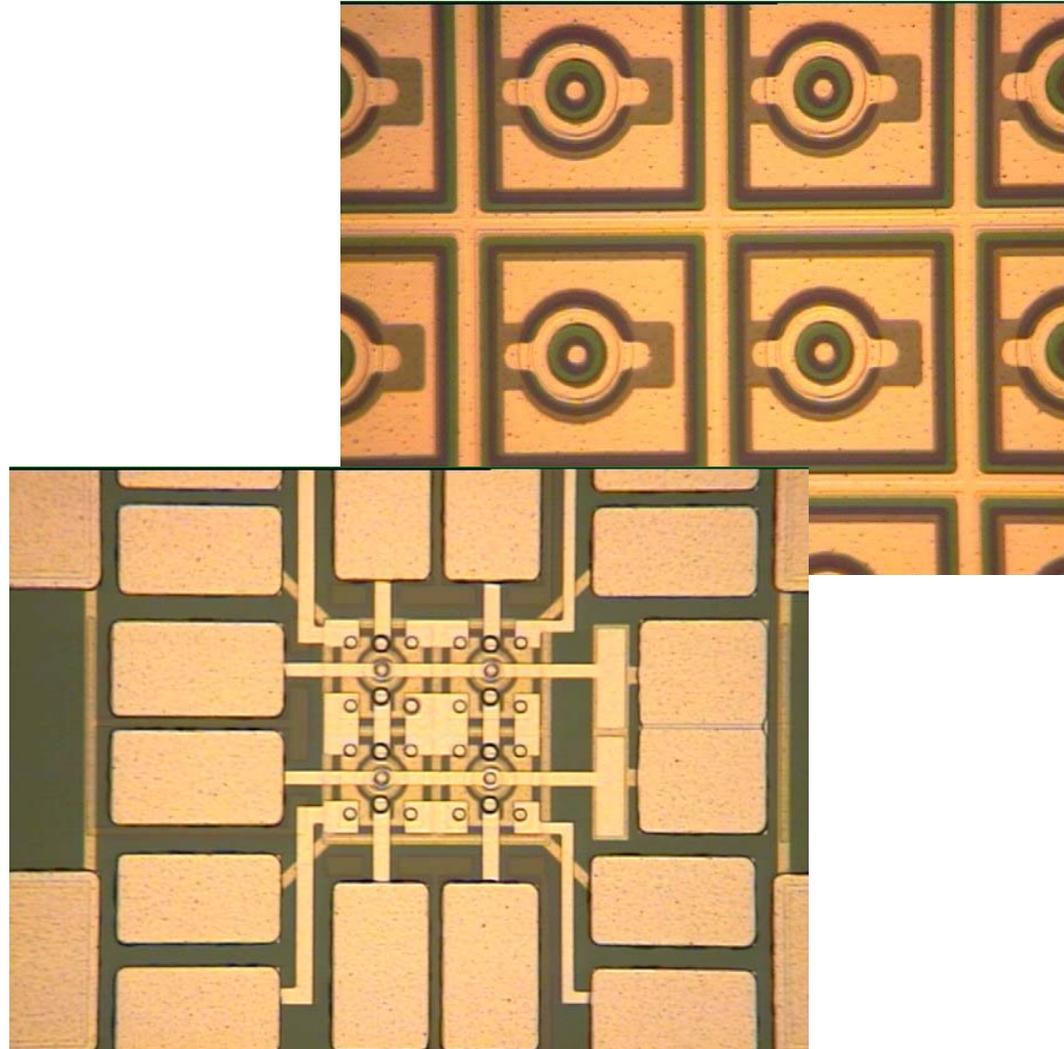
JFET vs MOSFET structure comparison

- Both start with high-res. wafer..
- Both make implants on both sides of the wafer
- BNL's process needs careful alignment between layers
- IBM's process is self-aligning for several key layers
- If successful, IBM's process allows more complex circuits to be designed than BNL's
- We have first devices from both processes in hand.



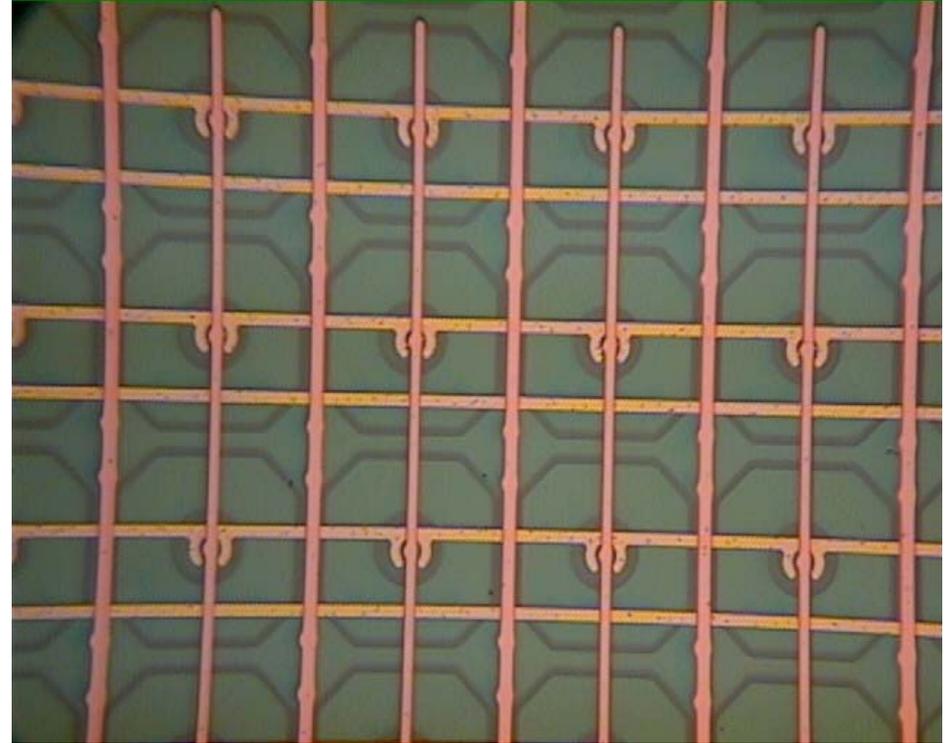
Images of BNL matrix structures

- Upper picture shows gate ring metal and charge collection capacitor plate
- Lower picture shows complete 2 x 2 array, showing two metal layers separated by a polyimide insulation layer.

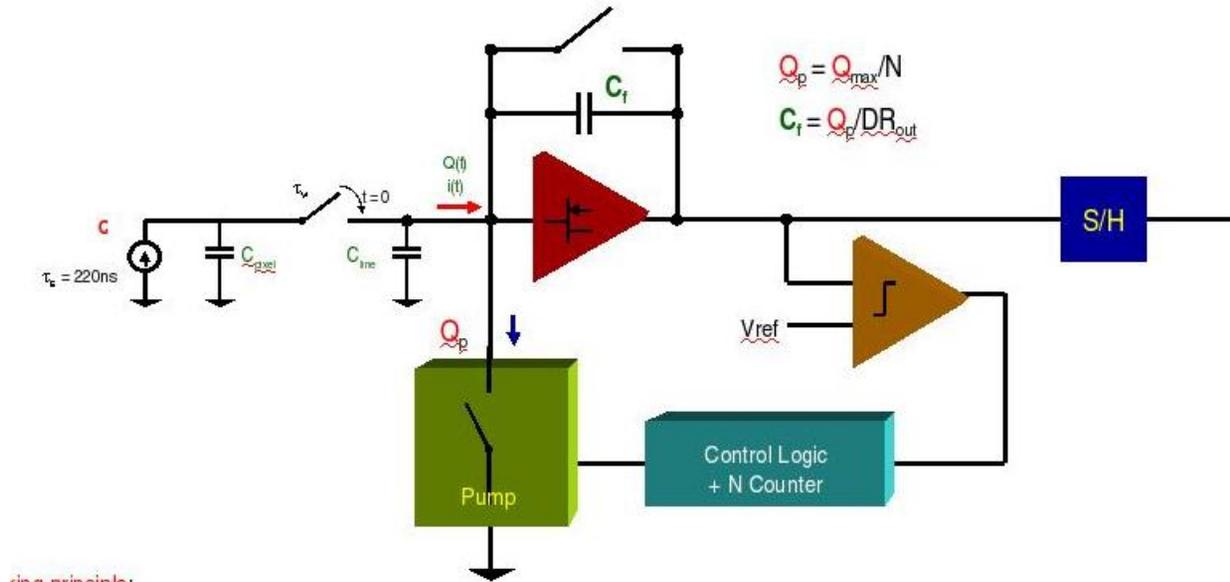


IBM collaboration

- MOS version of XAMPS
- Fabricated to our design by IBM Yorktown Heights
- Potentially lower noise
- Potentially mass-produceable



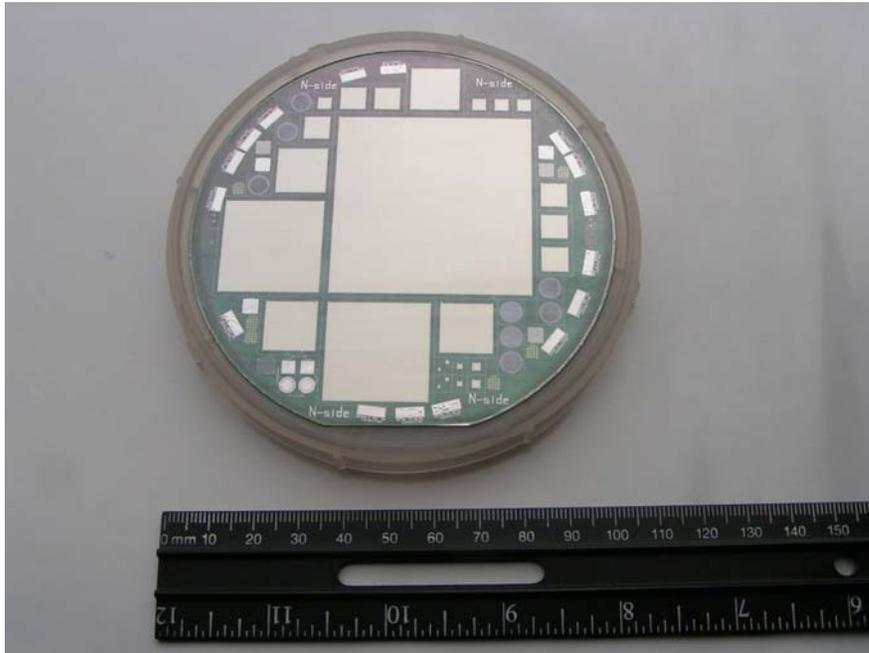
Readout ASIC



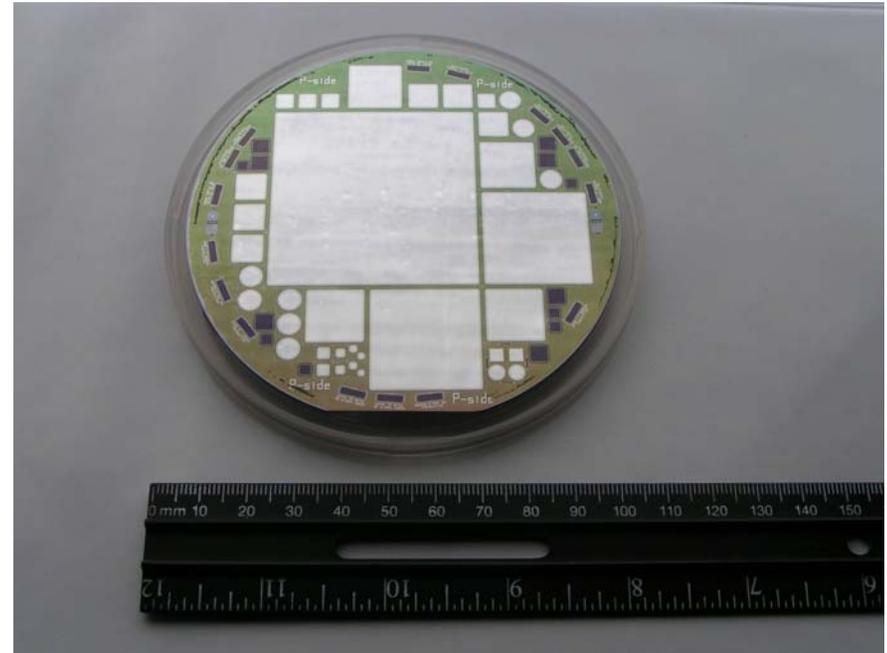
ring principle

- Problem is to handle both large signals and small signals while maintaining low noise for small signals
- Circuit works by 'pumping' large charge packets out of integrator summing node until amplifier falls into linear operation, then digitizing remainder.

BNL's device Wafer



Device side

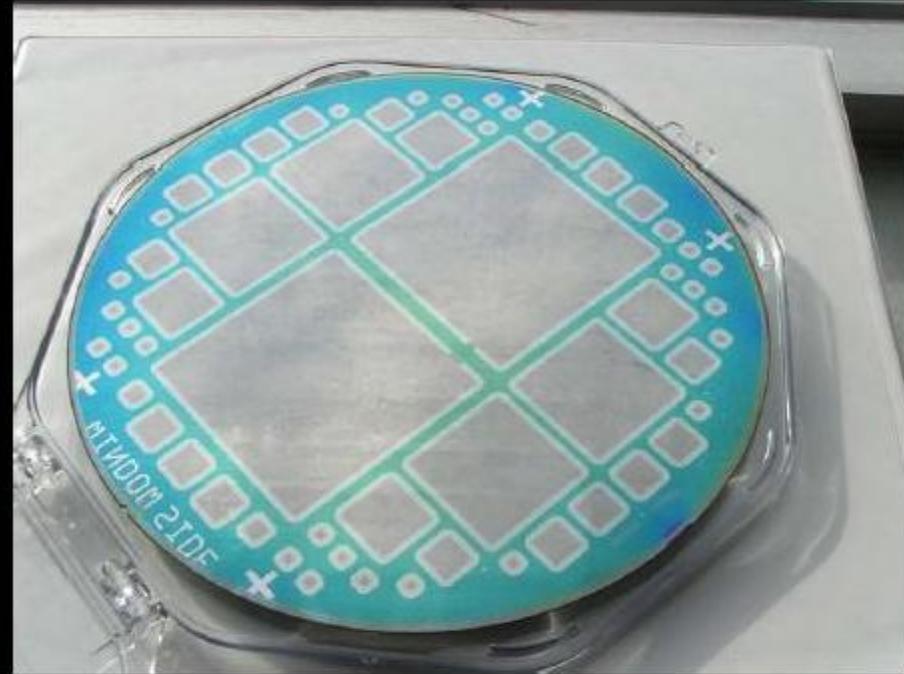
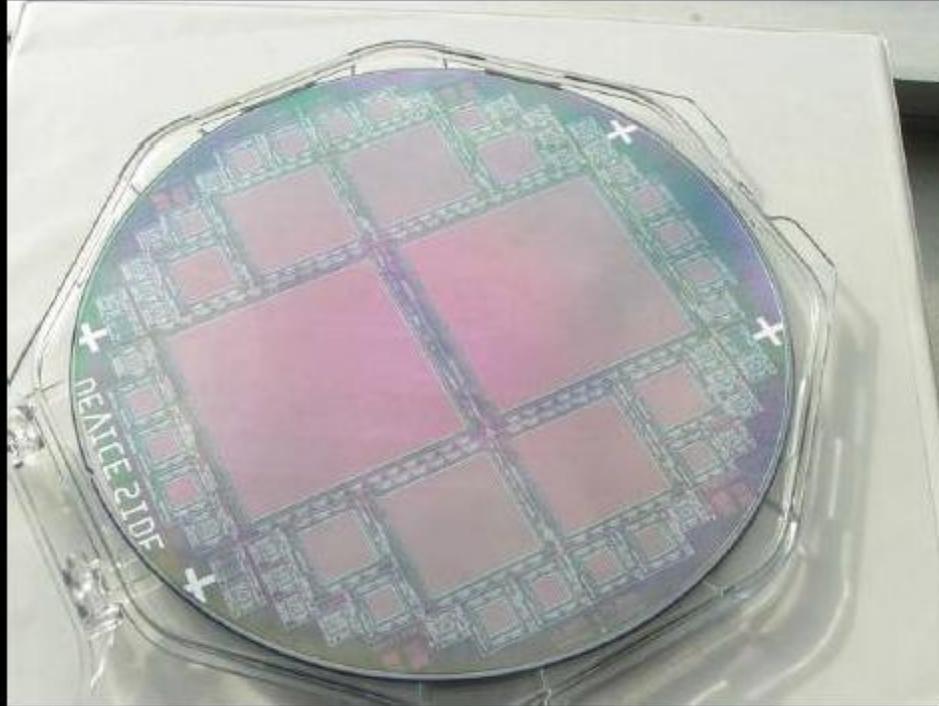


Window side

- 4" wafer carries a range of pixel numbers from 512 x 512 down. Next run will be on 6" wafers, and carry 1k x 1k devices.

IBM's device wafer

Actual Device and Window Sides



- 8" diameter wafer carries a range of pixel numbers from 1k x 1k down, with various design optimizations. Tests will determine best design.

Applications

- This device will be $>70\%$ efficient up to about 15keV
- It will offer millisecond readout
- We will develop a tiled version to provide greater pixel count.

The future

- Need to find a technology to put more functionality in each pixel
- Requirements for fabricating circuits are different from those for fabricating sensors
- How can we integrate these divergent requirements?

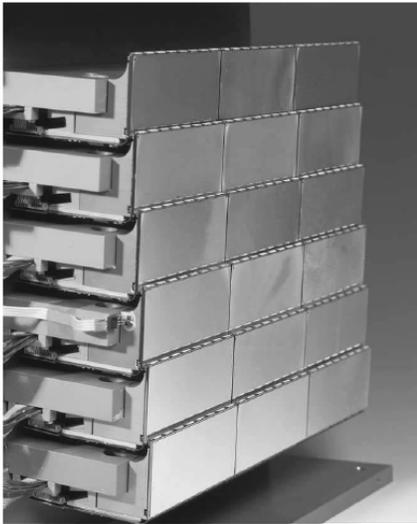
Possible Monolithic Approaches for Sensor/ASIC Integration

- Problem: sensor and readout optimize differently
- Solutions:
- Existing Technology
 - sensor in CMOS process (MAPS)
 - transistor in sensor process (DEPFET, XAMPS)
- Charge-Shifting
 - capture charge in a potential well and physically move it to output port (CCD, CDD)
- Physical Connection
 - bump bonding (PbSn, In)
 - direct wafer-wafer bonding

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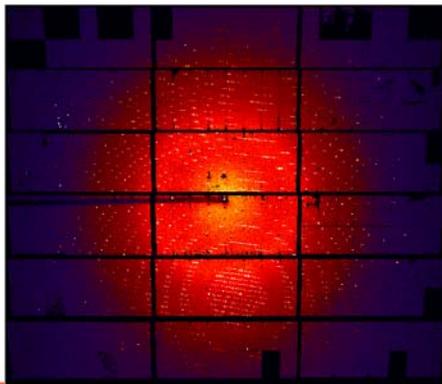
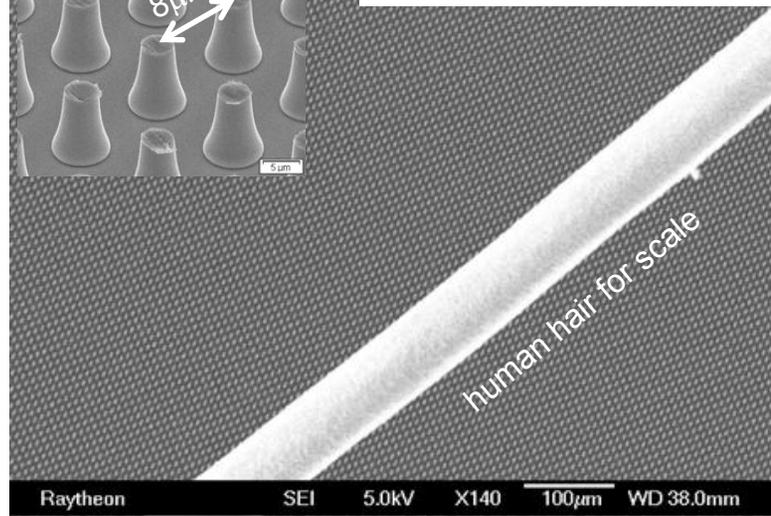
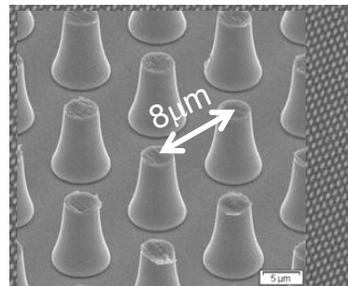
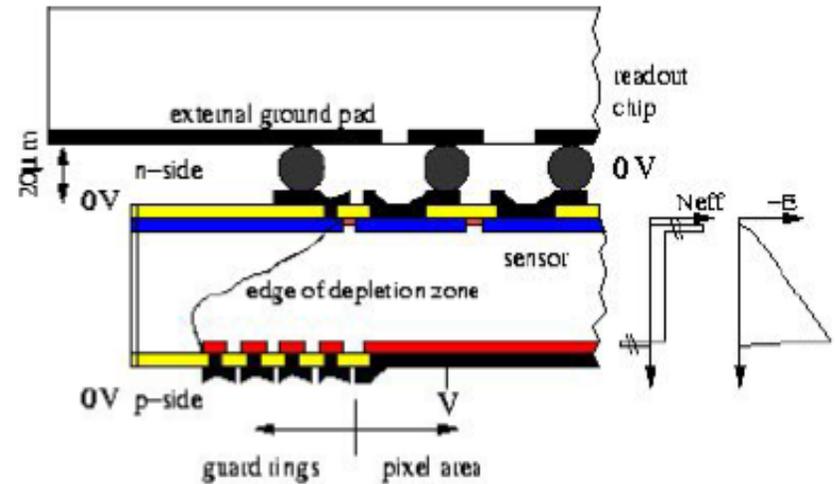
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Bump-bonding: Examples

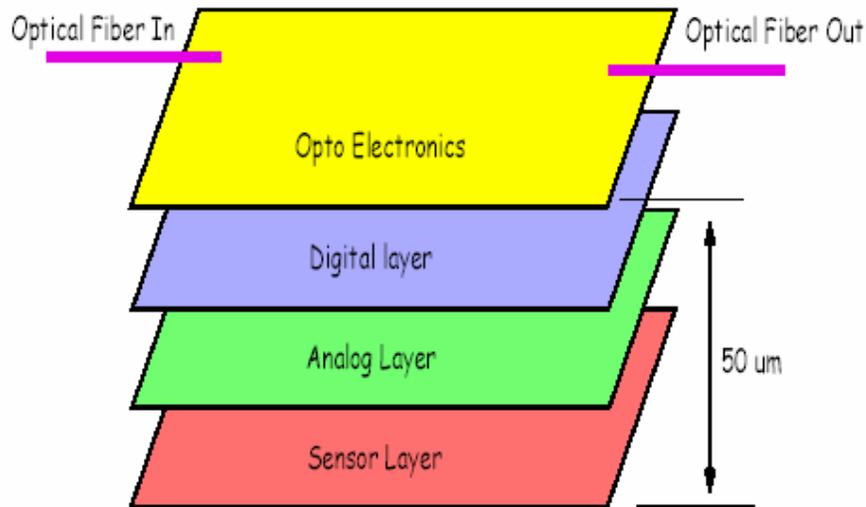


PILATUS 1M

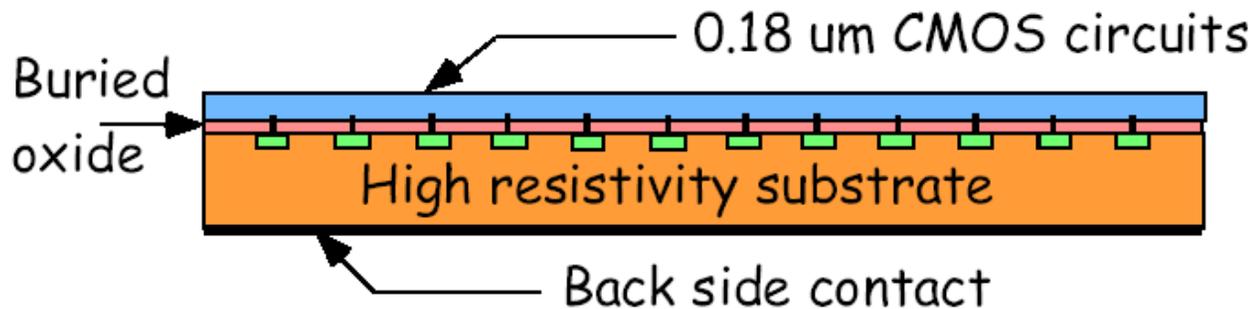
Swiss Light Source



direct wafer-wafer bonding



- Ultimate goal is monolithic integration of any technology
- Immediate push in industry is for reducing wireload distribution in digital ICs
- Science applications being pursued in optical/IR imaging, HEP tracking
- FNAL and KEK have active HEP designs
- Processes available at Lincoln Labs, JPL, OKI Semiconductor, IBM (?)



A Monolithic Photon-counting pixel detector

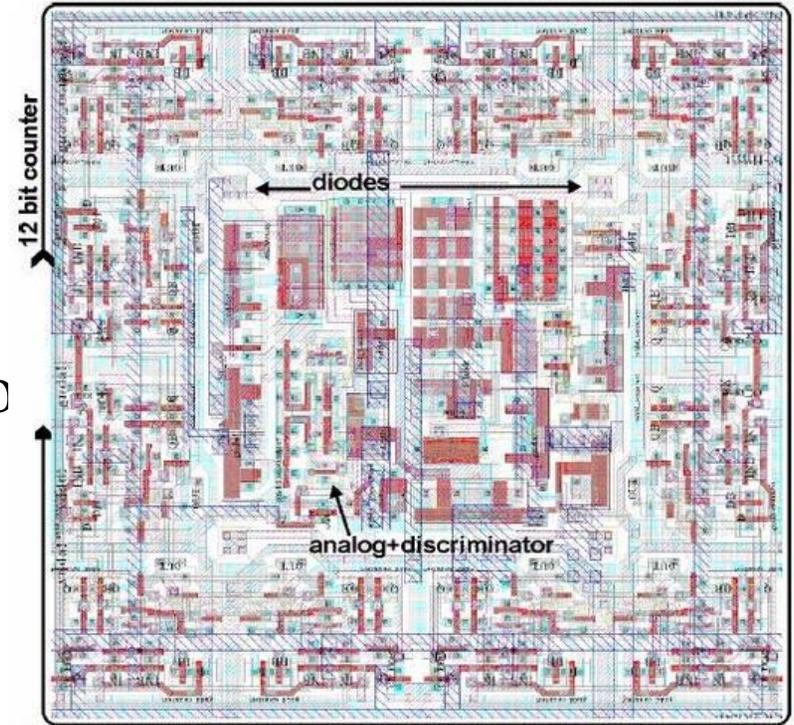
26 x 26 um (G. Deptuch, 2006)

- 280 transistors
- Built using standard SOI CMOS
- Impossible to properly prepare 'detector'.

Bonding CMOS and sensor after sensor implant gives full control over interfaces

60 x 60 um pixel would allow ~1500 transistors

- Better analog circuits
- More bits
- Double-buffering (no dead-time for readout?)



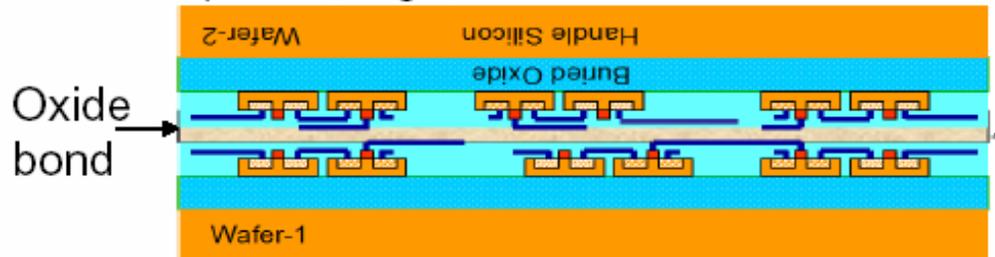
Process flow for 3D Chip

- 3 tier chip (tier 1 may be CMOS)
 - 0.18 um (all layers)
 - SOI simplifies via formation
- Single vendor processing

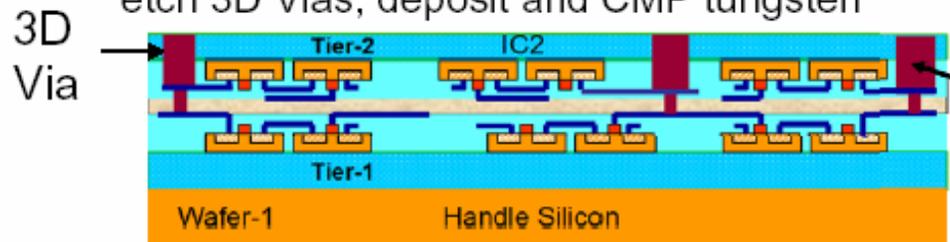
1) Fabricate individual tiers



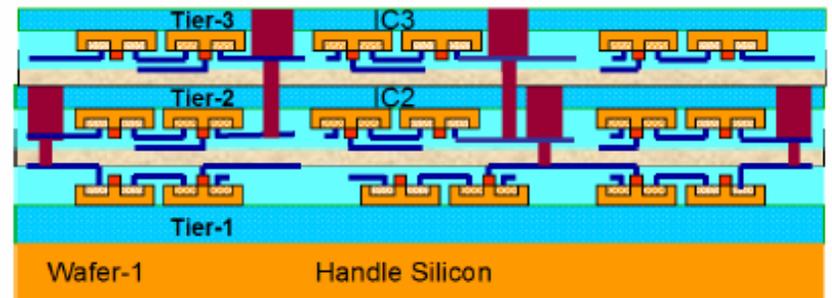
2) Invert, align, and bond wafer 2 to wafer 1



3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



Goals for NSLS-II Detector Development

A 'monolithic' photon-counting pixel detector

- 3D version of Pilatus
 - Smaller pixels
 - Better yield

A pixelated detector with spectrum-per-pixel

- Simultaneous spectroscopy/diffraction detector
- energy and spatial resolution
- Laue diffraction
- x-ray microprobes with microdiffraction and fluorescence analysis on the same sample position with the same detector

A pixel detector with multiple-tau time autocorrelation electronics on each pixel

- megapixel detector with on-pixel correlators can provide sufficient sampling density to access the sub-microsecond domain
- 3D technology will provide the necessary integration density

Acknowledgements

- NSLS detector group: Tony Kuczewski, Rich Michta, Kate Feng, Gabriella Carini, Angelo Dragone
- NSLS User Science Division techs: Dennis Poshka, Tony Lenhard, Shu Cheung
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