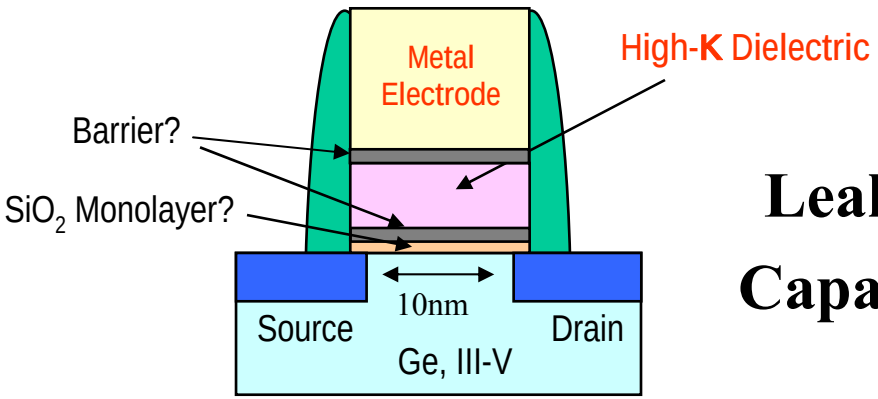
Interfaces in nanoelectronics

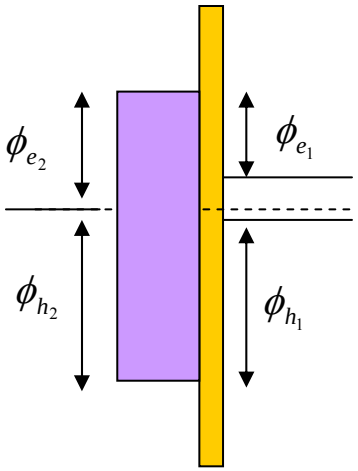


CMOS gate >2012?

Leakage too high!

Capacitance scaling

$$C \propto A\varepsilon_\kappa/d$$



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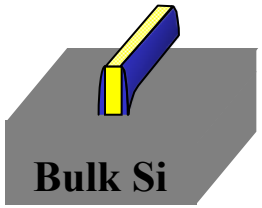
Funding: NSF, SRC

CMOS gate stack activities

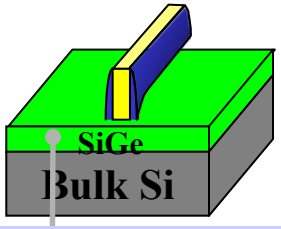
- Ion scattering - MEIS, RBS
- Electronic structure – XPS, UPS, Inverse PES, Internal PES
- Substrates: Si, SiGe, Ge, GaAs, InGaAs
- Etching chemistry and roughness
- Film stoichiometry and thickness for multilayer structures
- Microscopy - TEM, SEM, AFM….
- Electrical – CV, IV
- Film initiation and growth (esp. for ALD growth)
- Influence of interface layers (diffusion barrier, growth initiator, work function engineering)
- Metal gate/high-κ dielectric film and interface stability
- Diffusion/atomic mobility (O, Si, N, metal, etc…)
- Epitaxial oxides and higher-K - e.g. STO/Si, La compounds

Lysaght - Sematech

High-k / Metal Gate

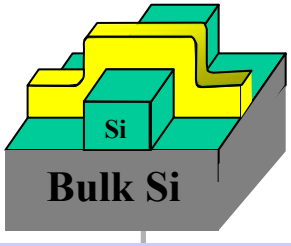


Hi Mobility Channel



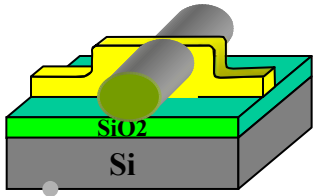
Characterization Issues:
- SiGe-HK Interface
- Damage at p-n in SiGe
- Strain in channel

FinFET

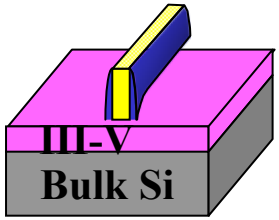


Characterization Issues:
- Sidewall S/D doping
- Sidewall silicidation
- Sidewall etch

Nanowires



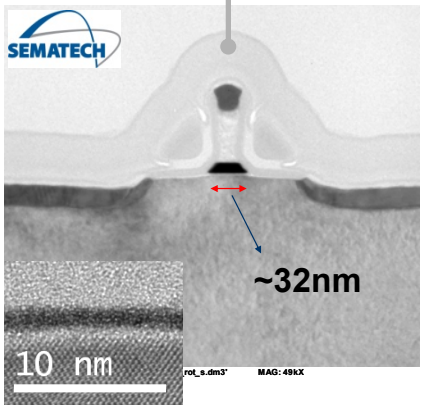
III-V

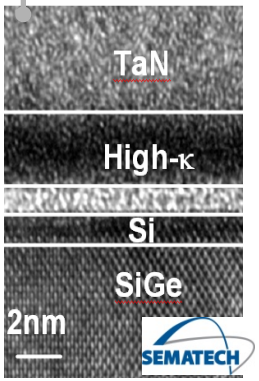


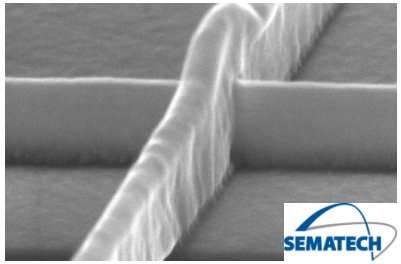
Characterization Issues:
- strain, E_g for III-V on Si
- III-V – HK interface
- Doping

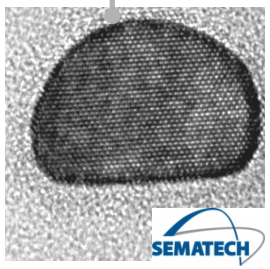
Many options!

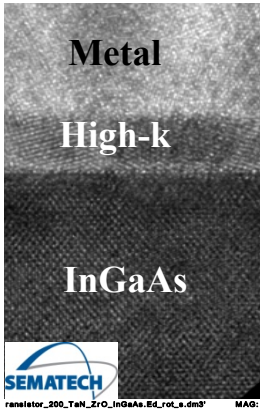
2009 | 2011 | 2013 | 2015 | 2017 | 2019







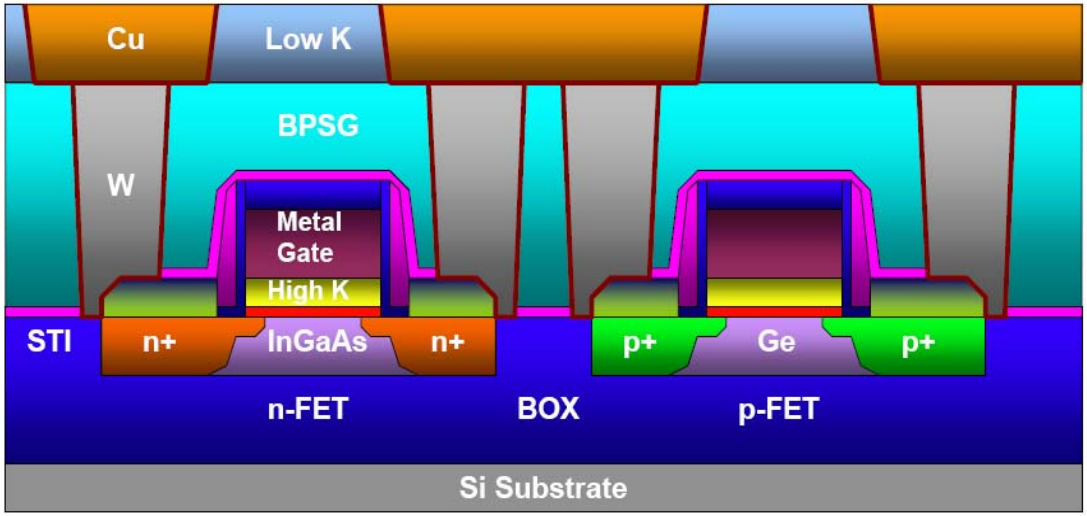




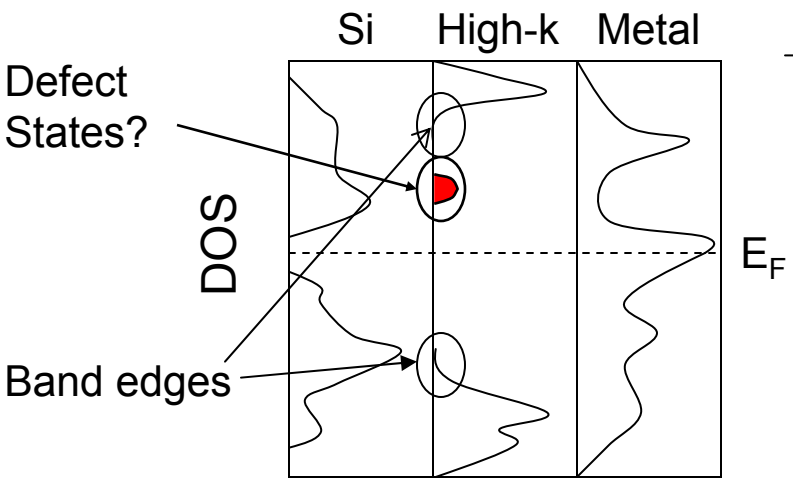
Alternative Channel Materials

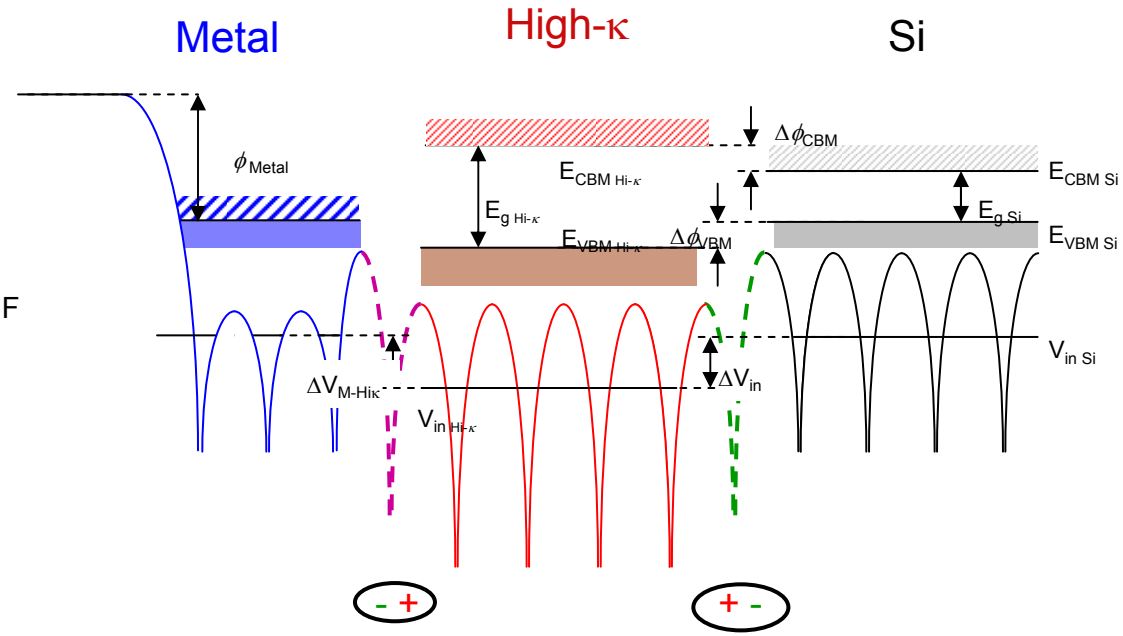
- Mobility improves by straining Si, but CMOS scaling would benefit from yet higher mobility….try other semiconductors.
- A key challenge for alternative channel materials is passivation – need low interface and bulk defect concentration.
- Need high I_{on}/I_{off} ratio, appropriate integration, high thermal stability, appropriate band alignment with no E_f pinning, etc.
- Ge and SiGe studied for years for CMOS; now III-Vs as well.

- InGaAs-on-insulator: NFET (surface channel)
- Ge-on-Insulator: PFET (surface channel)



Electronic structure across multilayer stacks



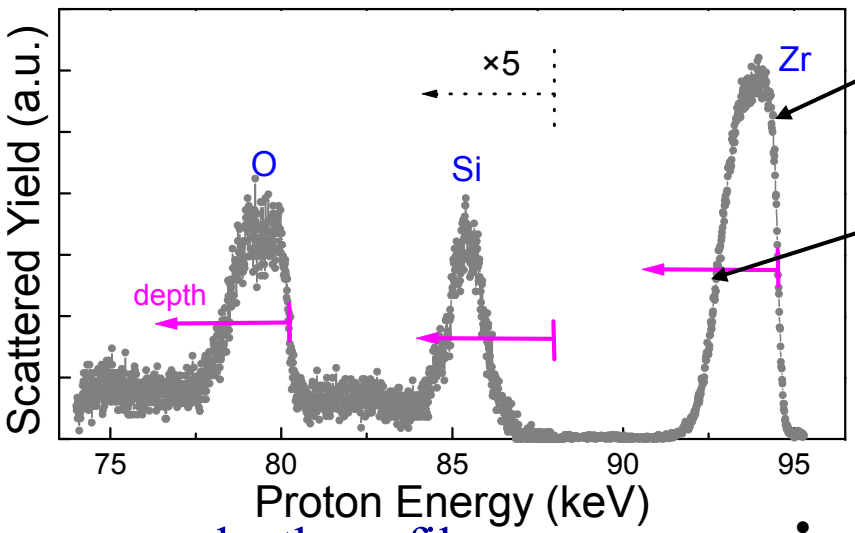


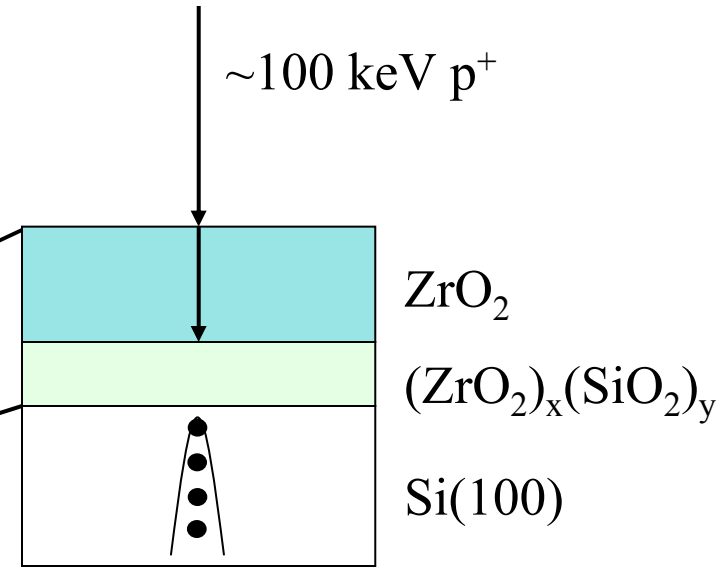
Band alignment, "effective" work function, energy gap…

- Band edge energies determined in many ways – elec. and optical spec.
- Can we use spectroscopies to (i) measure energies and LDOS more precisely, (ii) determine interface dipoles and band alignment, and (iii) use interface engineering to control effective work function…

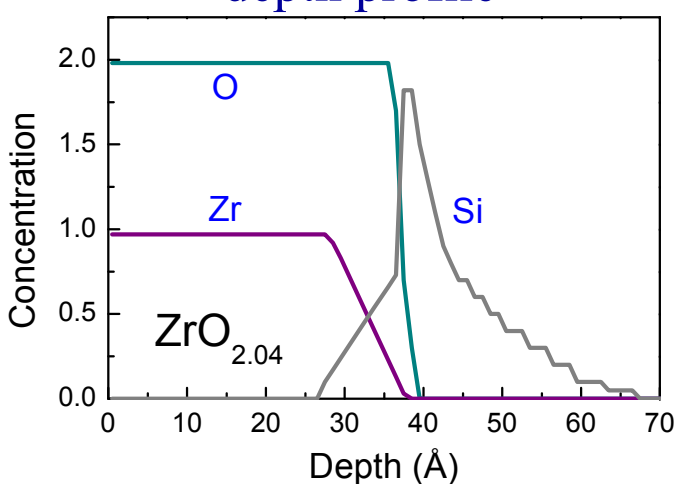
Ion scattering: MEIS

Backscattered proton energy spectrum



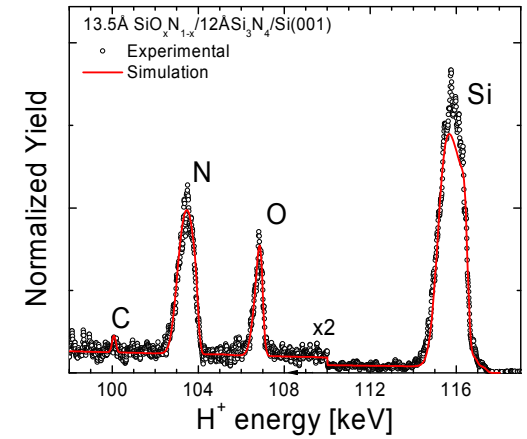


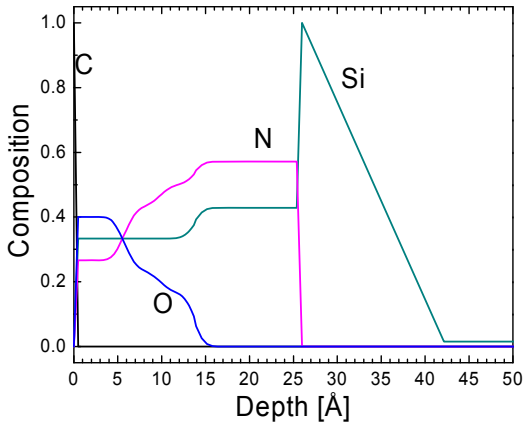
depth profile

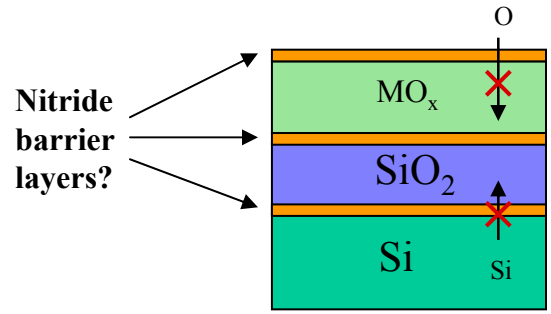


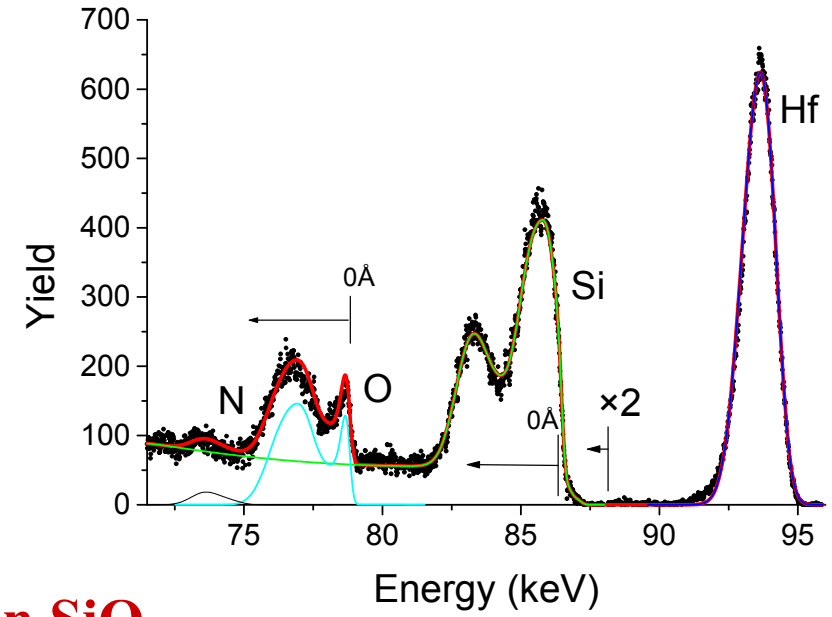
- **Sensitivity**:
  ≈ 10^{+12} atoms/cm^2 (Hf, Zr)
  ≈ 10^{+14} atoms/cm^2 (C, N)
- **Accuracy** for determining total amounts:
  ≈ 5% absolute (Hf, Zr, O), ≈ 2% relative
  ≈ 10% absolute (C, N)
- **Depth resolution**: (need density)
  ≈ 3 Å near surface
  ≈ 8 Å at depth of 40 Å

Nitride dielectric layers and diffusion barriers





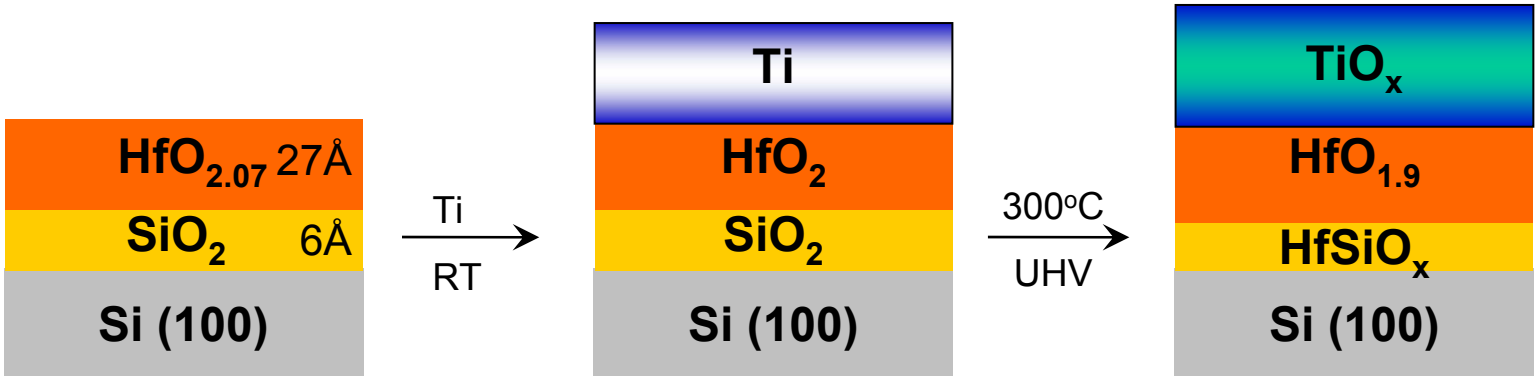


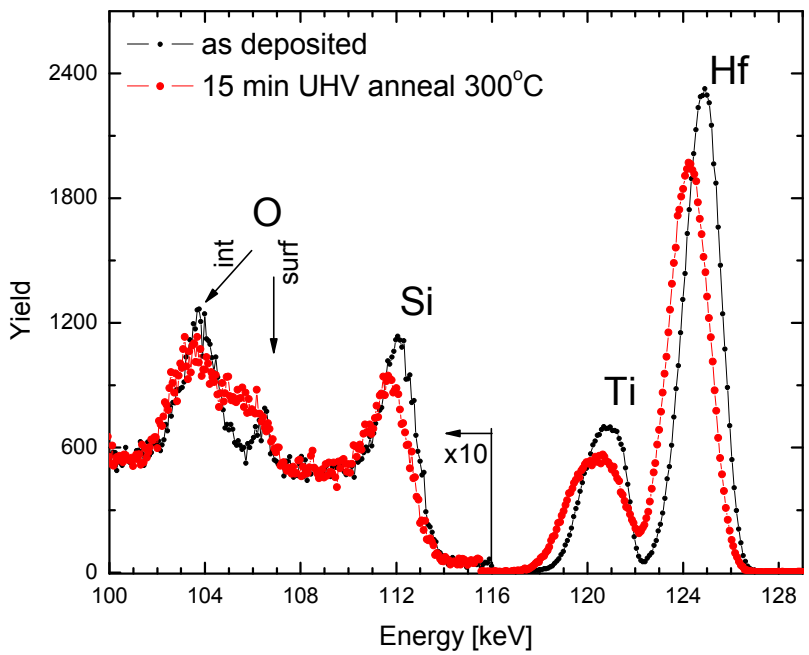


- **SiN has a higher permittivity than SiO_2.**
- **Nitride layers help slow dopant diffusion and silicate formation**
- **Nitridation also raises crystallization temperature of some oxides.**

Gate metal effect on chemical stability of dielectrics

Metal as source or sink for oxygen/hydrogen



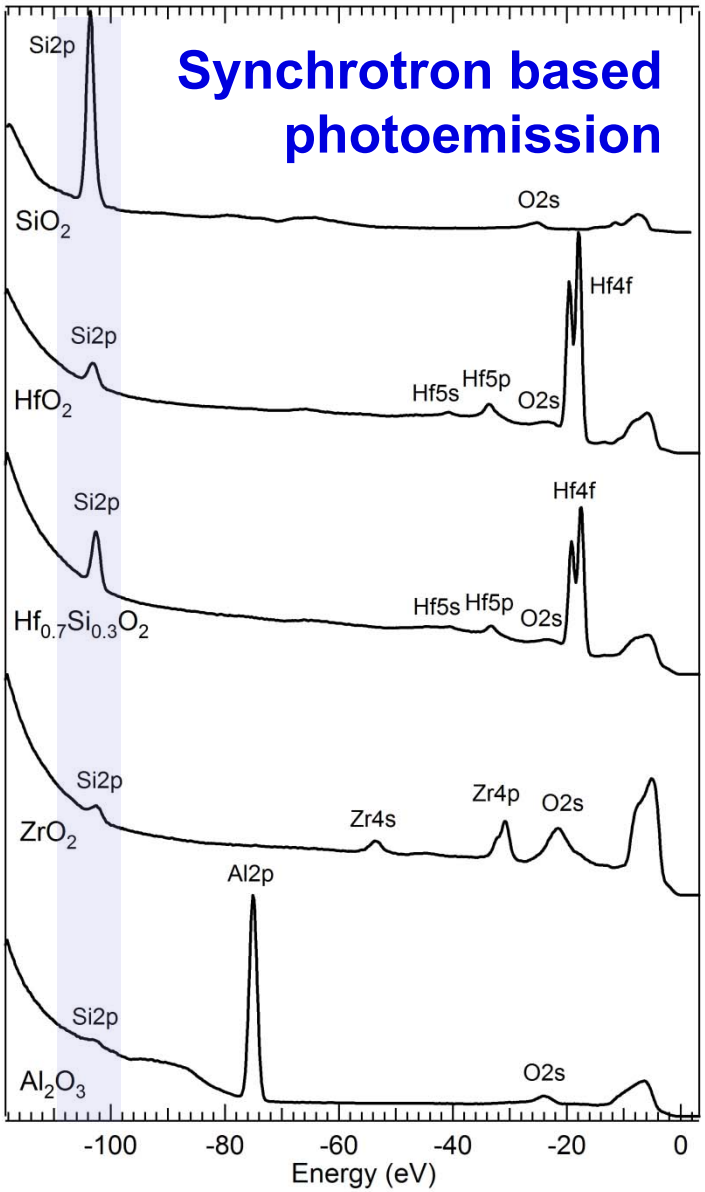


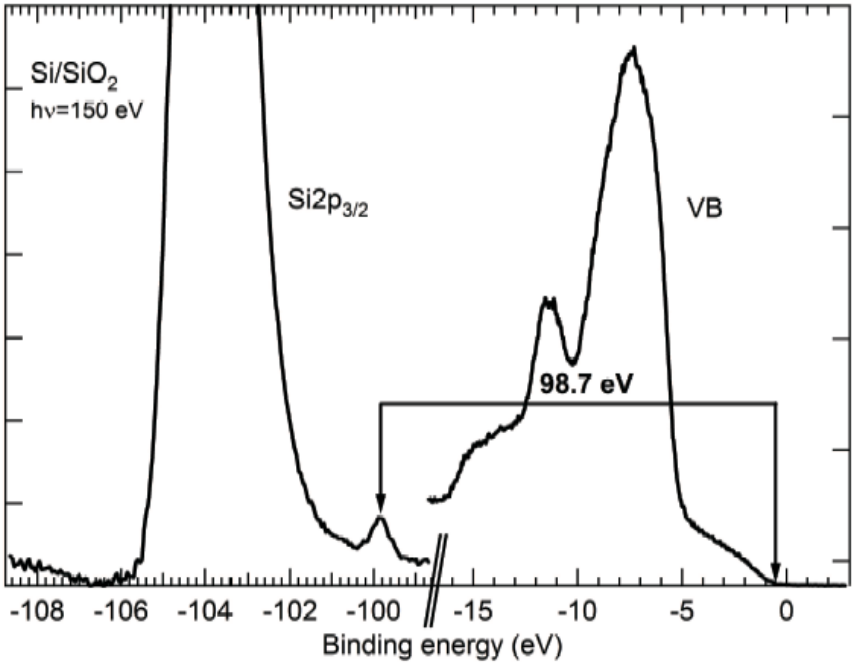
- Initial HfO_2 film has small amount of interfacial SiO_2 (~6-7Å) and excess of oxygen (~$HfO_{2.07}$)
- Deposited Ti forms uniform layer, no strong intermixing with HfO_2;
- Oxygen concentration in Ti layer is small

<u>After UHV anneal at 300°C for 15 min:</u>

- Lowering and broadening of Ti peak
- Hf and Si peak shift and O peak changes

⇒ Ti layer partially oxidized





Core level information

Film quality : MEIS, XPS

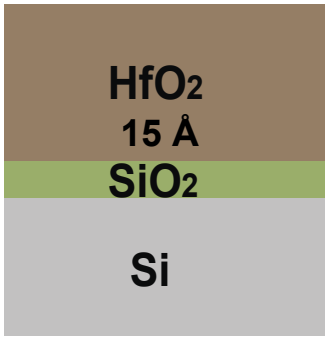
Thin oxides 15 to 30 Å

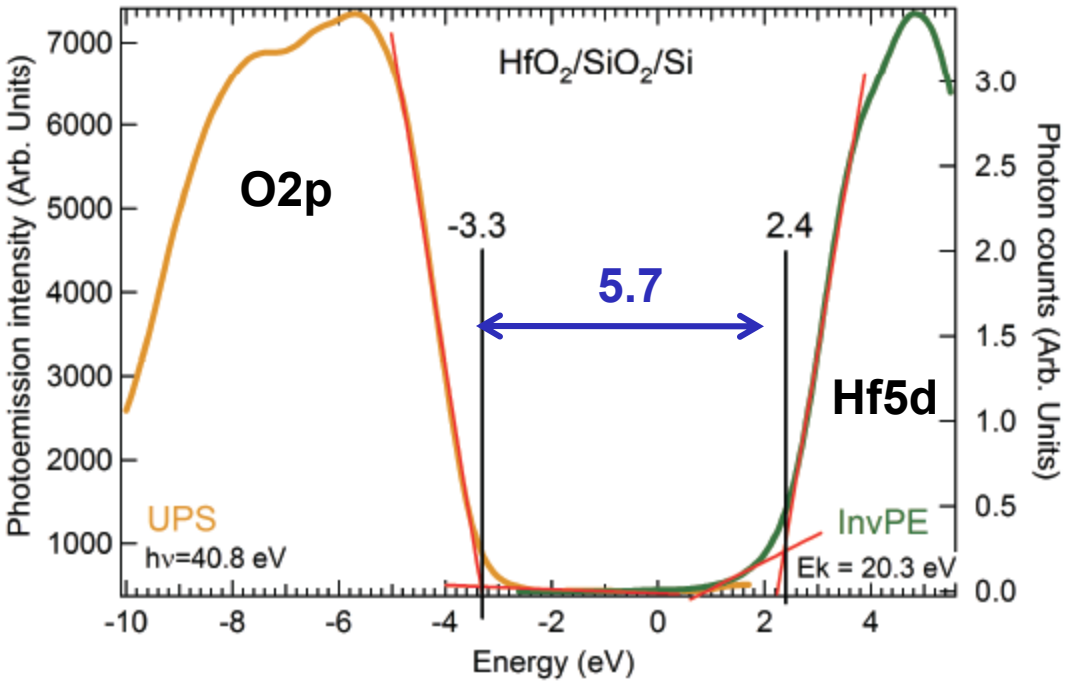
Silicon bulk contribution

Photoemission and inverse photoemission of $HfO_2/SiO_2/Si$

Single chamber

UHV measurments





Gap determination

Substrate band edges determination

↓

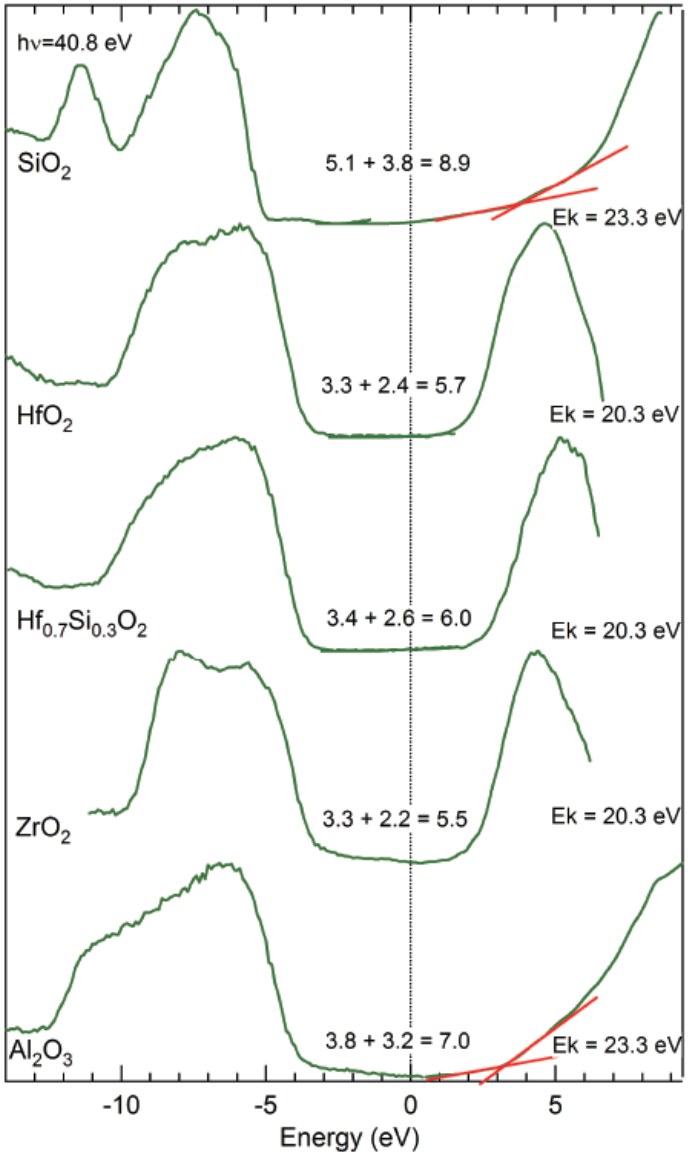
Band offsets

DOS, band gap and alignment results

Single chamber measurements

Spectra shifted to set zero at the intrinsic Fermi level of silicon

Gaps and band offsets comparable to literature



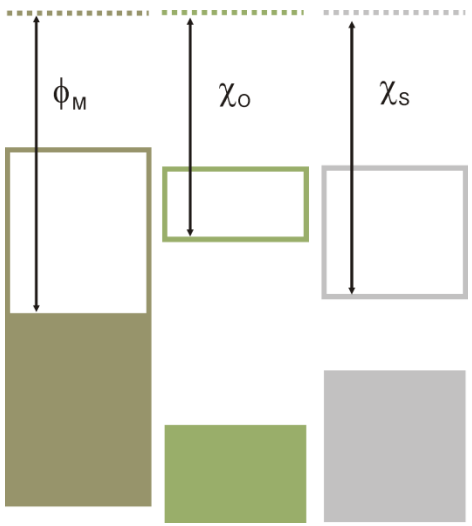
Band alignment models

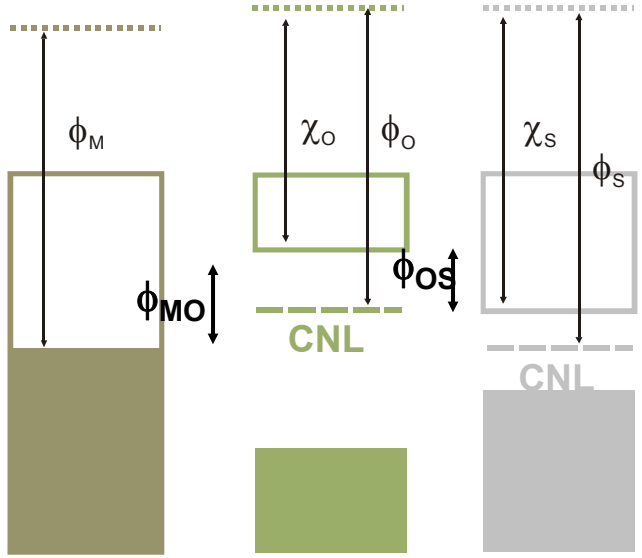
Semi-empirical model

Schottky limit

S = 1

→ No pinning





$$\phi_{MO} = S\,(\phi_M - \phi_O) + (\phi_O - \chi_O)$$

$$\phi_{OS} = (\chi_O - \phi_O) - (\chi_S - \phi_S) + S\,(\phi_O - \phi_S)$$

S = pinning parameter

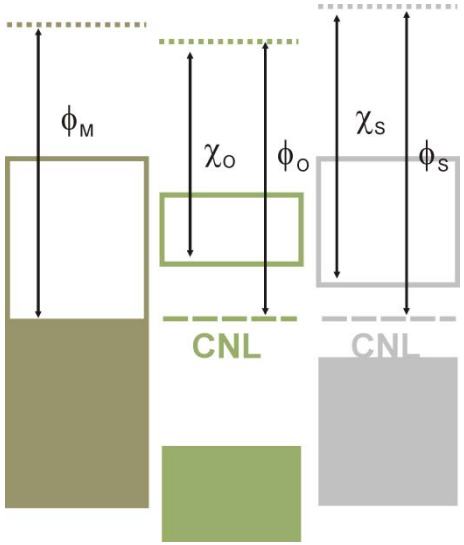
Reality is in between

Alignment of the CNL modified by S

Bardeen limit

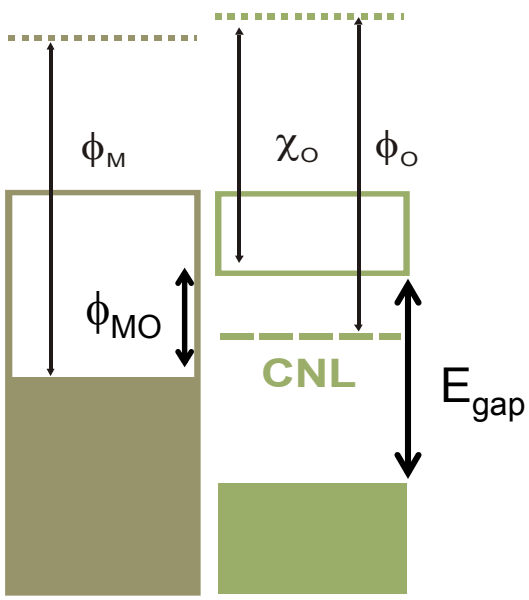
S = 0

→ Strong pinning



Robertson, Demkov, et al

$Ru/HfO_2/Si$: Metallization and Work Function



$$\phi_{MO} = S\,(\phi_M - \phi_O) + (\phi_O - \chi_O)$$

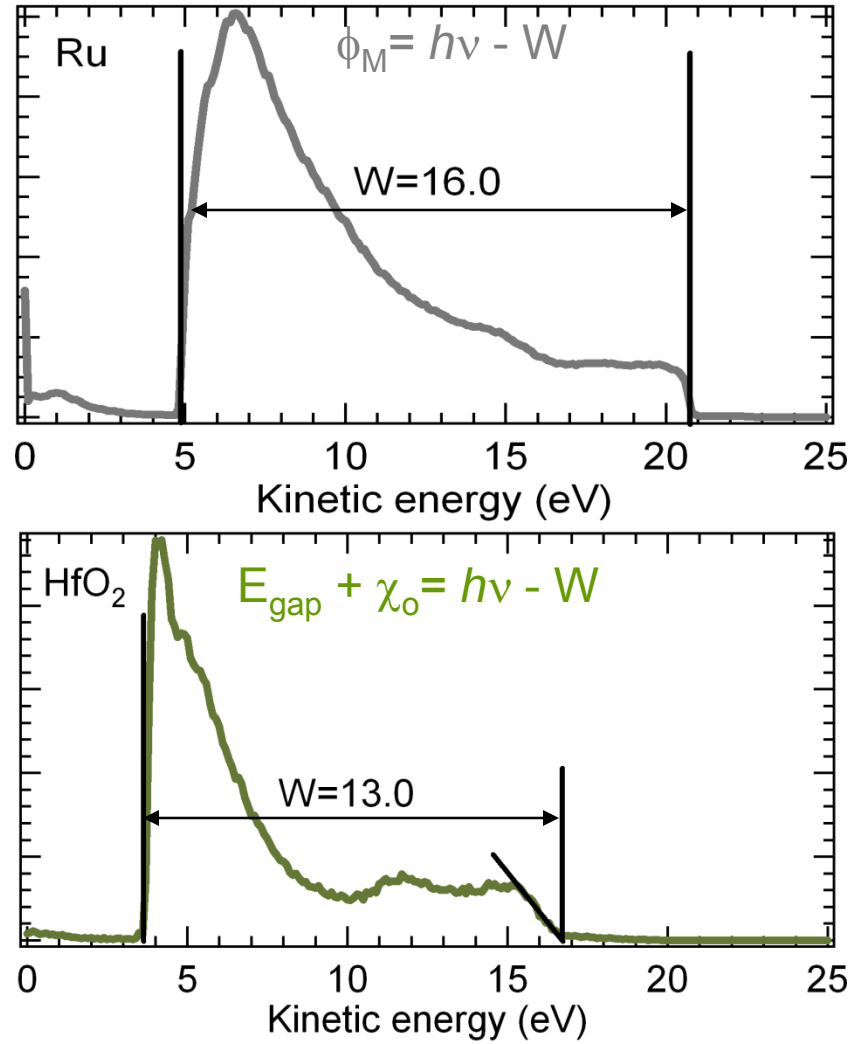
S=0.53 CNL=3.7

Robertson, JVSTB,18,1785, 2000

Theoretical prediction of the conduction band offset for the Ru/HfO2 interface

ϕ_{MO}=2.8 eV

Energy values used in model can be extracted directly from experimental data



Work function – real and linguistic issues

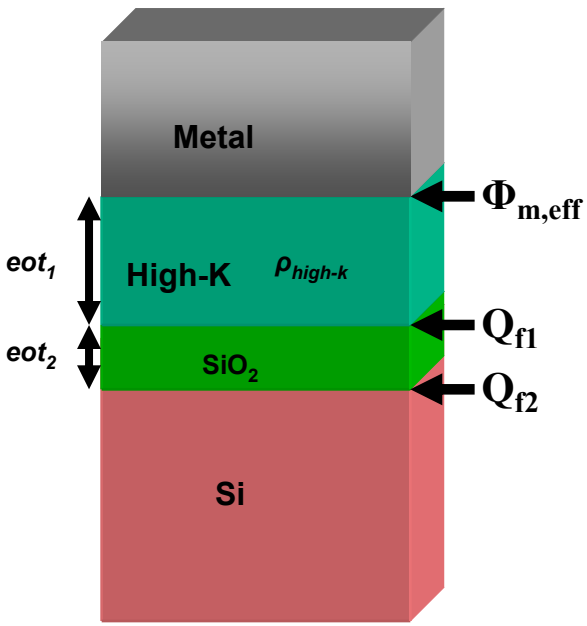
- Work function (or vacuum work function) – minimum energy to remove an electron from a solid to a distance >1nm.

  work function ≠ electrochemical potential

$$(E_N - E_{N-1}) \rightarrow \left(\frac{\partial A}{\partial n}\right)_{T,V} = \bar{\mu}$$

- Many ways to measure work function: UPS, kelvin probe, thermionic emission….

- "Effective work function" in devices – fictitious quantity, qualitatively assumed to be related to the real work function, that is used to explain band alignment between solids

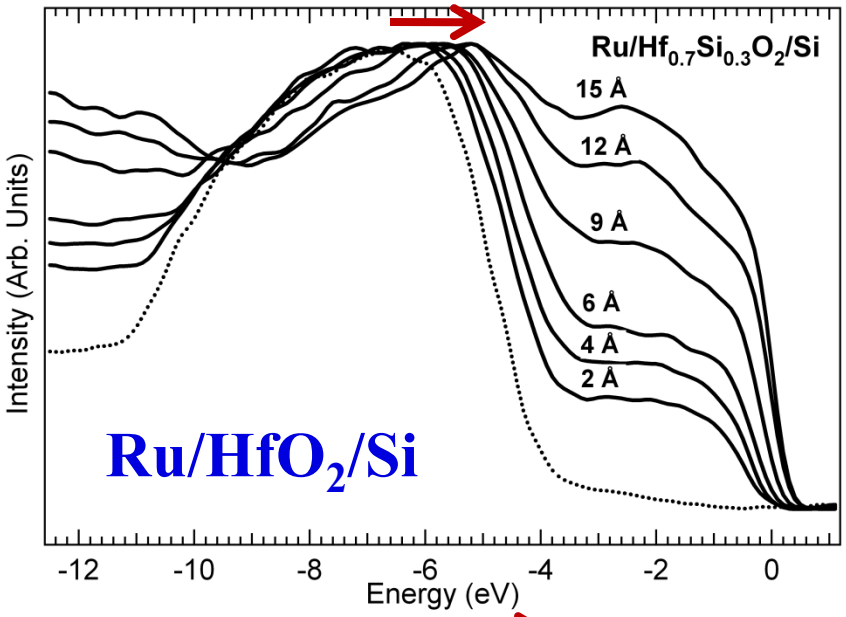


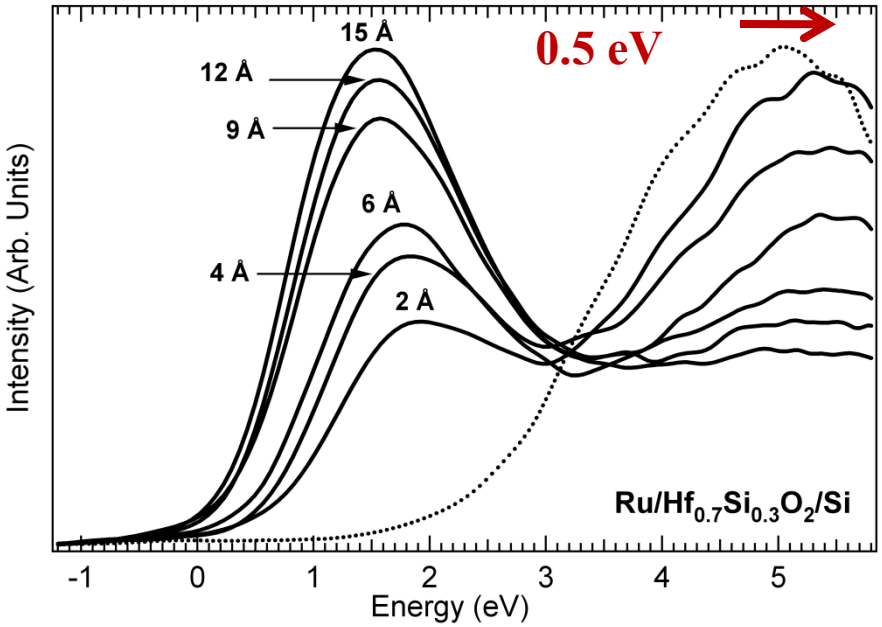
$$\Phi_{m,eff} = \Phi_{m,vac} + \Delta\Phi_{m,charge} + \Delta\Phi_{m,MIGS,dipoles,reaction}$$

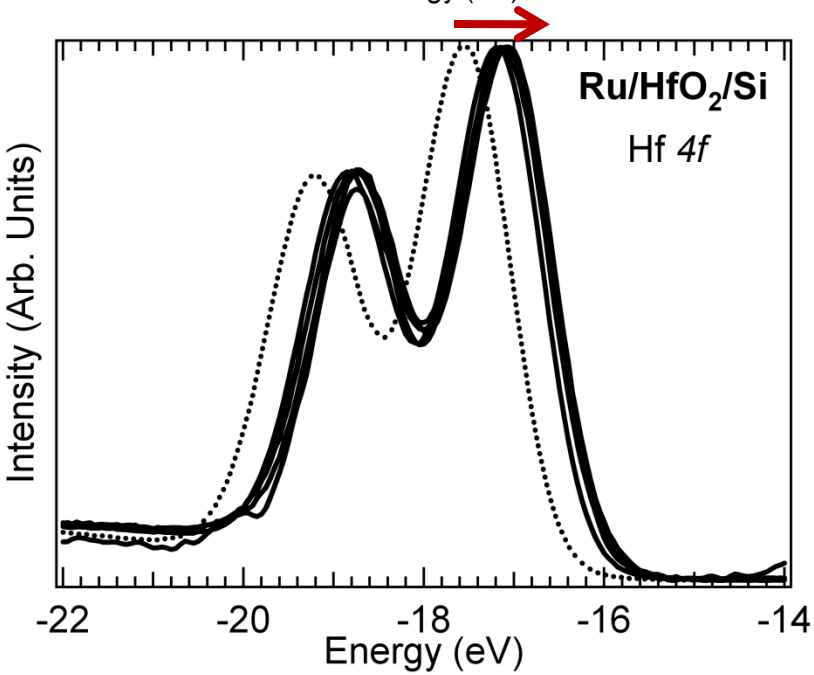
$$V_{FB} = \Phi_{m,eff-s} + \frac{1}{\varepsilon_{OX}}\left(Q_{f1} eot_2\right) - \frac{1}{\varepsilon_{OX}}\left(Q_{f1} + Q_{f2}\right) eot$$

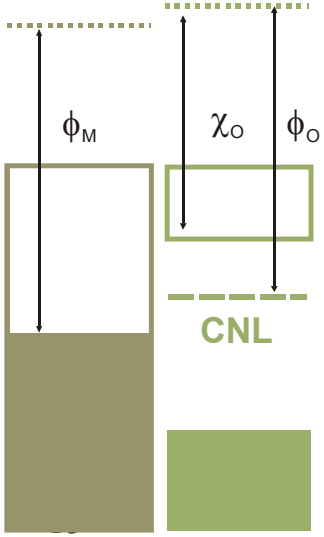
$$V_{fb} = (\underline{\underline{\Phi'_{ms}}} - \frac{Q_i * EOTh}{\varepsilon_{ox}} - \frac{\rho_b * (\varepsilon_h / \varepsilon_{ox}) * EOTh^2}{2 * \varepsilon_{ox}} + \underline{\underline{\Delta D + \Delta Q}}) - \frac{Q_f * EOT}{\varepsilon_{ox}}$$

UTA, Sematech, NCSU, etc.









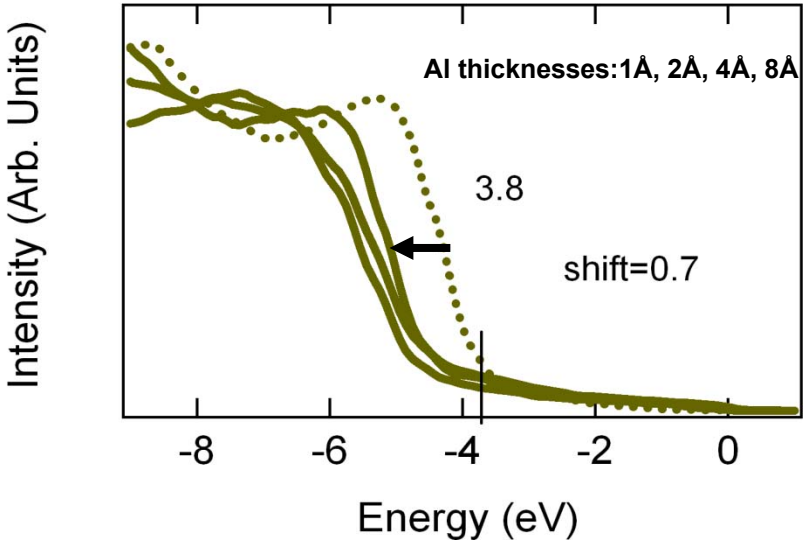
$$\phi_{MO} = S\,(\phi_M - \phi_O) + (\phi_O - \chi_O)$$

S=0.53 CNL=3.7

Robertson, JVSTB,18,1785, 2000

Theoretical shift: 0.4 eV

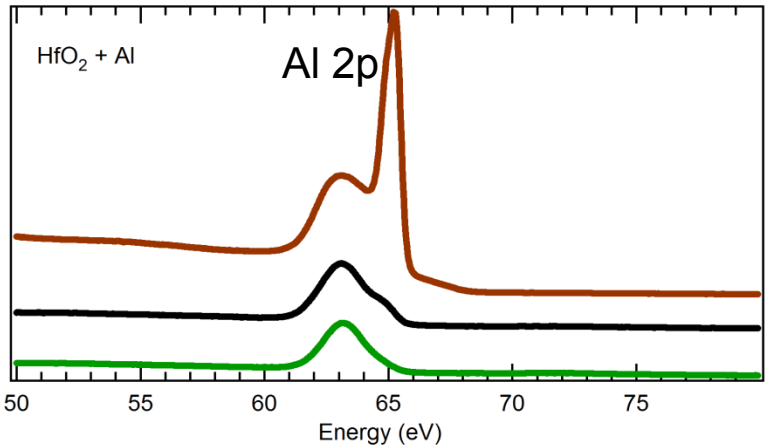
Al/HfO_2/Si



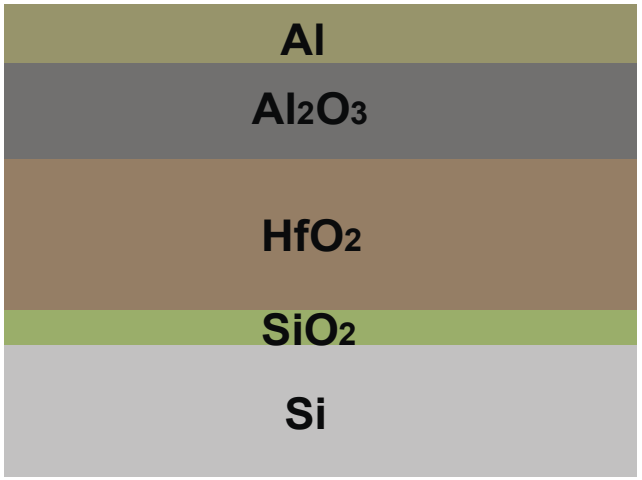
$\Delta E_{C\text{-}MO} = E_{C\text{-}O} + \text{shift}$
$= 2.2 - 0.7$
$= 1.5$ eV measured

$\Delta E_{C\text{-}MO} = 2.1$ eV predicted

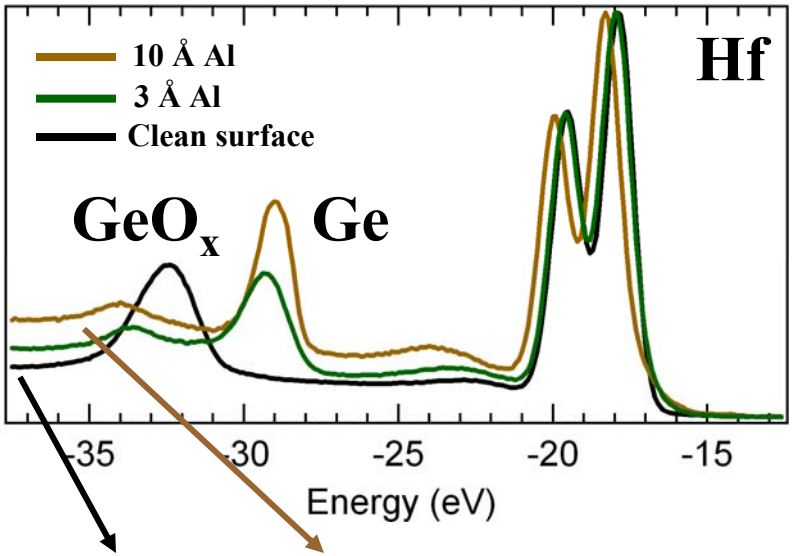
Why is the agreement so poor?

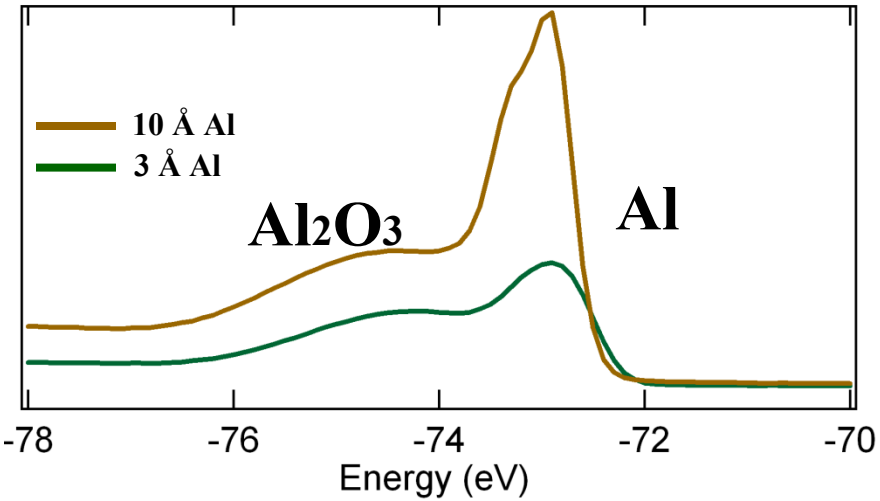


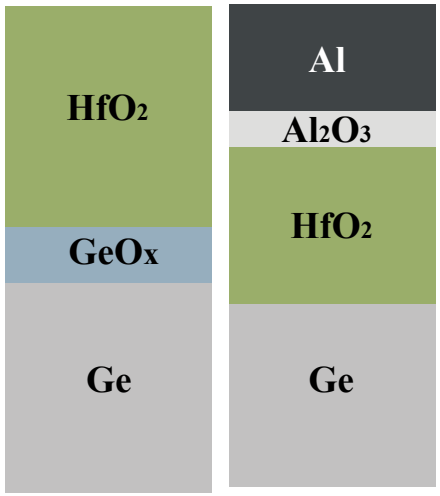
Oxidation of Aluminium
Formation of a Al_2O_3 layer



Al/HfO_2/GeO_x/Ge



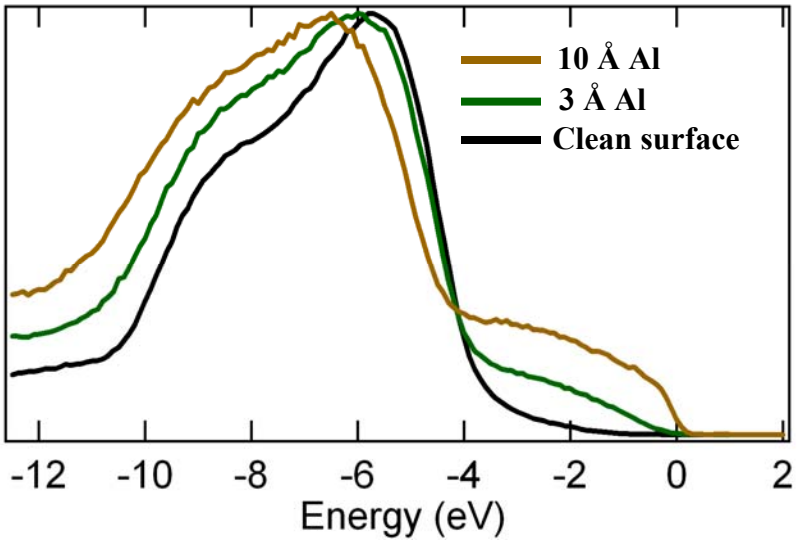




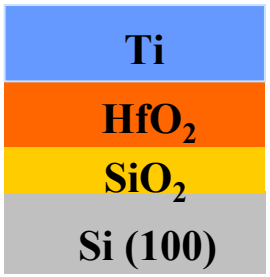
Hf4f and VB shift

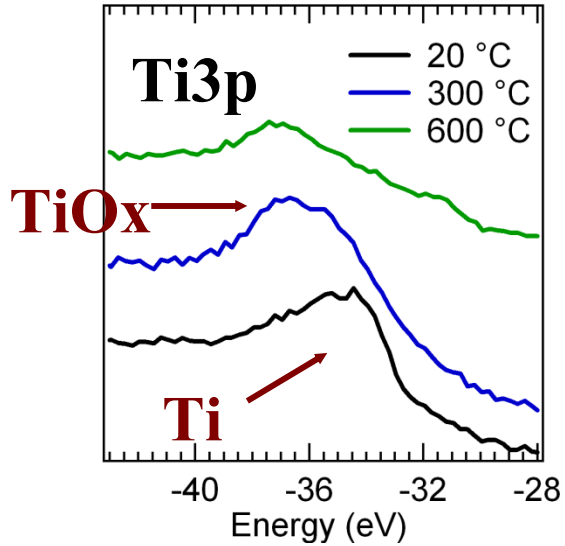
No significant reduction of HfO_2 in Hf4f

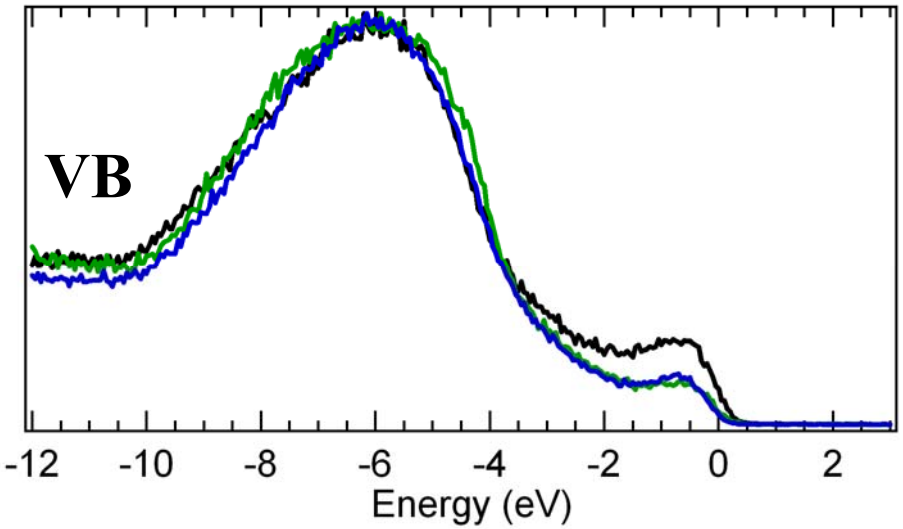
Interfacial oxide reduction at 300 K

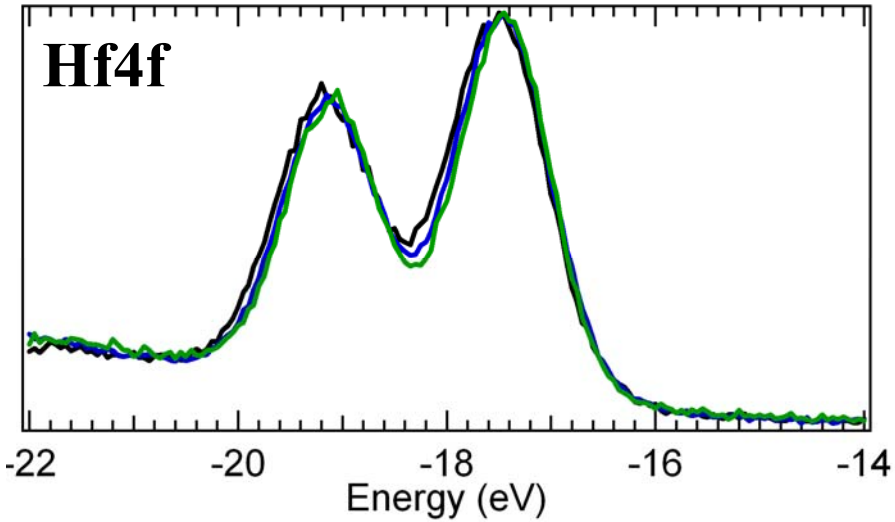


$Ti/HfO_2/SiO_2/Si$





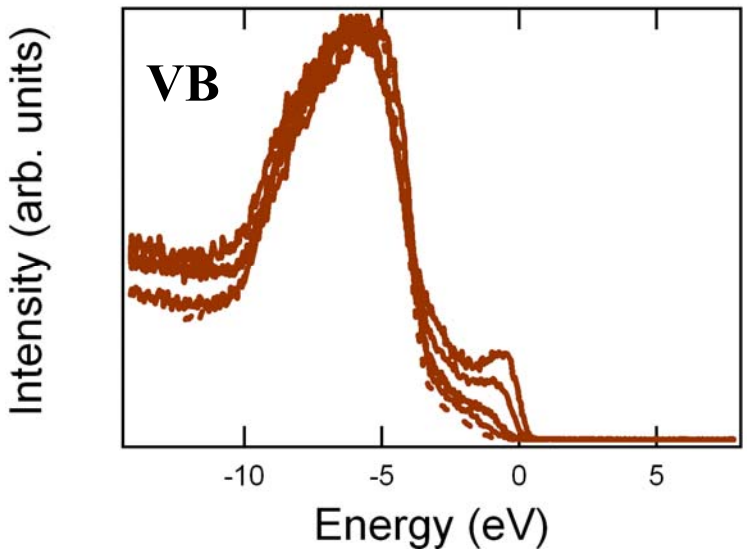


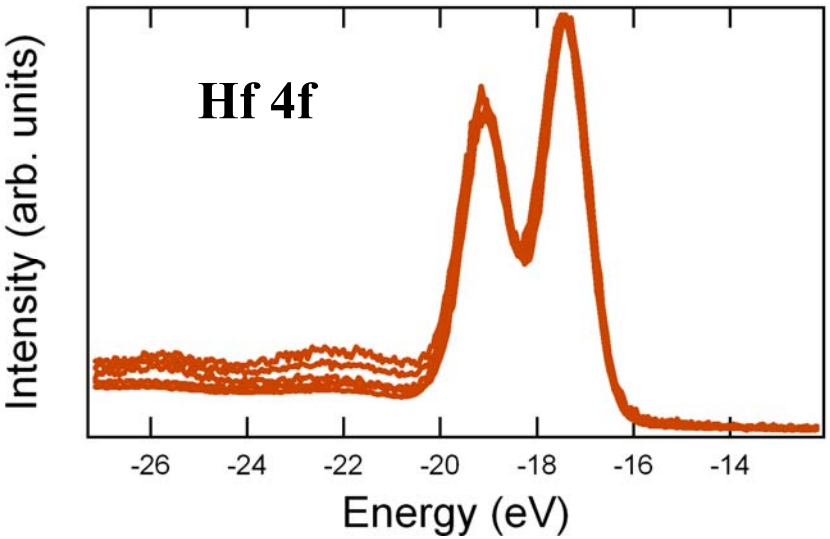


Partial Ti oxidation at 300 °C
No strong chemical shift of Hf4f

No reduction of HfO_2

Ti/HfO_2/Si: no shift of HfO_2 features





Ti thicknesses: 1,3,5,9 Å

$$\Delta E_{C\text{-}MO} = E_{C\text{-}O} + \text{shift}$$
$$= 2.2 + 0.0$$
$$= 2.2 \text{ eV measured}$$

$$\Delta E_{C\text{-}MO} = 2.1 \text{ eV predicted}$$

Fundamental understanding of band alignment (conduction band)

	Ru		Al		Ti	
Oxide	Expt	MIGS	Expt	MIGS	Expt	MIGS
HfO_2	2.4	2.5	1.5	1.9	1.8	1.9
$Hf_{0.7}Si_{0.3}O_2$	2.4	2.4	1.5	1.8	1.7	1.8
SiO_2	3.8	3.9	3.4	3.0	3.1	3.0
Al_2O_3	3.0	2.7	2.0	2.0	2.4	2.0

Agreement between experimental CBO and MIGS-predicted CBO when no metal-induced interface oxide is present.

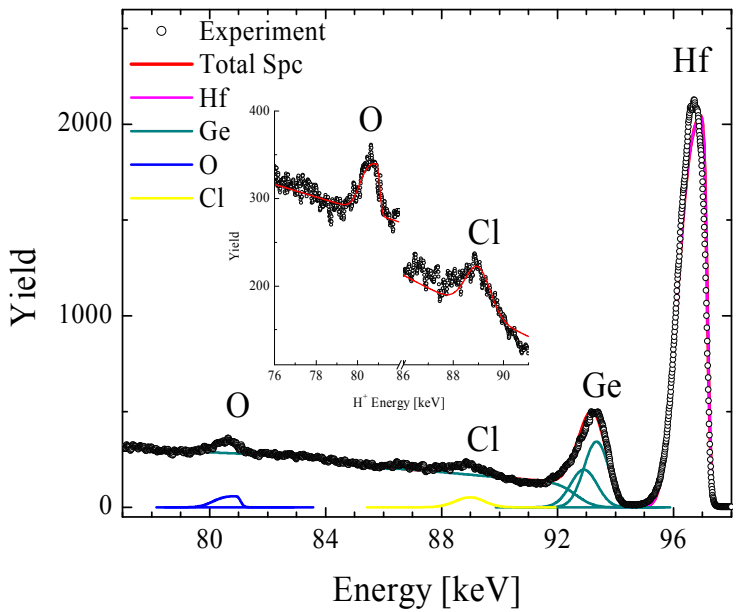
Band offsets of a ruthenium gate on ultrathin high-k oxide films on Si, Rangan et al., Phys. Rev. B 79 (2009) 075106

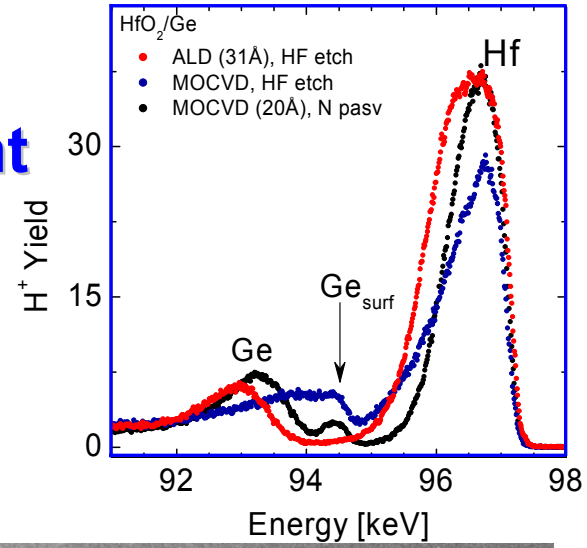
Aluminum gate interaction with ultrathin high-k oxide films on Si, Rangan et al., submitted APL

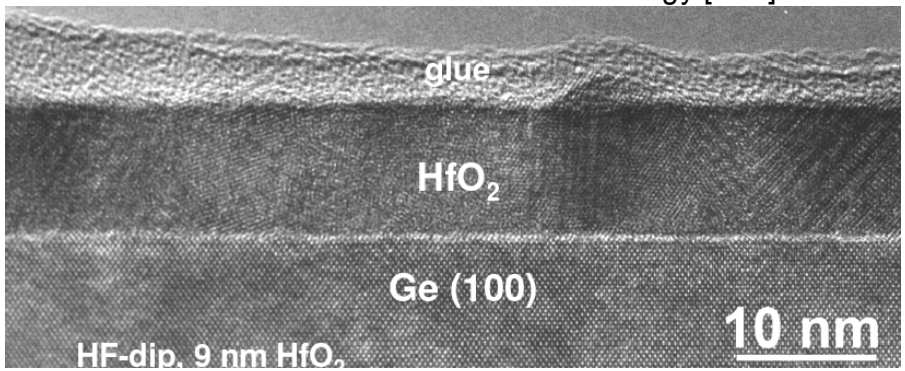
Band offsets of a Ti gate with ultrathin high-k oxide films on Si, Rangan et al., manuscript in preparation

HfO_x/Ge (ALD and MOCVD)

Film properties very growth dependent





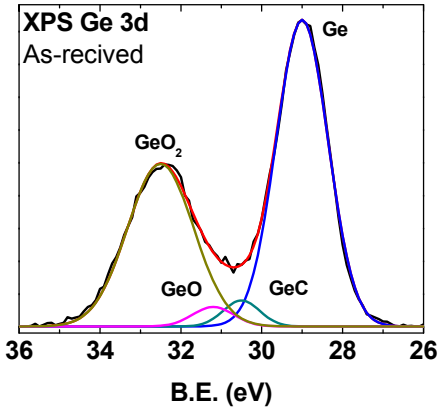


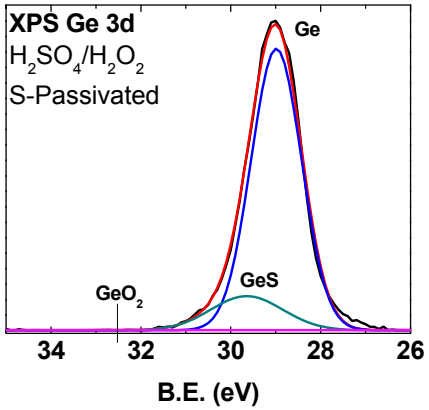
ALD little interfacial GeO_x (within sensitivity of the measurements)
some Cl accumulation at the interface
some epitaxial growth

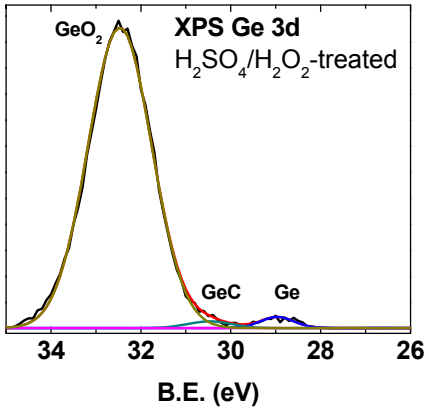
MOCVD HfGe and $HfGeO_x$ intermixing (condition dependent)
surface Ge (supressed by Ge nitridation)

W/Stanford, IMEC…

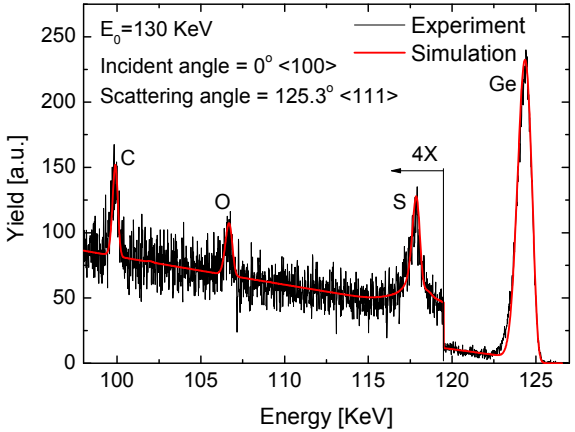
Ge surface preparation: cleaning and passivation

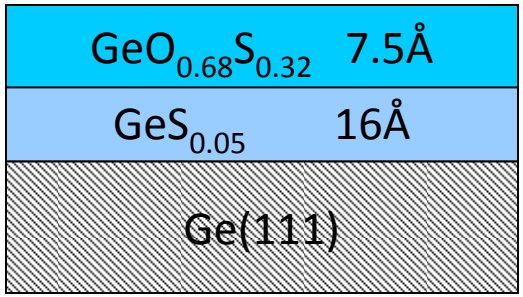




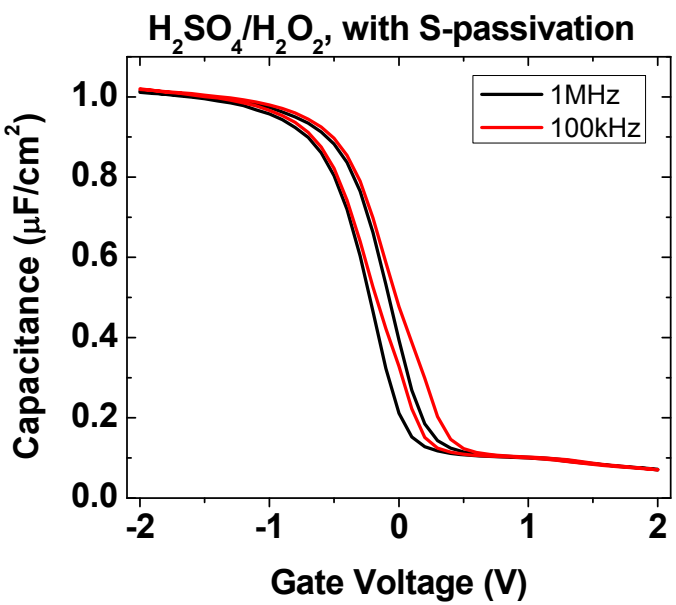


- Starting film - GeO_2, GeO, GeC and CH_x
- Oxidation/etch
  - GeO completely removed
  - GeC greatly reduced
  - GeO_2 formed as protective oxide ~10nm for H_2SO_4/H_2O_2-treated Ge
- Sulfur passivation by $(NH_4)_2S$ removes oxide and leaves S-Ge passivation layer



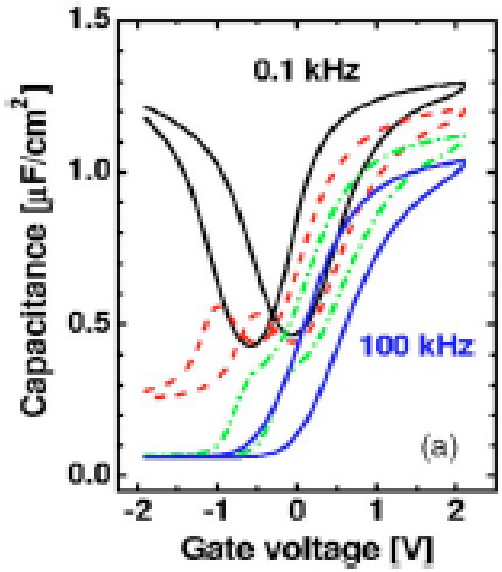


Cleaning	HF	HF/DIW/H_2O_2	H_2SO_4/H_2O_2 HF	H_2SO_4/H_2O_2
S-passivation	No	Yes	Yes	Yes
Q_i/e (cm^{-2})	4.00×10^{13}	4.17×10^{12}	3.56×10^{12}	3.19×10^{12}
Q_{HS}/e (cm^{-2})	1.15×10^{13}	2.09×10^{12}	1.5×10^{12}	9.72×10^{11}
ΔV_{FB_HS}(V)	0.31	0.29	0.22	0.15
D_{it} (eV^{-1} cm^{-2})	3.80×10^{12}	1.66×10^{11}	8.91×10^{10}	6.23×10^{10}



Prior work (lit.)

Current work

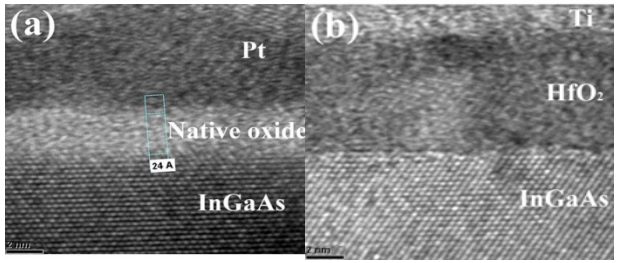


HfO_2 40A, hysteresis is ~0.15V.
Ge surface was first H_2SO_4/H_2O_2 treated.
No HF used before sulfidation in $(NH_4)_2S$.

77A HfO_2, hysteresis is ~0.5V.
10% HF etching for 10mins before sulfidation in $(NH_4)_2S$.
APL 89, 112905 (2006)

Interface reduction during ALD or metallization

- "Self-cleaning" during ALD growth is a phrase that described the concomitant reduction and removal of surface oxides from a substrate during the ALD process. It has been observed by several groups (P.D. Ye et. al.,APL, 83, 180; M. Frank et. al., APL, 86, 152904; C. Hinkle et. al., APL, 92, 071901).

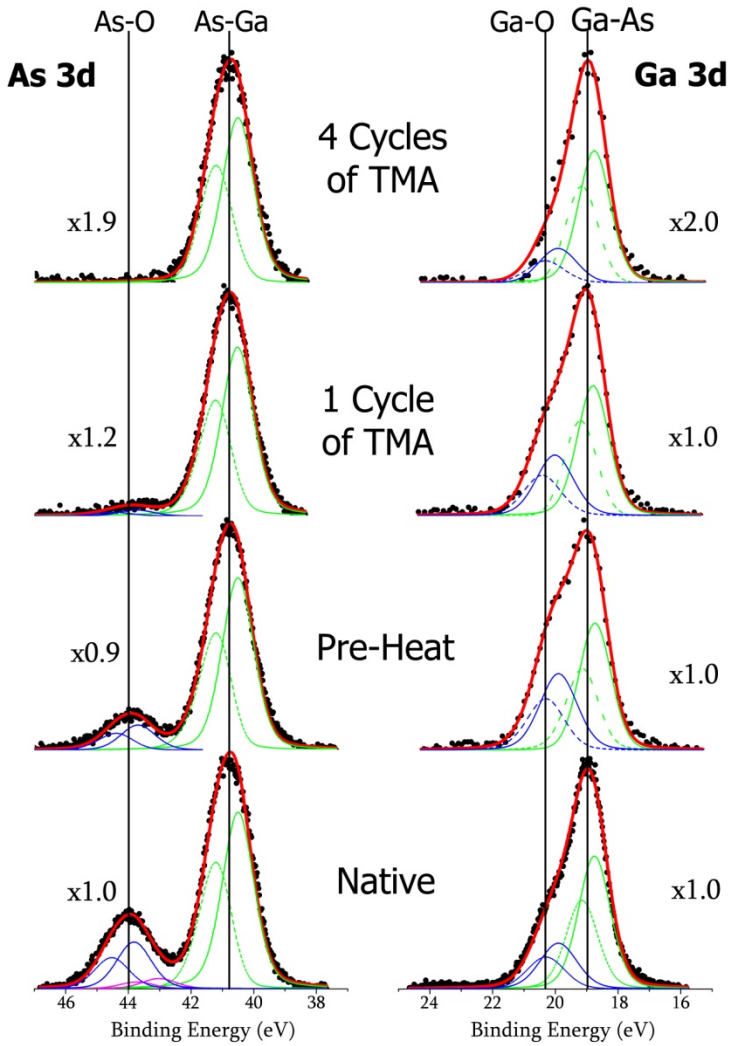


C.H. Chang et. al. (APL, 89, 242911)

- Some issues regarding "self-cleaning":

1. When does it occur? At the very first introduction of precursor or continuously through the growth?
2. Where do the surface chemical species go? Desorb or incorporate into the dielectric or substrate?
3. Can it help us prepare optimal gate stacks?
4. No detailed structural data reported regarding "self-cleaning".

XPS



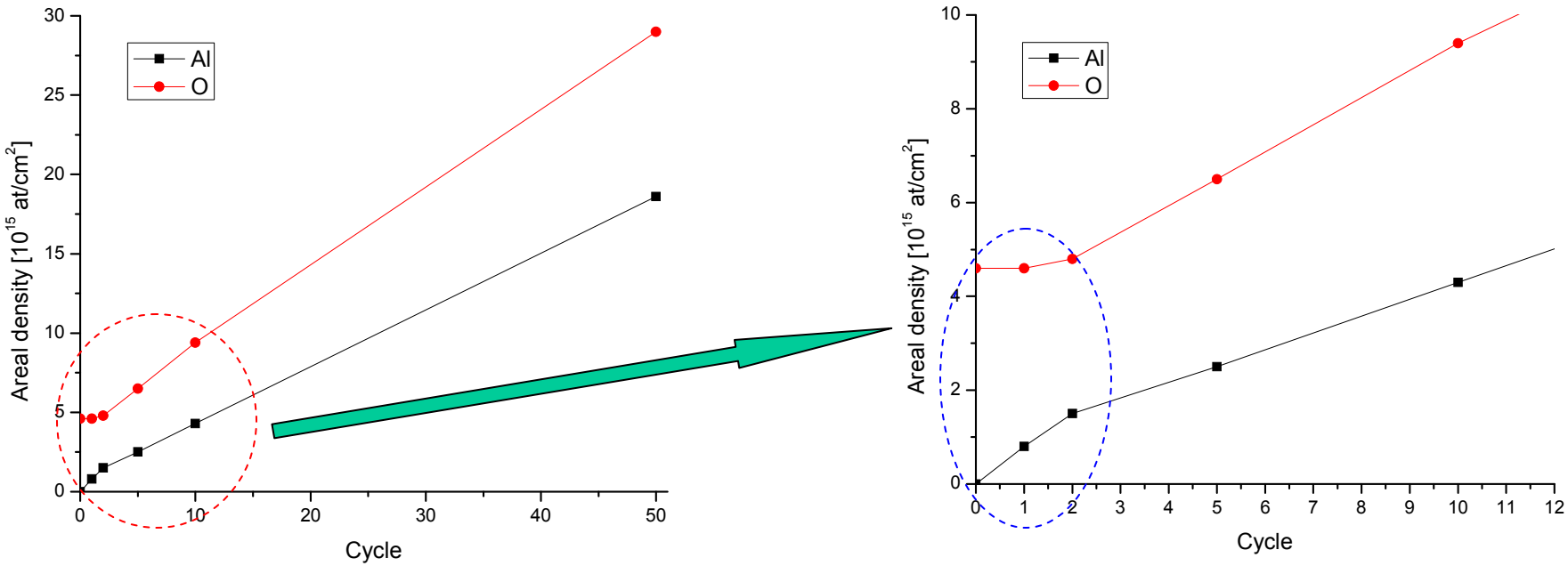
After preheating: Conversion of As_2O_3 (46% decrease) to Ga_2O_3 (47% increase) (relative to as-received wafer).

The native oxides in the preheated samples consist of a mixture of As_2O_3, As_2O_5 and Ga_2O_3. The Ga:As ratio (~2:1) is close to the one from MEIS (2.3:1).

After 1 TMA pulse: Decrease of the As-O (~75%) and Ga-O (~16%) peak areas, consistent with MEIS.

After 4 TMA pulses: Further decrease of As-O below the XPS detection level (to a lesser extent also Ga-O) - confirms the MEIS result.

Normal linear Al oxide ALD growth after the 2nd cycle

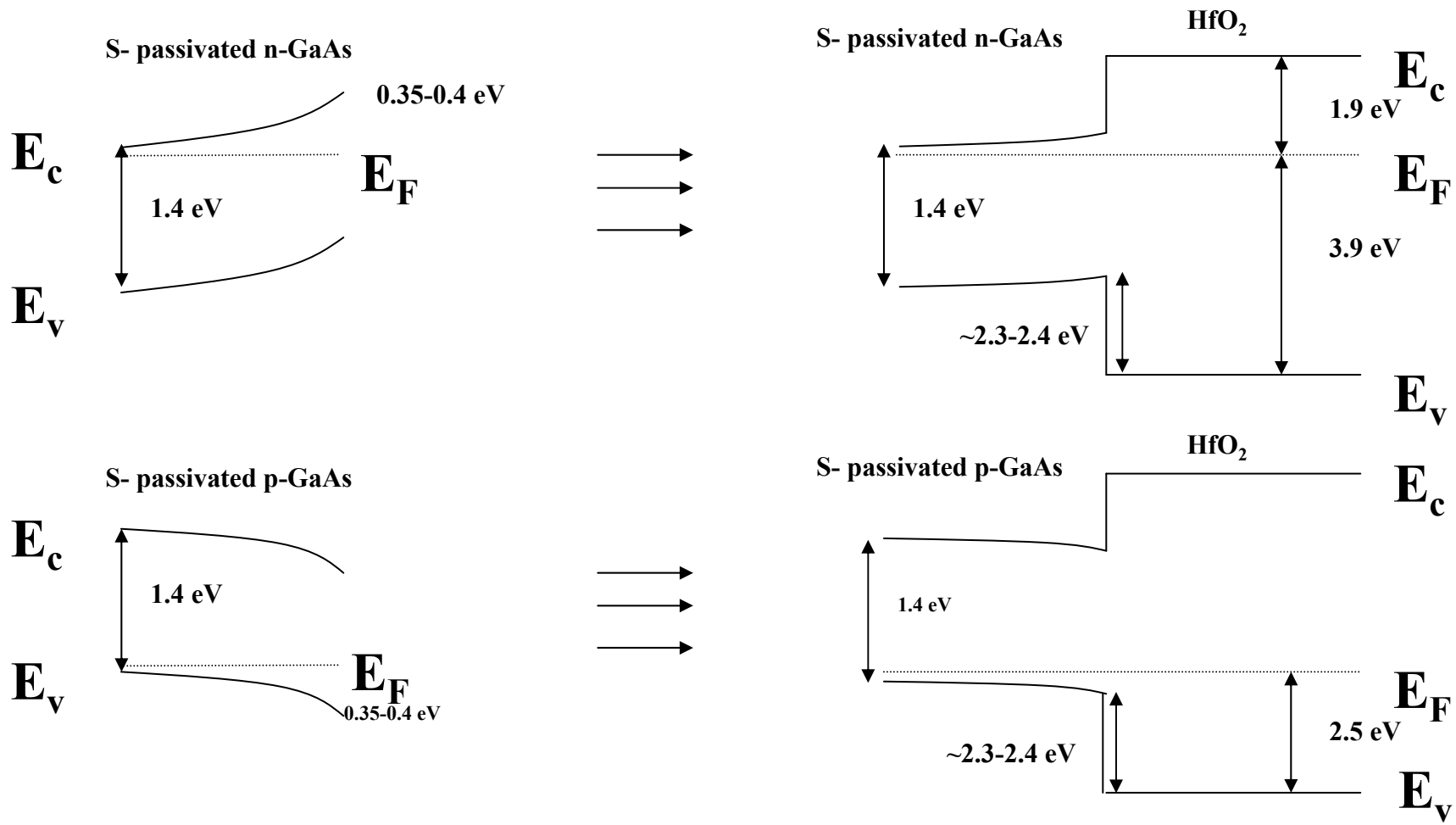


Areal Density (10^{15} at/cm^2)

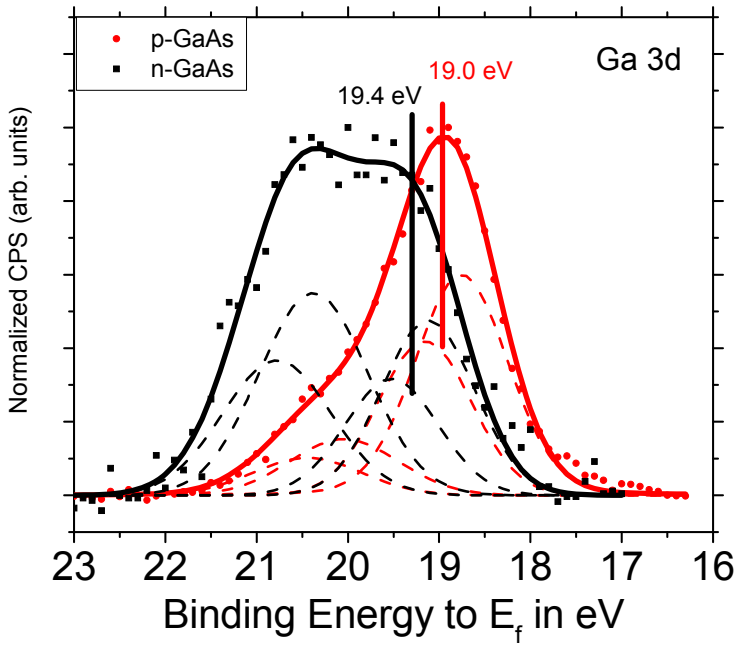
Cycle	0 (pre-heated)	1	2	5	10	50
Al	0	0.8	1.5	2.5	4.3	18.6
O	4.6	4.6	4.8	6.5	9.4	29.0

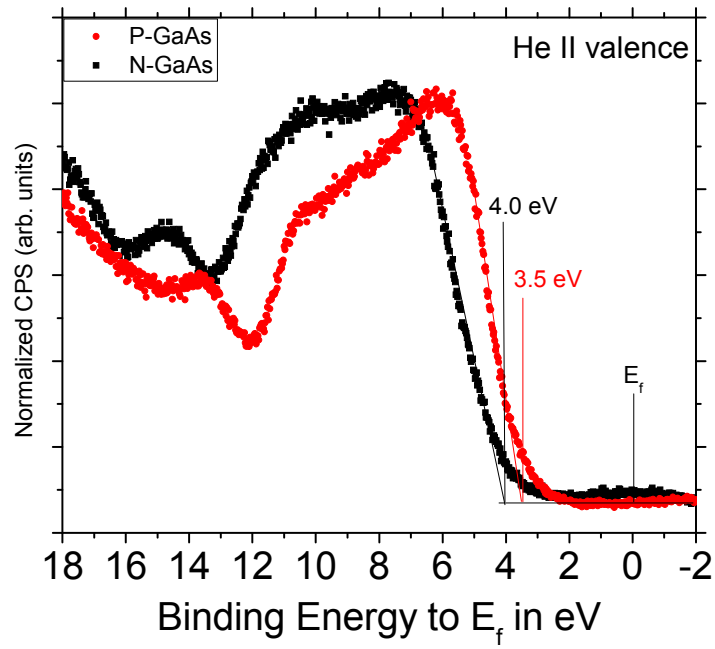
- **After self cleaning (2nd cycle) the Al oxide growth rate becomes slower.**

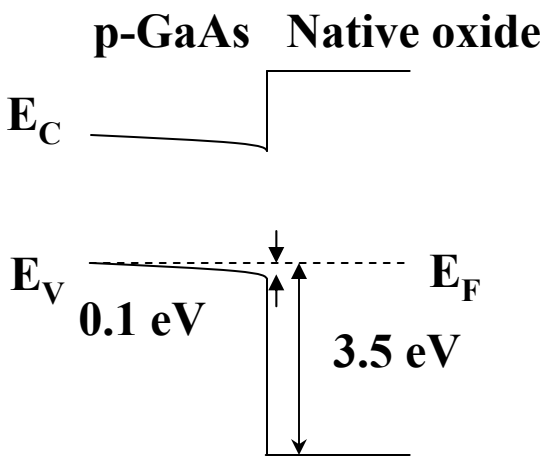
- On S-passivated films the Fermi level is partially pinned.
- After HfO_2 growth, much less pinning.
- Conduction and valance band offsets agree with literature.

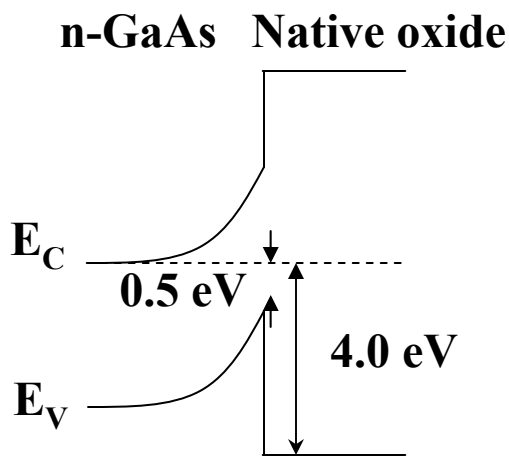


Band alignment of GaAs native oxide





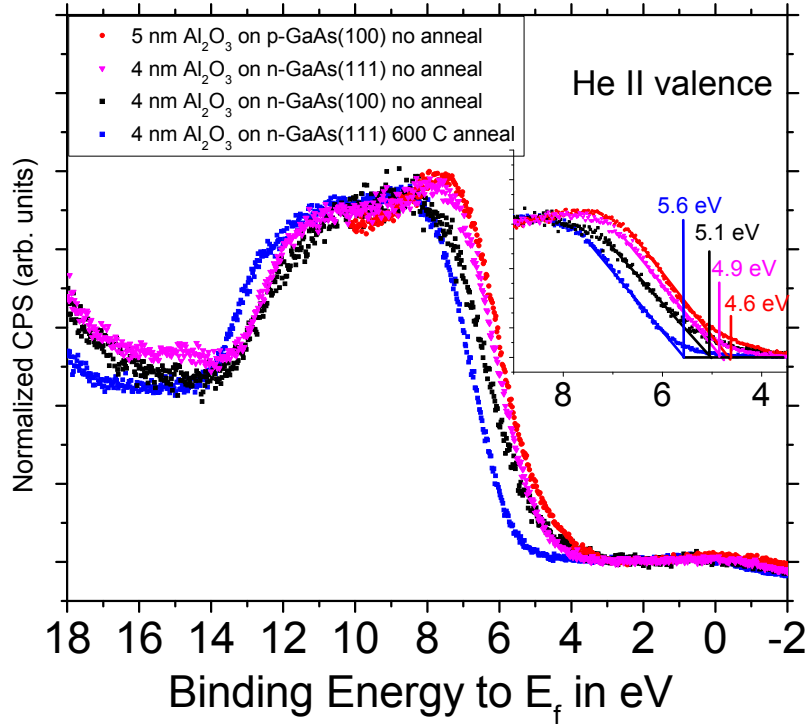


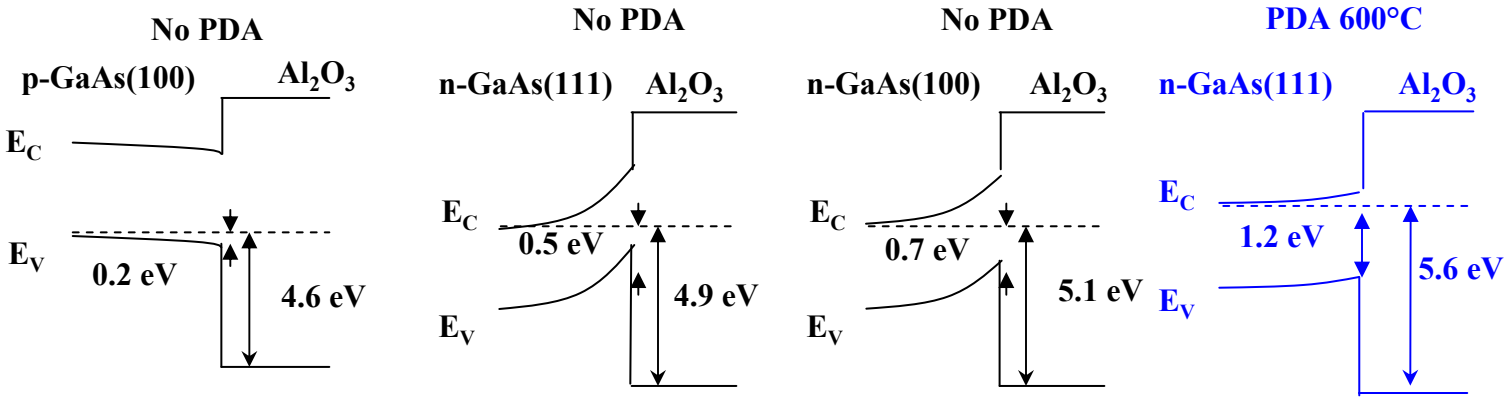


Pinning effects much stronger on n-GaAs than p-GaAs on native oxide surface

Improvement of band alignment with post-deposition annealing

- **Post deposition anneal (PDA) @ 600°C in forming gas for ~ 15 sec yields improved energy level alignment for both n-GaAs and p-GaAs**
- **Valence band offset = 4.4 eV**





Estimating the interface state density from band alignment

- Change in barrier height $\Delta\varphi$ vs change in work function $\Delta\Phi$
- Work function difference between n-GaAs and p-GaAs ≈ 1.4 eV
- Pinning parameter $S = \Delta\varphi/\Delta\Phi$ has been proposed to be related to the interface state density at $D(E_F)$ by:[2-3]

$$S = \frac{1}{[1 + (4\pi e^2/\varepsilon_i)\, D(E_F)\, \delta/A]}$$

- For no PDA 4nm Al_2O_3/GaAs, measured S = 0.3 eV/1.4 eV = **0.21**
  $D(E_F) = 5.2 \times 10^{11}$ cm^{-2} eV^{-1}
- For PDA 600°C 4nm Al_2O_3/GaAs, measured S = 1.0/1.4 = **0.71**
  $D(E_F) = 5.6 \times 10^{10}$ cm^{-2}eV^{-1}
- Maximum S value given by empirical formula determined by the *optical* dielectric constant:[4]

- For Al_2O_3, $\varepsilon_\infty = 3.1$, S = **0.69**

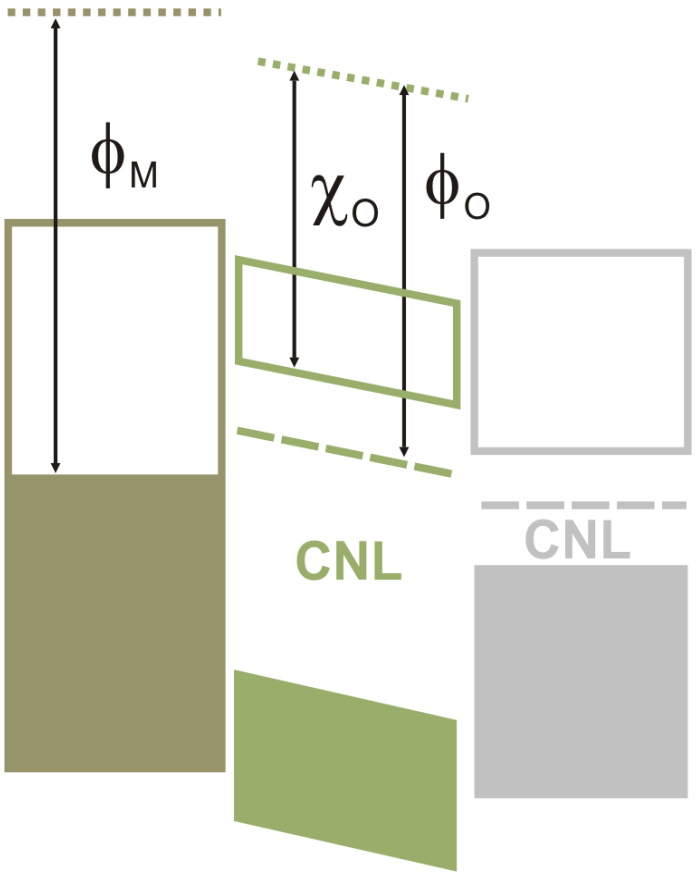
$$S = \frac{1}{1 + 0.1\,(\varepsilon_\infty - 1)^2}$$

2. C. Tejedor, E. Louis, F. Flores, *J. Phys. C* 10, 2163 (1977).
3. W. Mönch, "Semiconductor surfaces and interfaces" 3rd edition, Springer, New York (2001)
4. J. Robertson and J. Falabretti, *Mat. Sci. Eng. B* 136, 267 (2006)

Post-silicon CMOS take home messages:

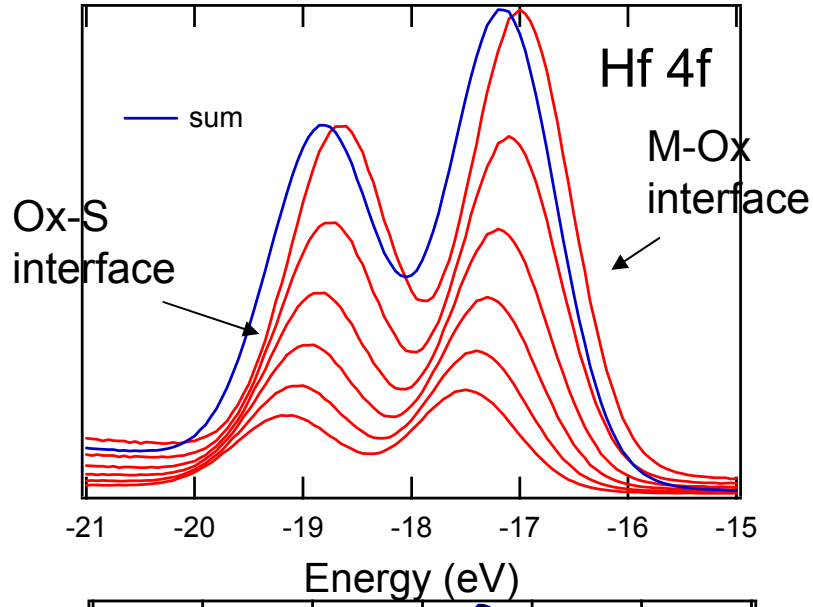
- High-K dielectrics and metal gates are in product!
- Very good devices can and have been grown on Ge and III-Vs.
- Electrical properties a strong function of surface passivation.
- Favorable band alignment found for some passivation and film growth conditions. Fermi level pinning (of interface defects?) appears not critical if film grown properly.
- Oxides of Ge and III-V's less stable thermally and electrically relative to SiO_2; can be consumed during high-K growth.
- Tendency of high-K to be partially reduced by Si substrate or gate not present for Ge and III-V's.
- Metallization materials and processes strongly affect interface chemistry and electrical properties.
- Sulfur passivation of semicond. surface helps in some systems.
- Si monolayers at interface appear helpful in minimizing defects.

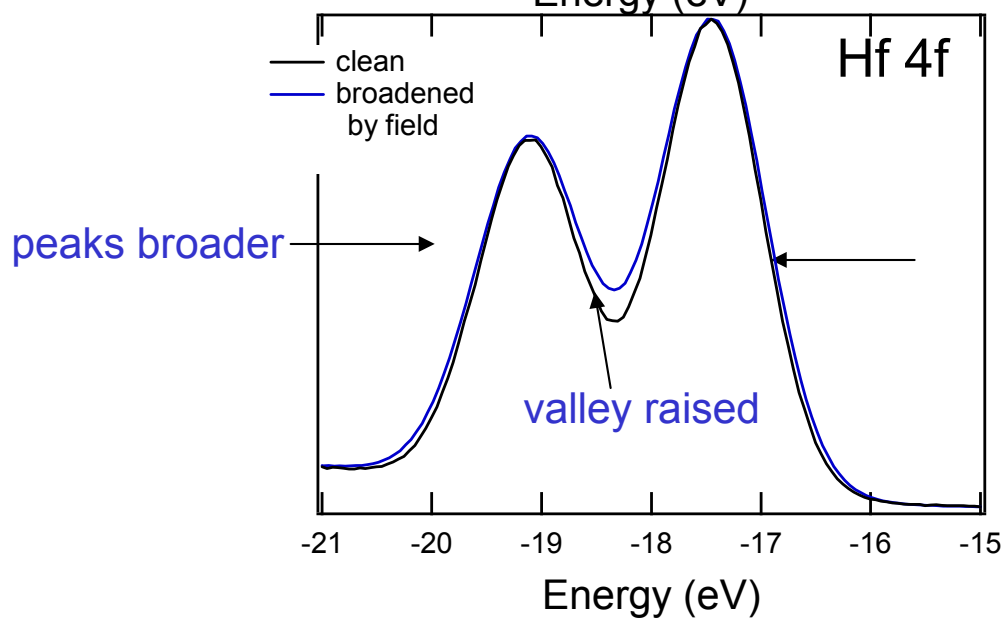
Simulation of core level broadening from ΔV across dielectric



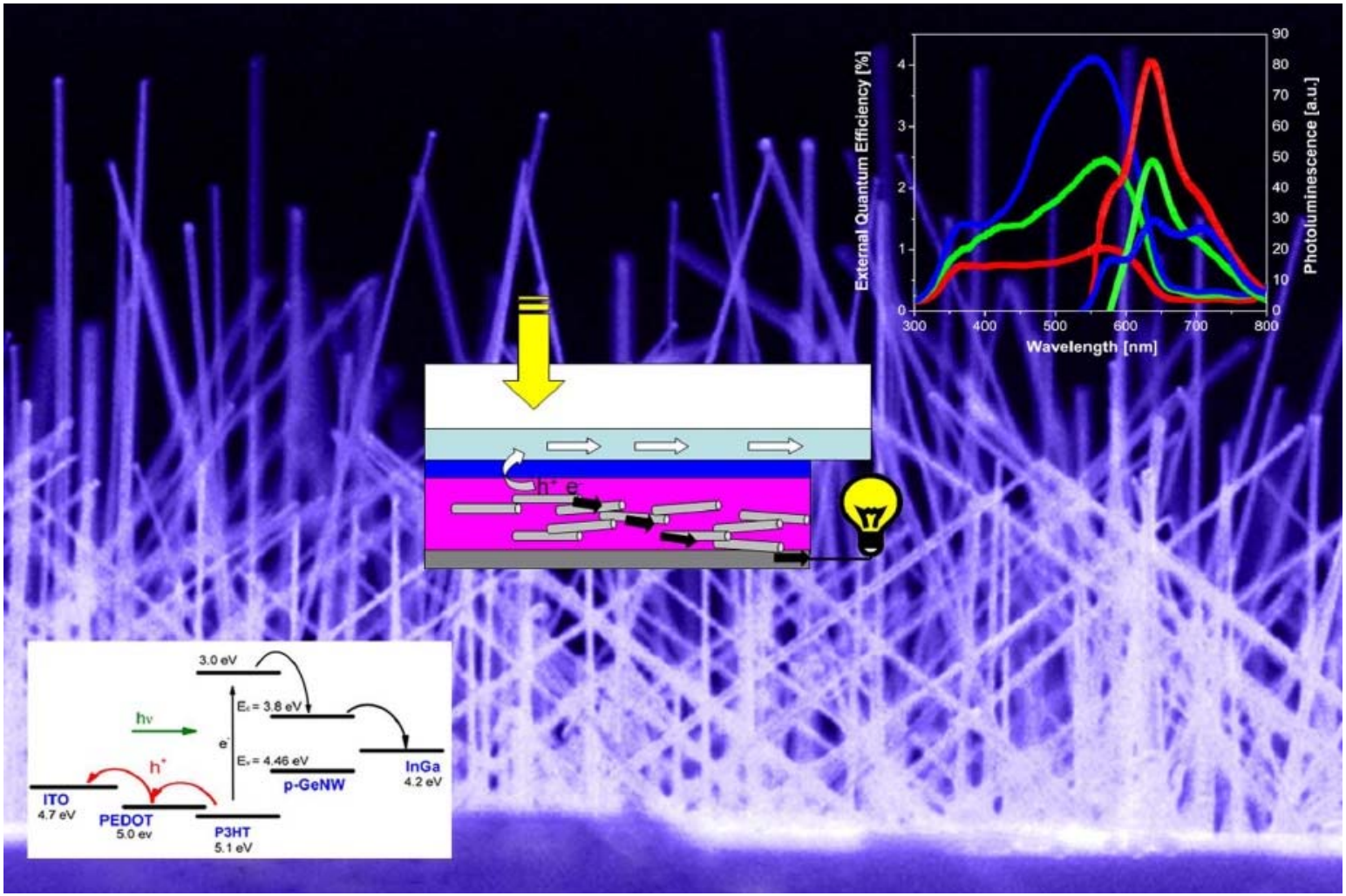
$$I = I_0 e^{\frac{-d}{\lambda}}$$

λ=20Å,
ΔV=0.5 eV,
d=30Å

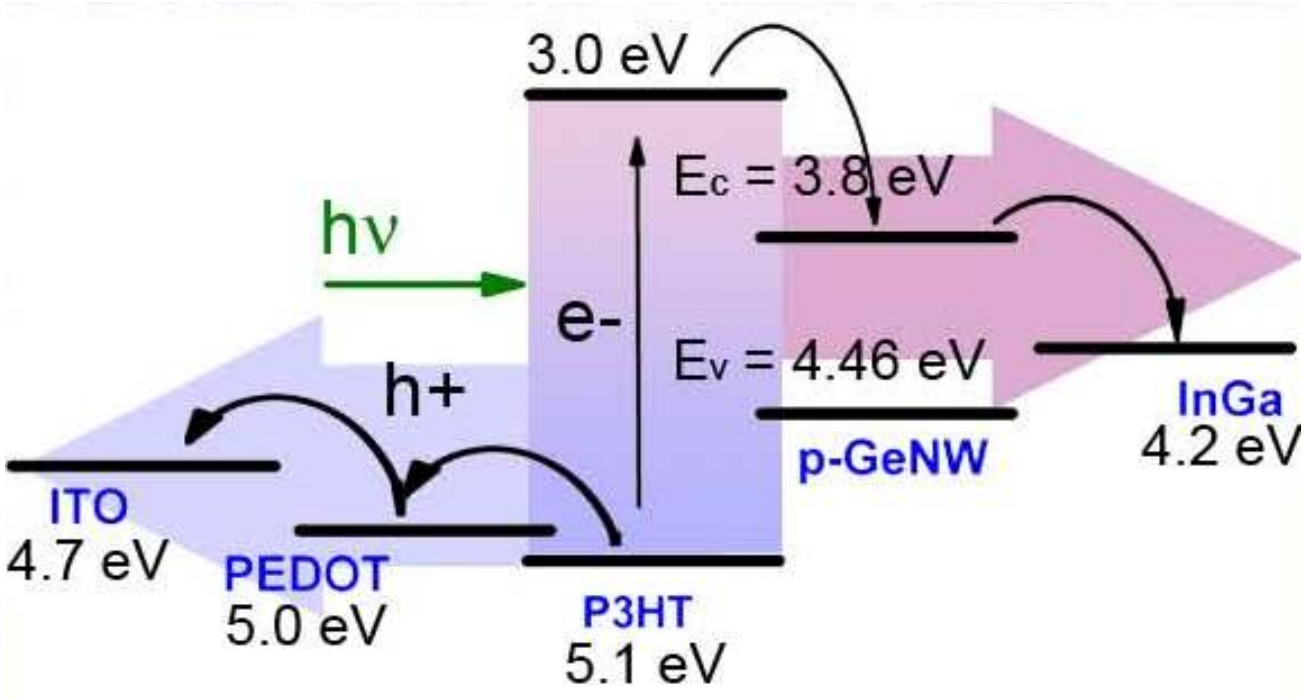


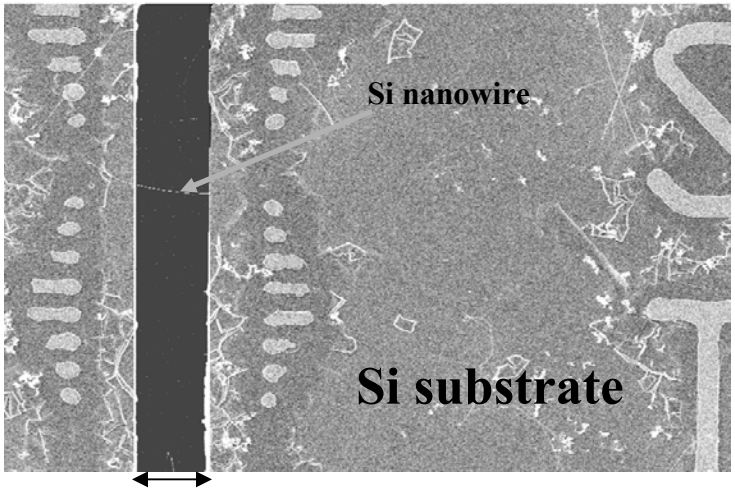


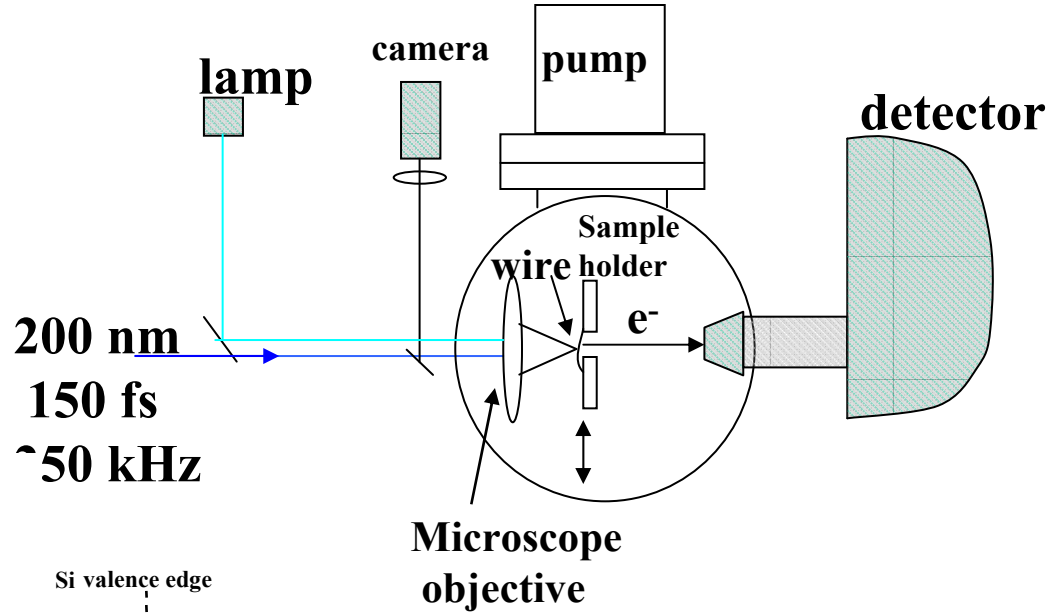
NW transistors and photovoltaics

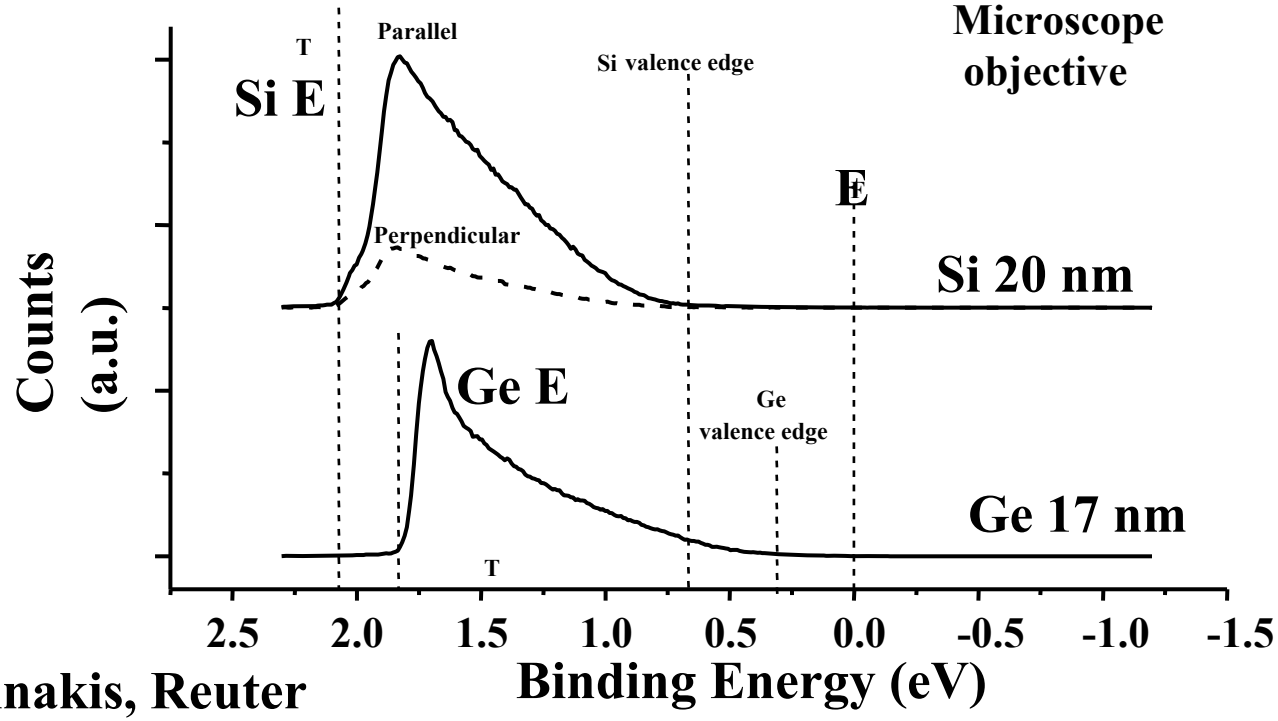


Interfaces in nanowire-enhanced photovoltaics: Rough approximation of band alignment





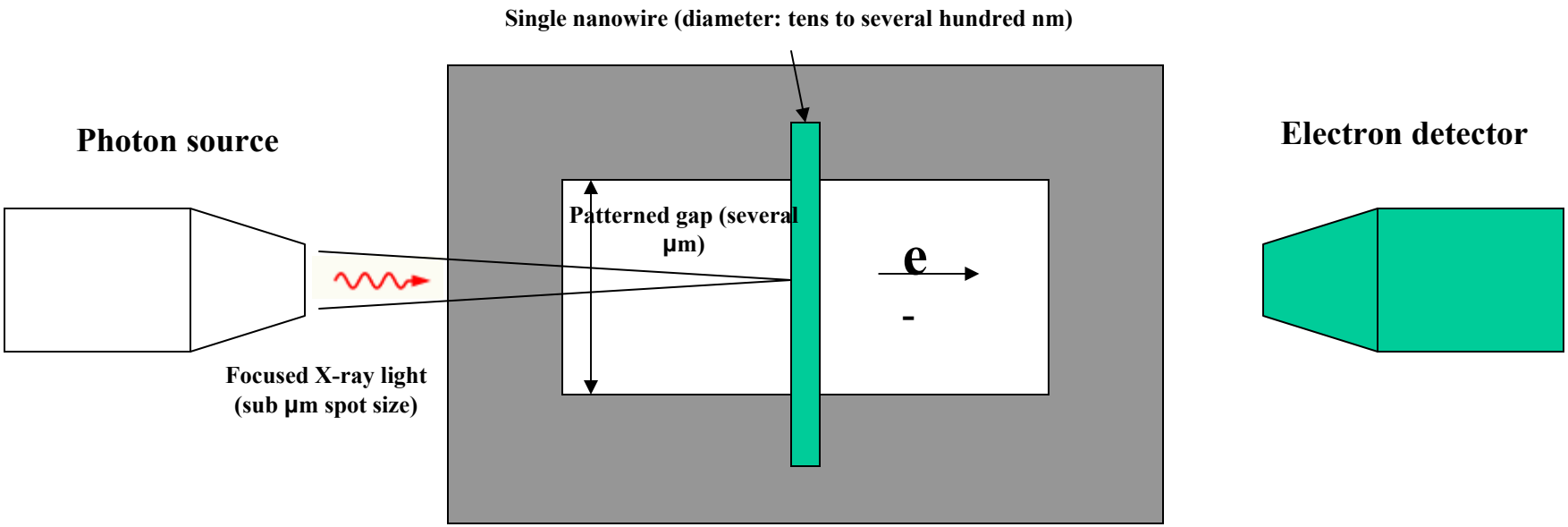




Haight, Sirinakis, Reuter
APL, 91, 233116 (2007)

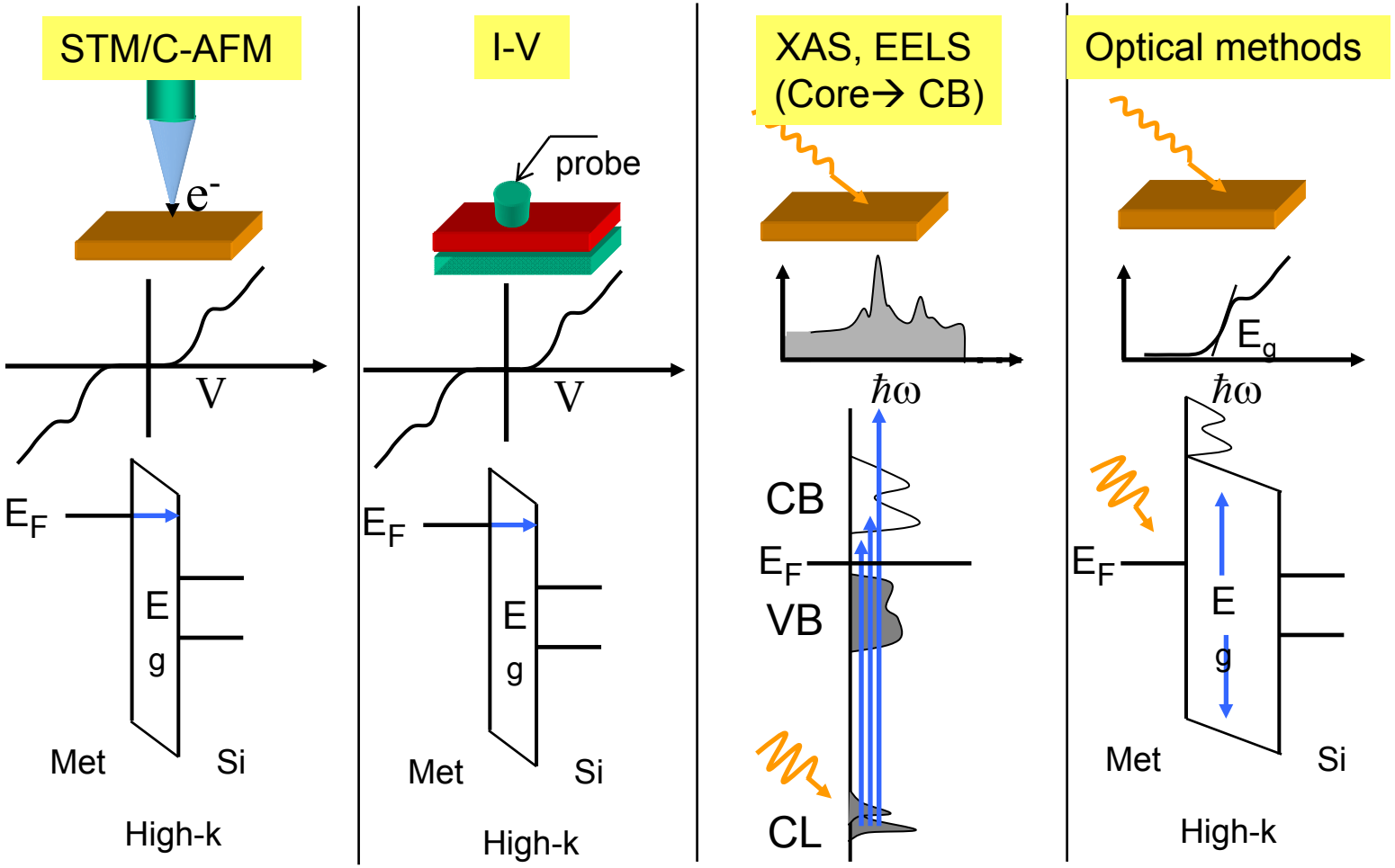
R. Haight, IBM

Photoemission of nanowire devices



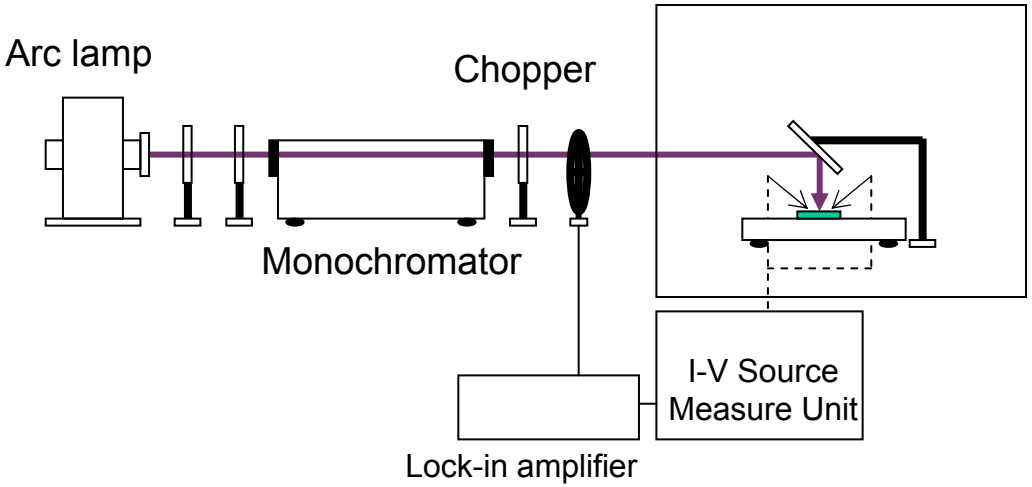
- Already demonstrated for low photon energies (R. Haight, IBM)
- Current X-ray optics and nanowire (NW) fabrication technology allow for single NW photoemission
- Allows for measurement of core-shell (gate stack analogs) structures in addition to intrinsic NW properties

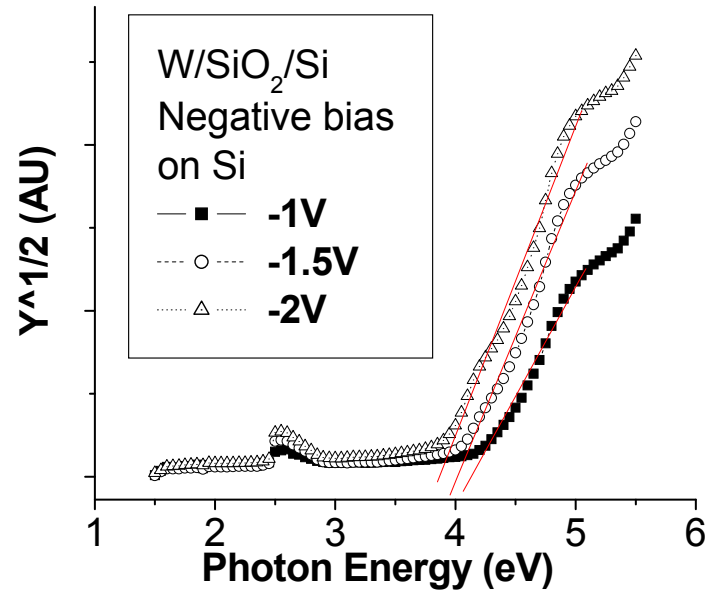
Additional spectroscopic tools

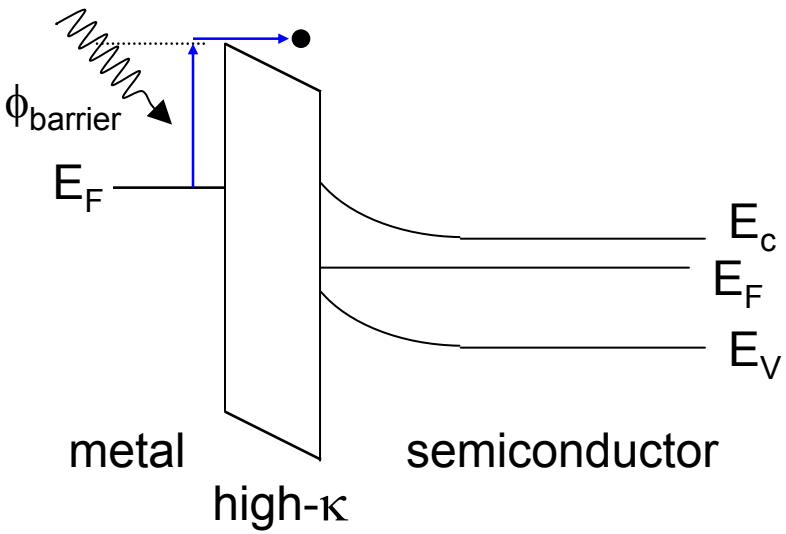


Also great new tools on market: new developments in TEM/STEM, atom probe tomography, He ion scattering, etc.

Internal photoemission (IntPES) for barrier height determination of buried interface



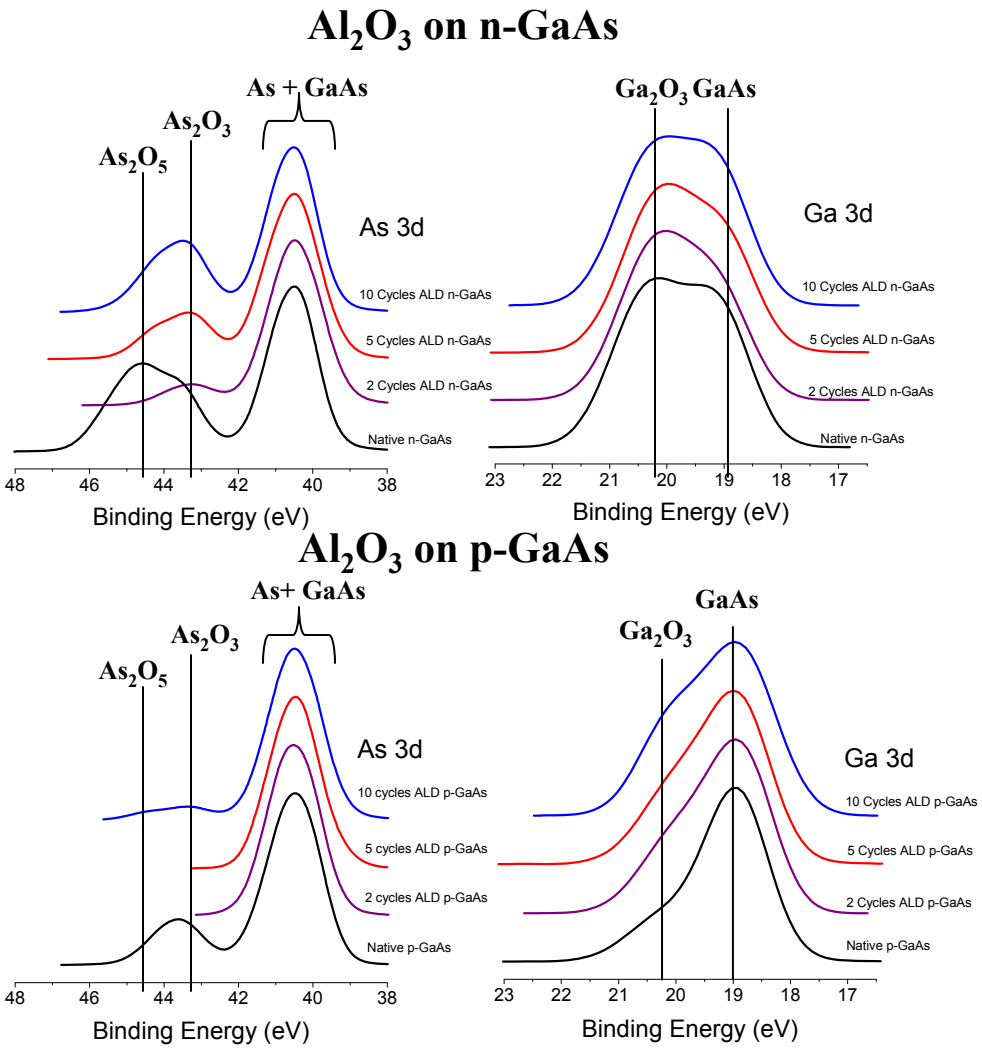




- Find threshold of $Y^{1/2}$ vs $h\upsilon$
- Extrapolate $h\upsilon_{threshold}$ to zero bias
- Determine barrier height

Interface chemistry of ALD growth

- Reduction of native oxides in first 2 cycles on both n-GaAs and p-GaAs
- Partial re-growth of As_2O_3 and Ga_2O_3 near interface during later cycles with regrowth more prevalent on n-GaAs than p-GaAs
- This behavior partially explains stronger pinning issues with ALD on n-GaAs



** Spectra normalized and aligned to emphasize chemistry (band bending removed)*