International Workshop for New Opportunities in Hard X-ray Photoelectron Spectroscopy: HAXPES 2009

Accelerating the next technology revolution

Understanding Chemical Interactions Between Thin Buried Layers of Microelectronic Materials in Advanced CMOS Structures

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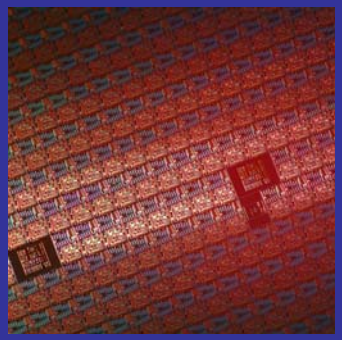

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Outline

- Intro – About SEMATECH
- High-*k*/Metal Gate Scaling Trends
- More than Moore - Novel Structures & New Materials
- **HAXPES Characterization – Practical Examples**
  - High-*k* Integration - VKE-XPS: $Si/SiO_x/HfO_2$
  - Dielectric Cap Layers: Higher-*k* & EWF Tuning
  - Disruptive Technology – Toward Zero IF
  - Flash Memory Retention - Impact of Intermixing

About SEMATECH…Global Consortium

SEMATECH Front End Processes (FEP) Division

Advanced Dielectrics & Electrodes for Logic & Memory

Advanced CMOS Scaling – Planar and Non-Planar

Electrical & Physical Characterization /Reliability & Metrology

Novel Emerging Technologies

SEMATECH Extensive R&D Network

- **University Network:** 80+ schools
- Examples: MIT, Stanford, Berkeley, UIUC, CMU, GATech, UT Austin
- Students completed (or completing) their PhD research: 27
- Co-authored papers = 180+
- Jointly arranged conferences, workshops = 9

National Lab Network:

- BNL Synchrotron XPS, XAS
- LANL Neutron SANS, SPEAR
- ORNL HR TEM
- ANL Ferroelectric, piezoelectric
- Sandia MEMS
- NIST FTIR,1/f Noise, XRD

Aus

Premier use

clean roo

R&D of

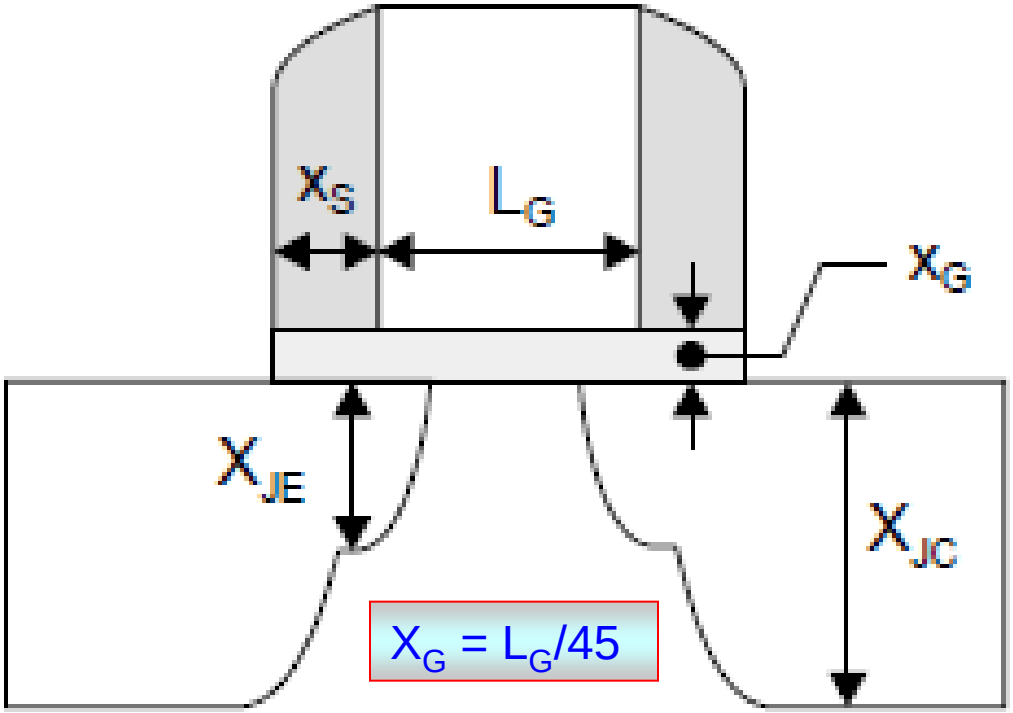
room

mm wafers

Highly Productive Collaborations w/NIST Scientists, Joe Woicik & Dan Fischer at NSLS/BNL

What's up with High-*k*?

When L_G scaled to 90nm, X_G =>2nm – 6-7 atomic layers SiO_2 -I_g



MOSFET control depends on the capacitance given by:

$$C = \frac{k\varepsilon A}{t}$$

where, *k* is the dielectric constant, A is the area and t is the thickness

equivalent oxide thickness (EOT) :

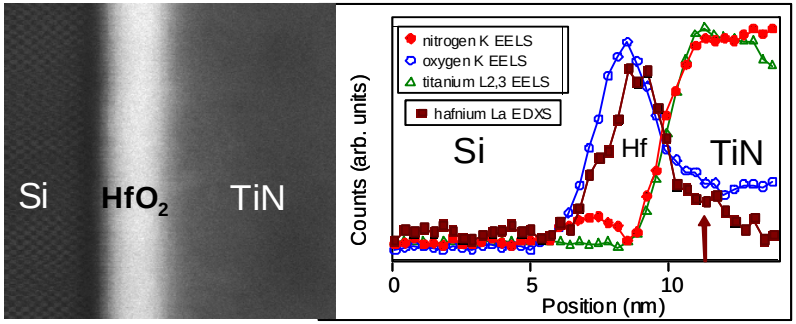
$$EOT = (k_{SiO2} / k_{HfO2}) t_{HfO2}$$

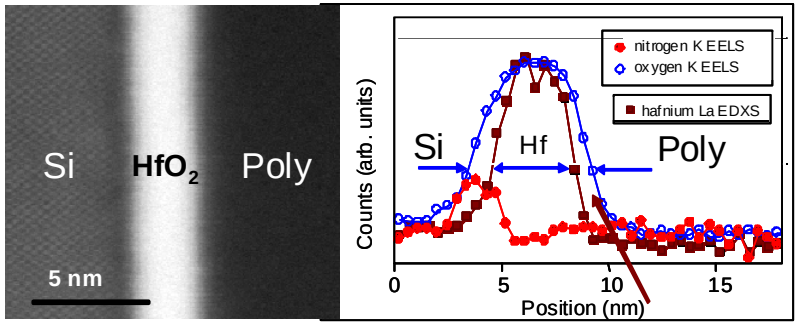
k_{SiO2} = 3.9, k_{HfO2} = 18-20

HfO_2 film 5x SiO_2 will provide same EOT with better leakage

Outline

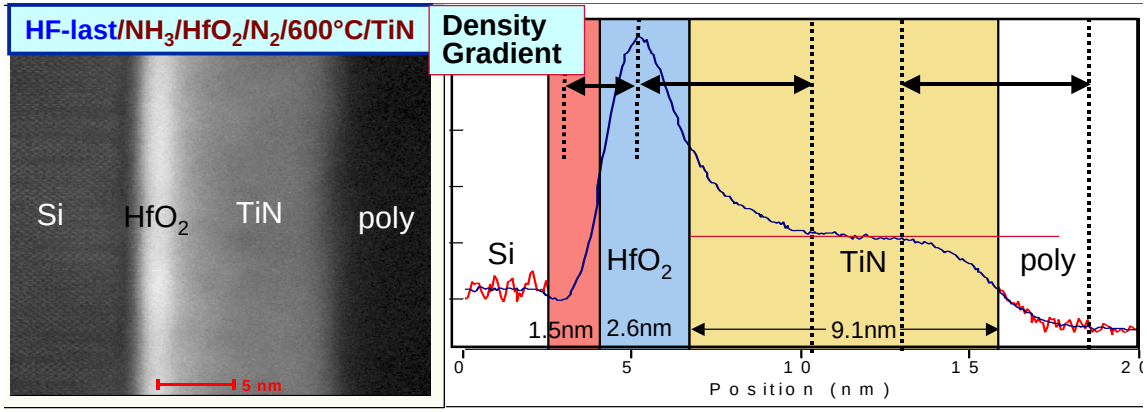
In the beginning there was Si/SiO_2/Poly-Si





TiN electrode facilitated scaling

Poly-Si produced thicker BIF and formed an additional low-k TIF



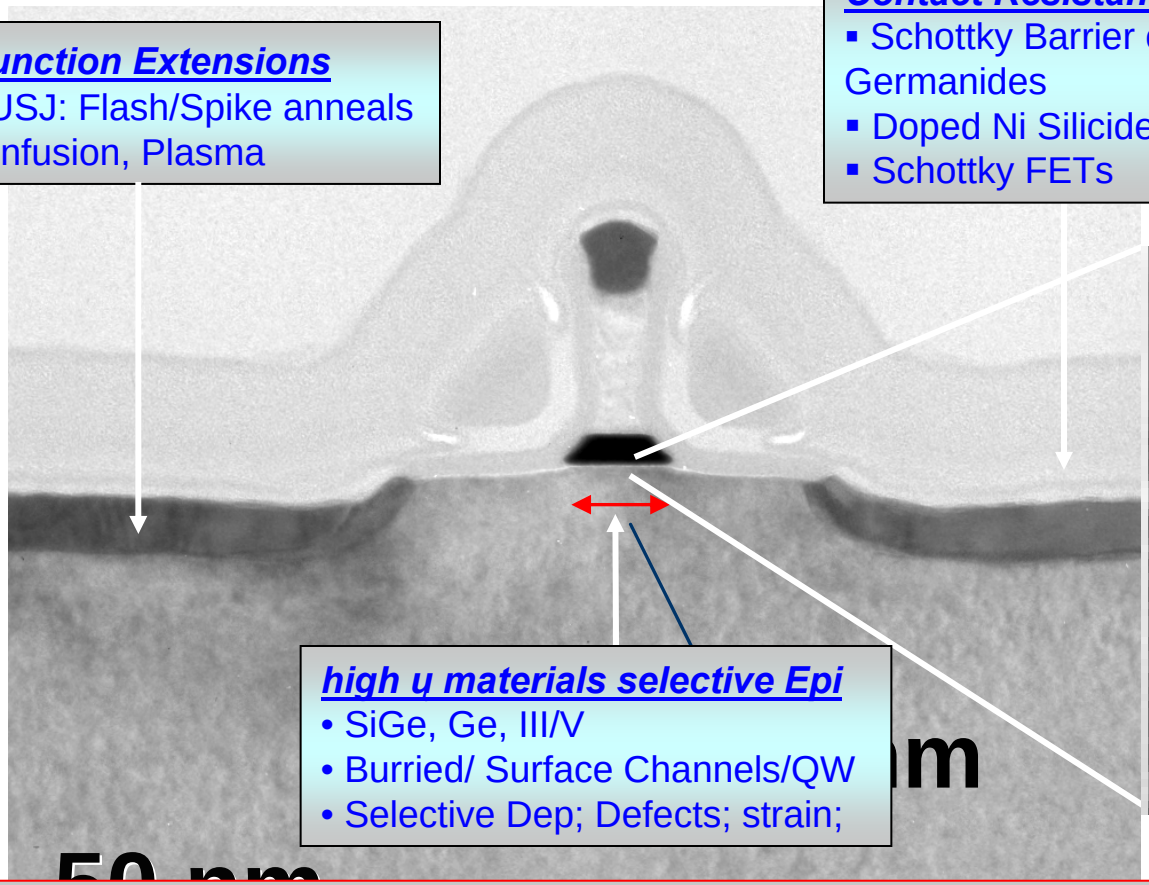
Hi-*k* deposition tools and clever processing tricks have yielded robust, stable films

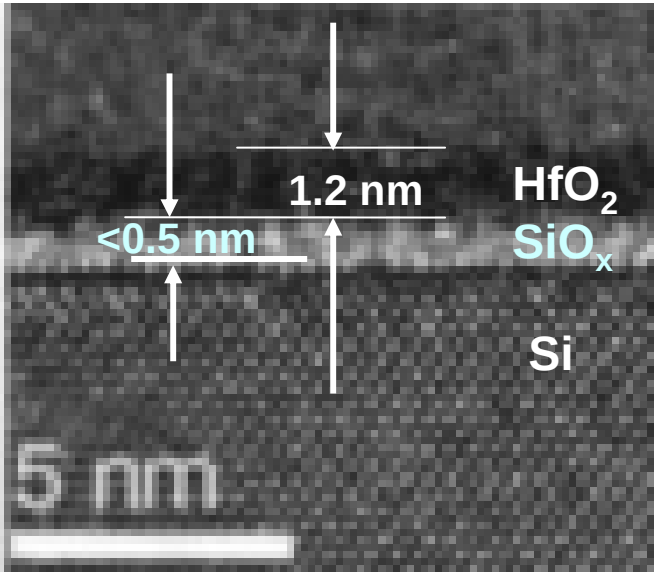
Planar CMOS Scaling:

Critical Modules

Junction Extensions
- USJ: Flash/Spike anneals
- Infusion, Plasma

Contact Resistance
- Schottky Barrier of Silicide / Germanides
- Doped Ni Silicide/Germanide
- Schottky FETs

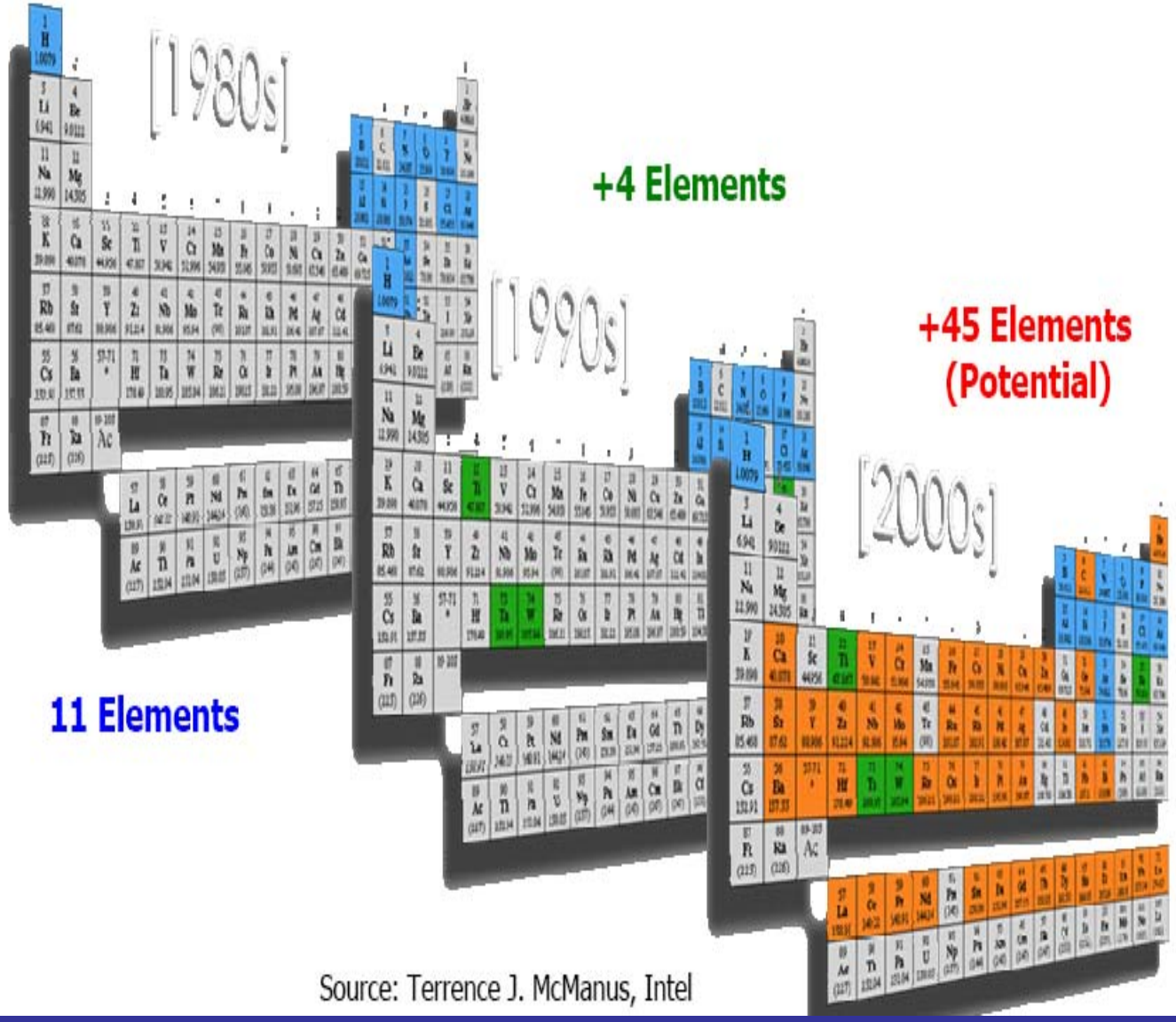




high μ materials selective Epi
- SiGe, Ge, III/V
- Burried/ Surface Channels/QW
- Selective Dep; Defects; strain;

Thermal stability: S/D activation to ~ 1000 ºC

CMOS Scaling Enabled by New Materials and/or Architecture

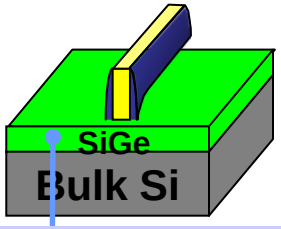


Source: Terrence J. McManus, Intel

Materials & Device Roadmap - Logic

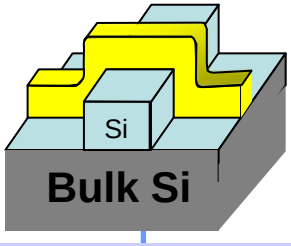
High-k / Metal Gate

Hi Mobility Channel



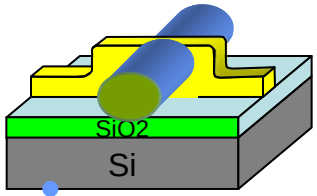
Characterization Issues:
- SiGe-HK Interface
- Damage at p-n in SiGe
- Strain in channel

FinFET

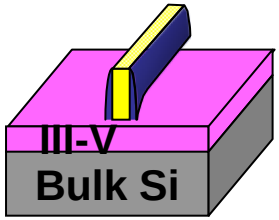


Characterization Issues:
- Sidewall S/D doping
- Sidewall silicidation
- Sidewall etch

Nanowires



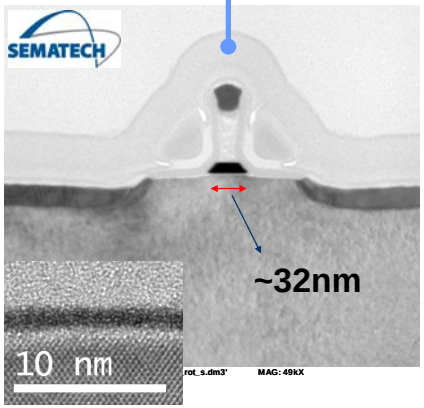
III-V

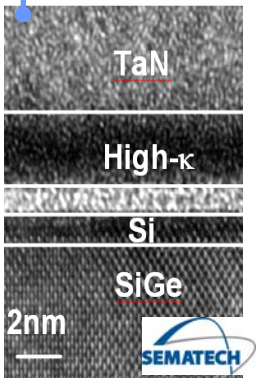


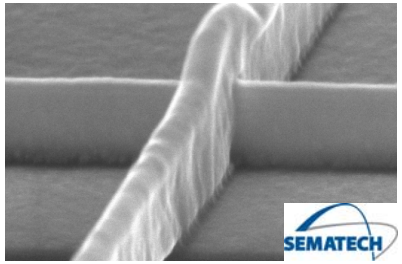
Characterization Issues:
- strain, E_g for III-V on Si
- III-V – HK interface
- Doping

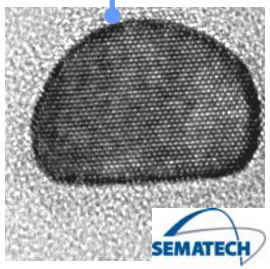
Many options!

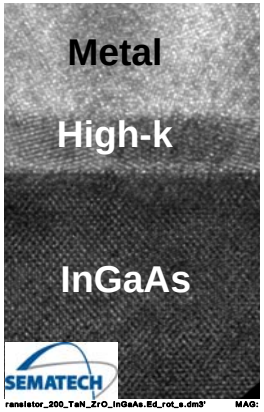
2009 | 2011 | 2013 | 2015 | 2017 | 2019







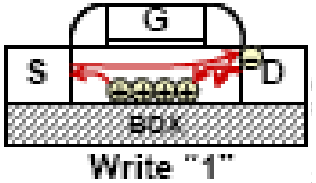




Materials & Device Roadmap -Memory

DRAM

SMSG 2008 IEDM

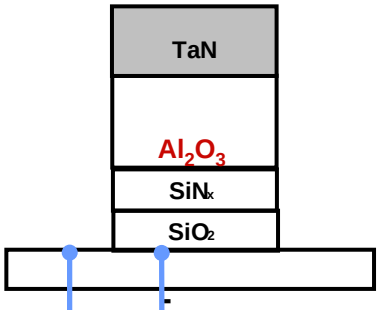


1T1C Issues:
- HK/MG interface
- HK/MG crystal

1T Issues:
- Charge storage
- Etch damage
- Junction quality

SiN Trap Flash

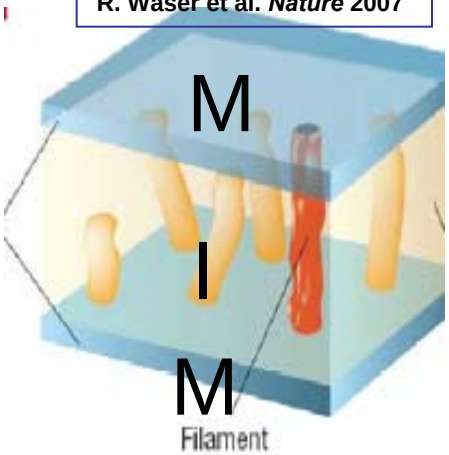
Metal Nanocrystal Flash



Characterization Issues:
- traps, defects in Al2O3
- Storage node: SiN -> metal NC
- High work function metal

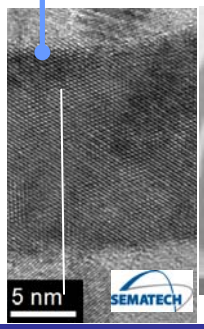
RRAM

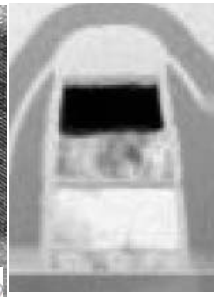
R. Waser et al. *Nature* 2007

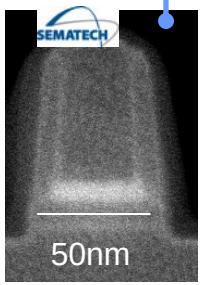


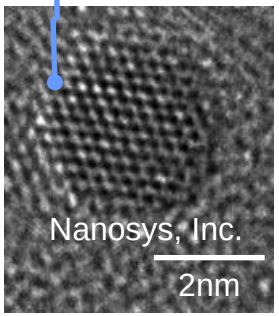
Characterization Issues:
- Conduction mechanism
- Oxygen Vacancies
- NiO, TiO, WO, TaO

2009 | 2011 | 2013 | 2015 | 2017 | 2019









Many options:
- Resistance Change
- Molecular
- Spin Torque

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  - High-*k* Integration - VKE-XPS: $Si/SiO_x/HfO_2$
  - Dielectric Cap Layers: Higher-*k* & EWF Tuning
  - Disruptive Technology – Toward Zero IF
  - Flash Memory Retention - Impact of Intermixing

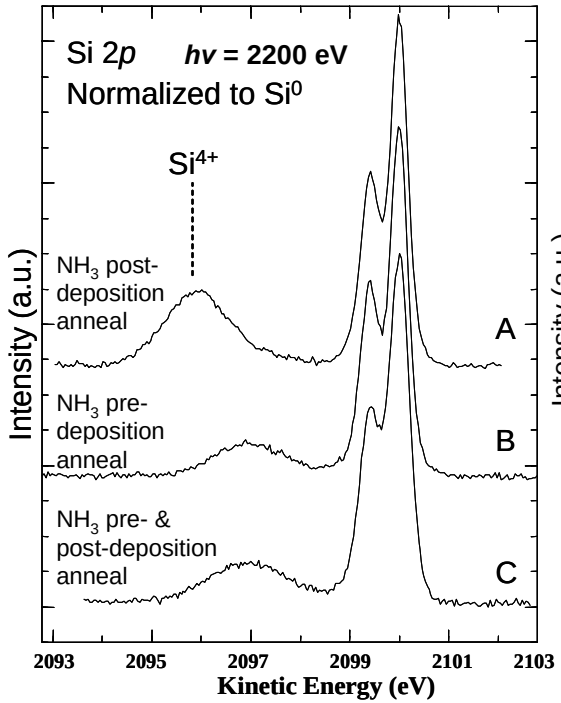
Influence of NH_3 on $HfO_2/SiO_2/Si(100)$

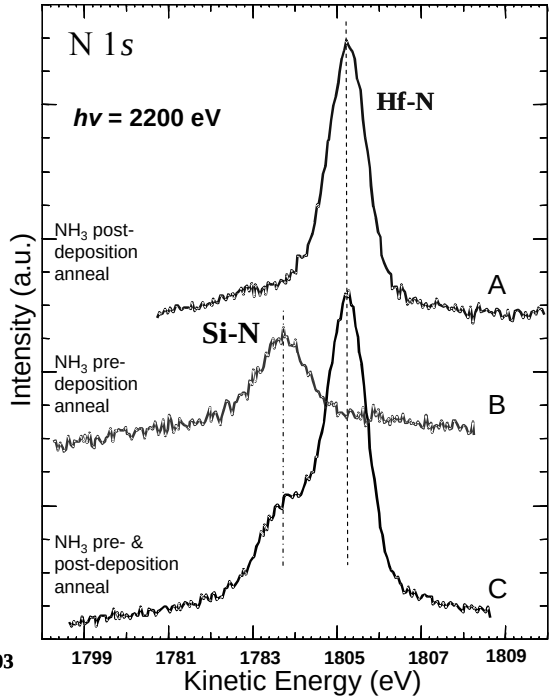
@ NIST Beamline X24A (NSLS/BNL)

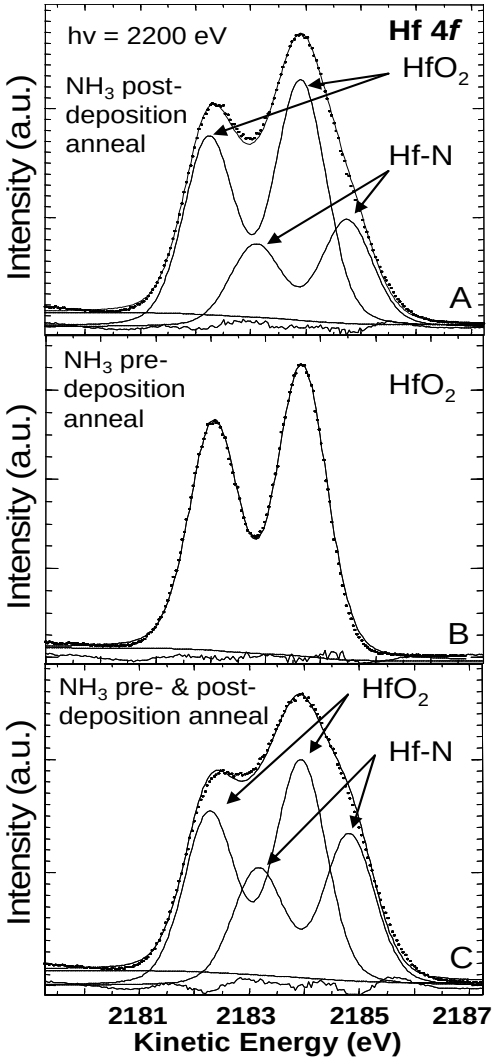
NH_3 Pre-DA strongly influences interface Si coordination (samples B & C)

NH_3 PDA strongly influences Hf coordination (samples A & C)

Sample	Interface	Pre Deposition Anneal	High-k Deposition	Post Deposition Anneal
A	ISSG 2 nm	None	HfO_2	NH_3 / PDA
B	HF - last	NH_3 / Pre-DA	HfO_2	None
C	HF - last	NH_3 / Pre-DA	HfO_2	NH_3 / PDA





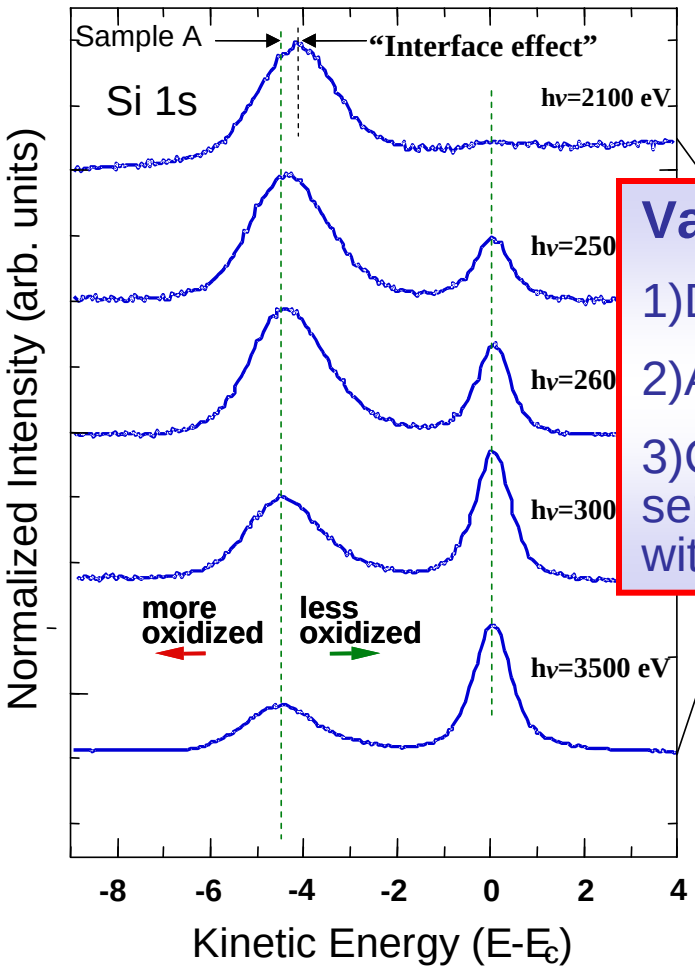


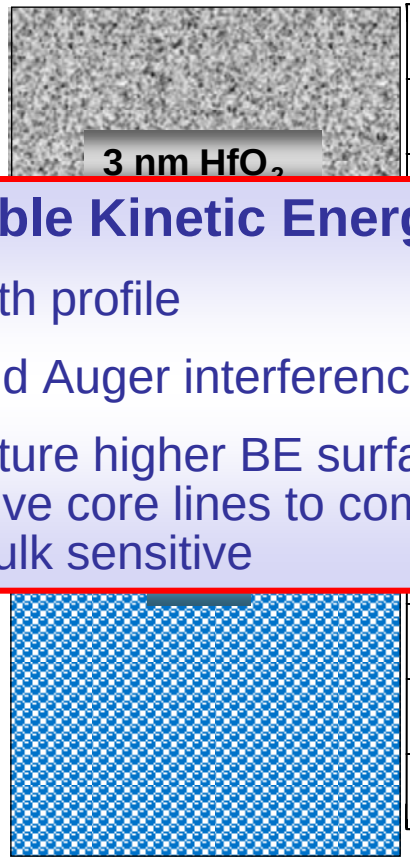
HAXPES: VKE-XPS Depth Profiling

@ NIST Beamline X24A (NSLS/BNL)

Variable Kinetic Energy-XPS: Si 1s BE as f(depth) through the IF

Hf 4f B.E. constant surface & interface, Oxygen deficient Si, at the SiO_2/HfO_2 IF



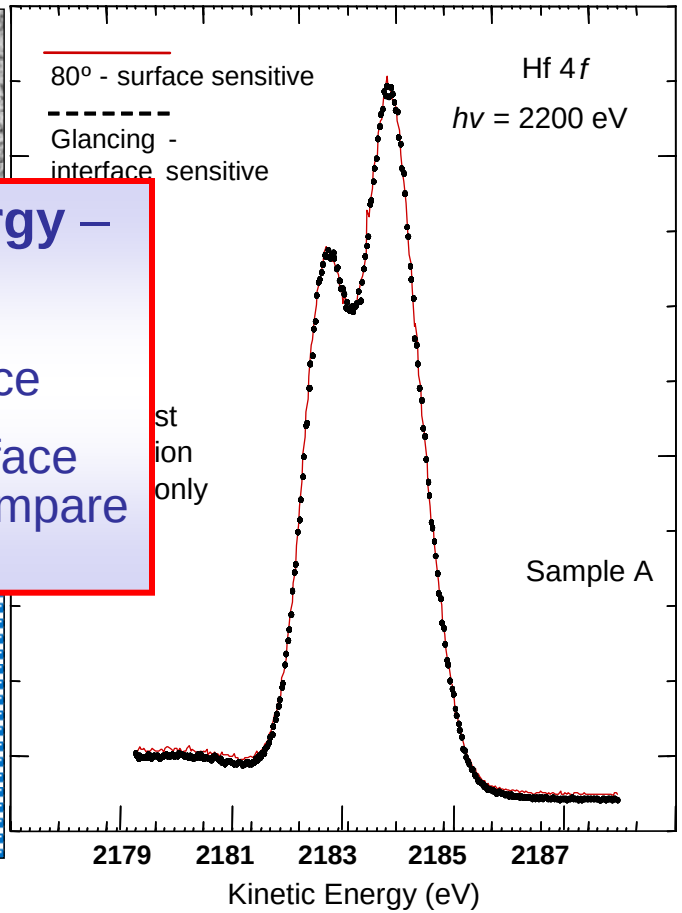


Variable Kinetic Energy –

1) Depth profile

2) Avoid Auger interference

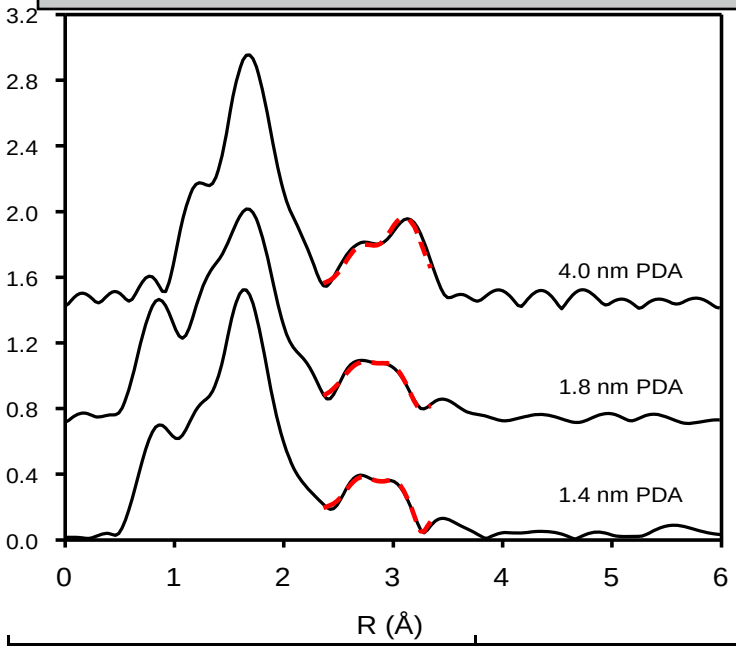
3) Capture higher BE surface sensitive core lines to compare with bulk sensitive

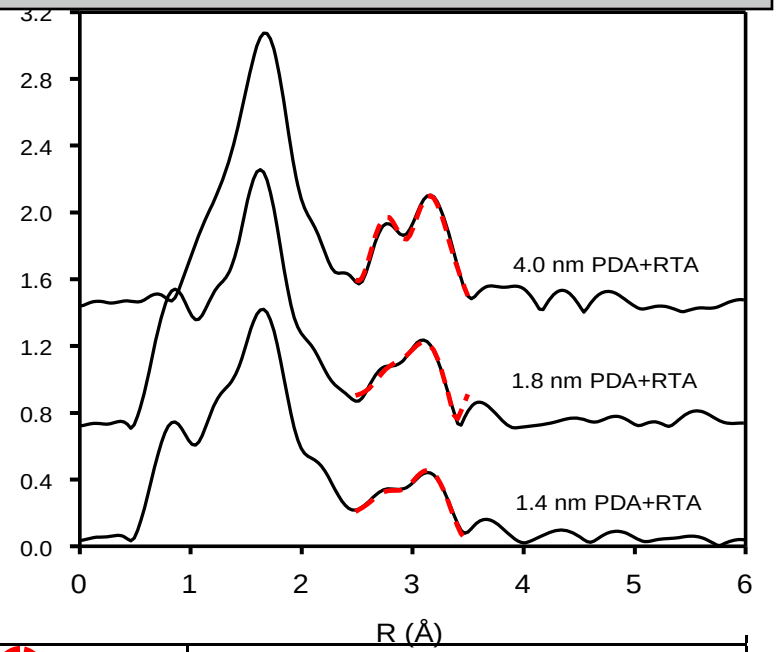


P. S. Lysaght, J. C. Woicik, D. A. Fischer, G. I. Bersuker, H-H. Tseng, and R. Jammy, *J. Appl. Phys*. 101, 024105 (2007).

EXAFS: Characterizing HfO_2 crystalline phase

Critical grain size (~ 4 nm) for t- to m- transformation, below which the t- phase is retained at temperatures sufficient to produce m-HfO_2 in slightly thicker films with slightly larger grains.

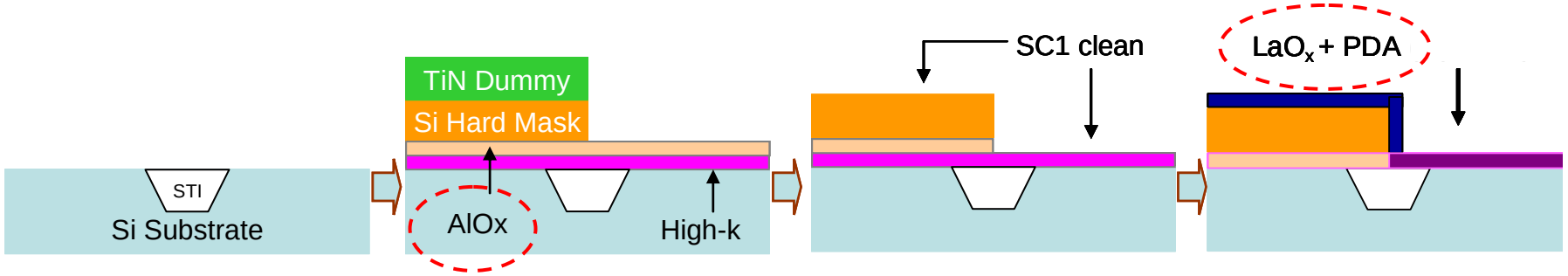


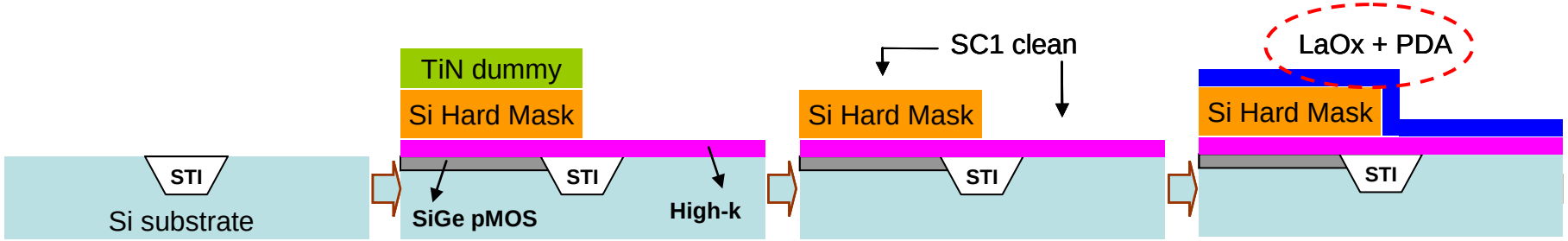


	Monoclinic	Tetragonal	Orthorhombic
1.4 nm PDA	0.00	0.96	0.04
1.8 nm PDA	0.00	0.99	0.01
4.0 nm PDA	0.67	0.33	0.00
1.4 nm PDA+RTA	0.57	0.43	0.00
1.8 nm PDA+RTA	0.60	0.40	0.00
4.0 nm PDA+RTA	0.96	0.04	0.00

***t*-HfO_2 (*k* = 28-29), *m*-HfO_2 (*k* = 16-18)**

Single channel dual cap or
Dual Channel (SiGe pFET) Single Cap (LaOx) Integration



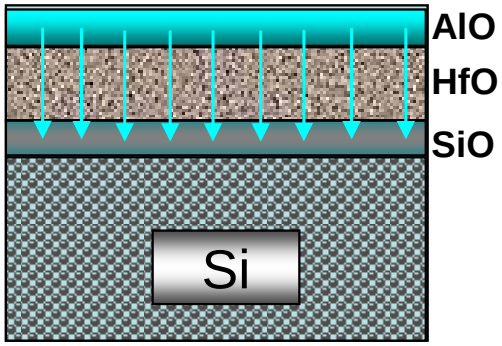


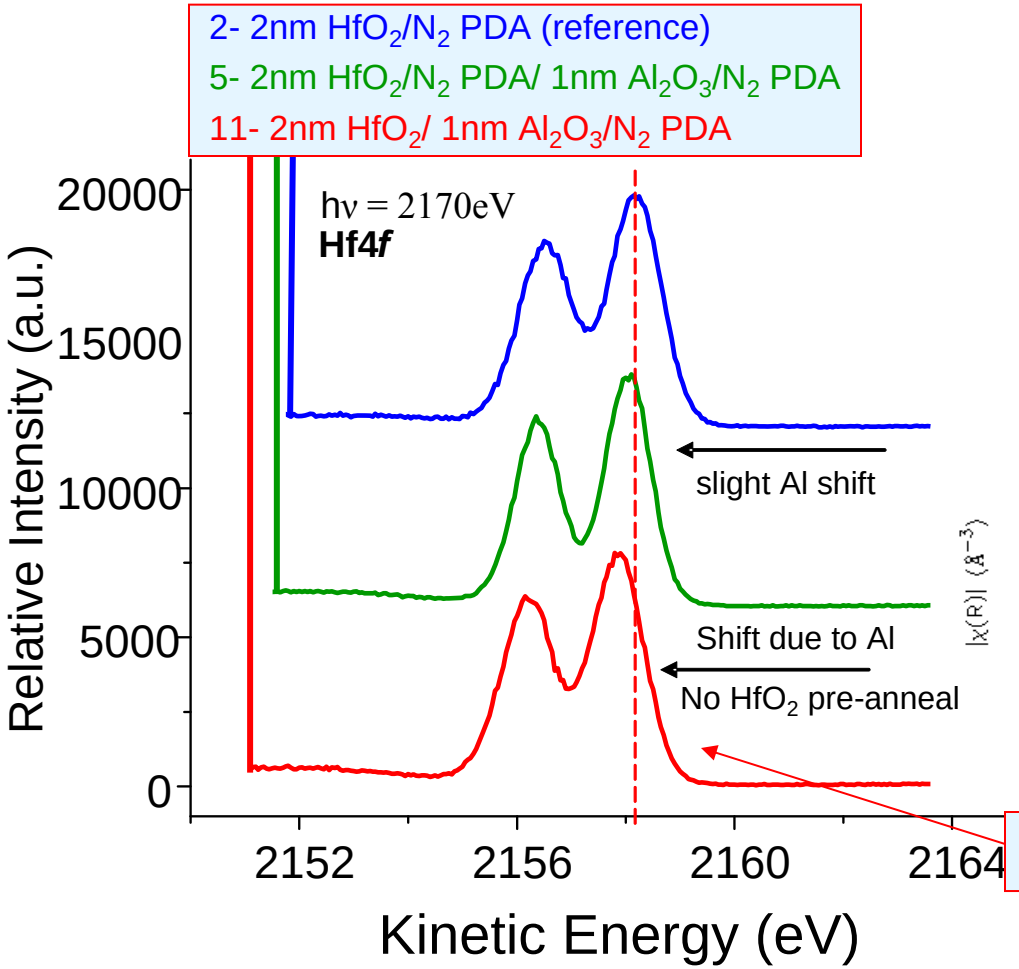
AlOx or SiGe for pFET and LaOx for nFET

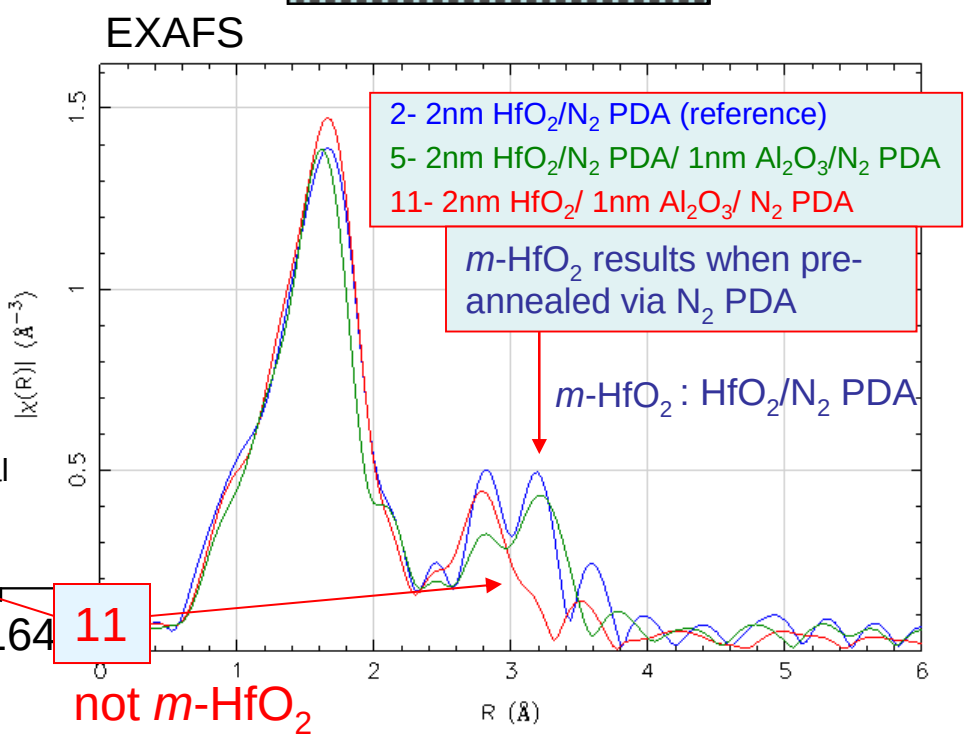
XPS & EXAFS: AlO Cap Layer Spectra

Hf 4*f* & Hf L_3 edge - N_2 Interactions

N_2 PDA forms stable *m*-HfO_2 – wrt Al diffusion



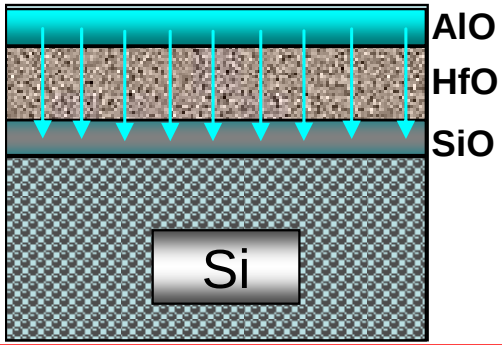


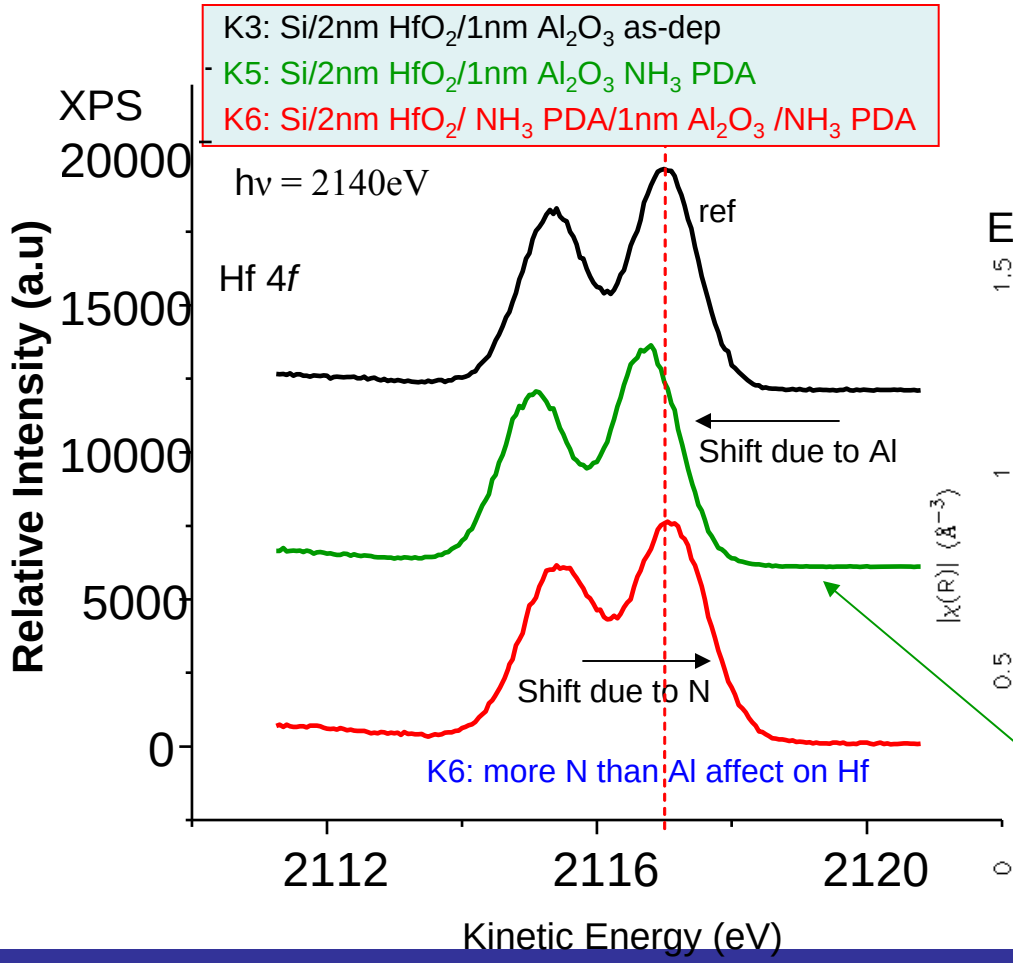


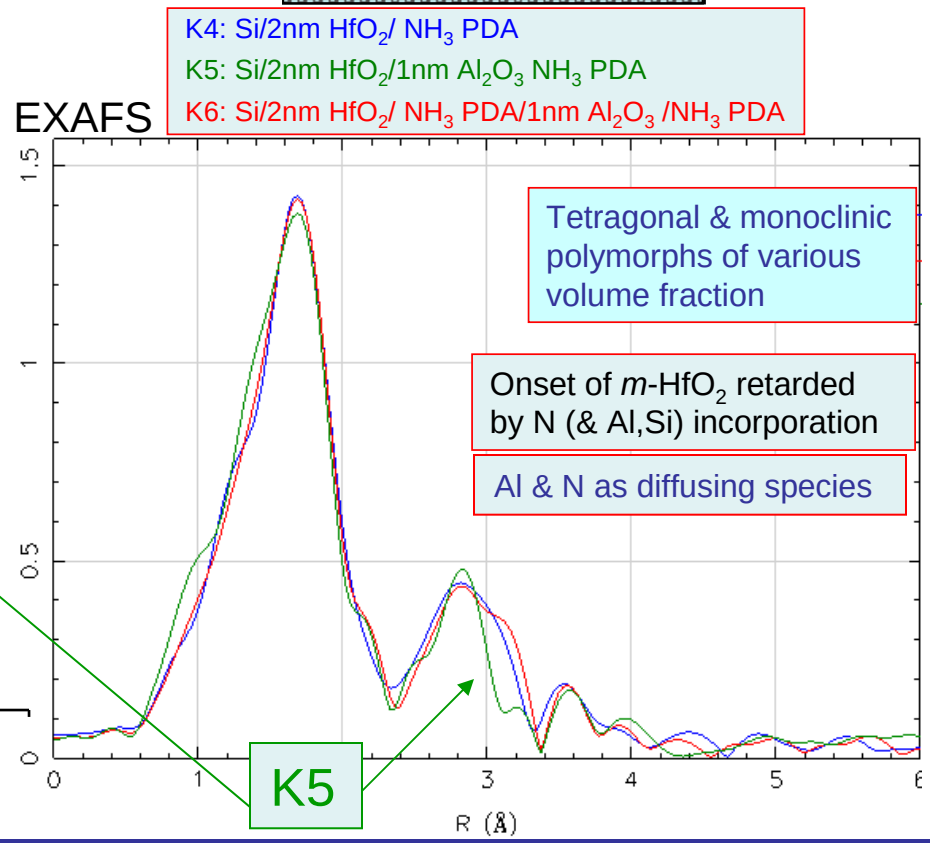
XPS & EXAFS: AlO Cap Layer Spectra

Hf 4*f* & Hf L_3 edge - NH_3 Interactions

K5: HfAlO – XPS Hf 4*f* and EXAFS Hf L_3 look like Hf silicate
K6: More N than Al incorporation in HfO_2





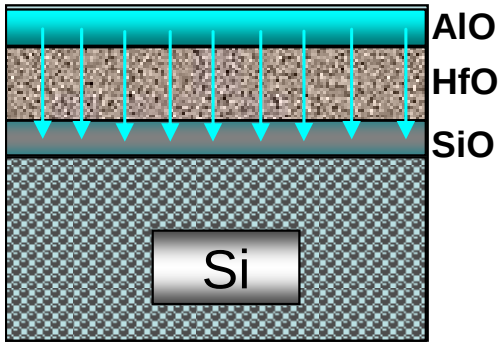


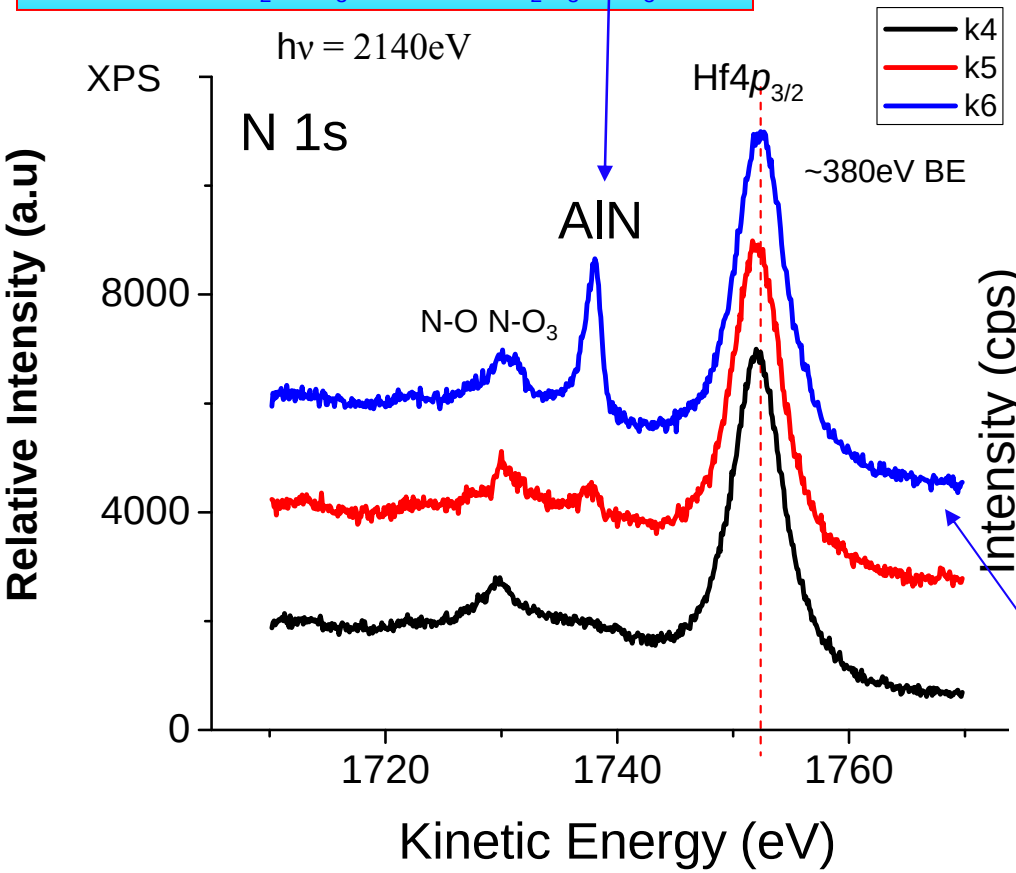
XPS & XAS: AlO Cap Layer Spectra

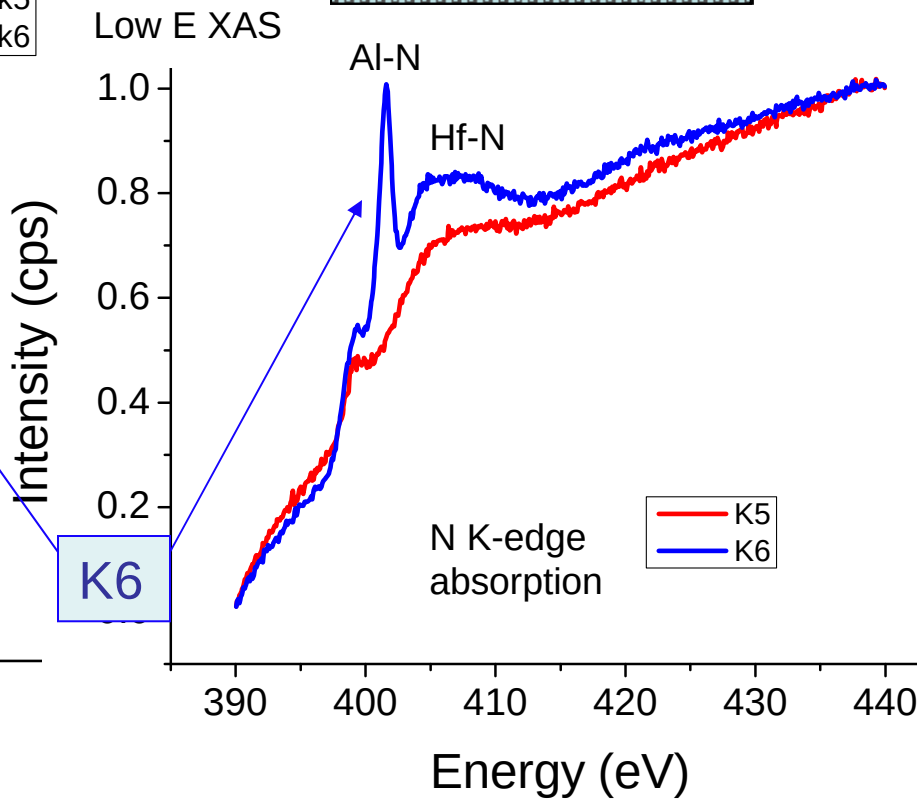
N 1s & N K_1 edge - NH_3 Interactions

Al cap more easily etched if HfO_2 is pre-annealed

K4: Si/2nm HfO_2/1nm Al_2O_3 as-dep
K5: Si/2nm HfO_2/1nm Al_2O_3 NH_3 PDA
K6: Si/2nm HfO_2/ NH_3 PDA/1nm Al_2O_3 /NH_3 PDA





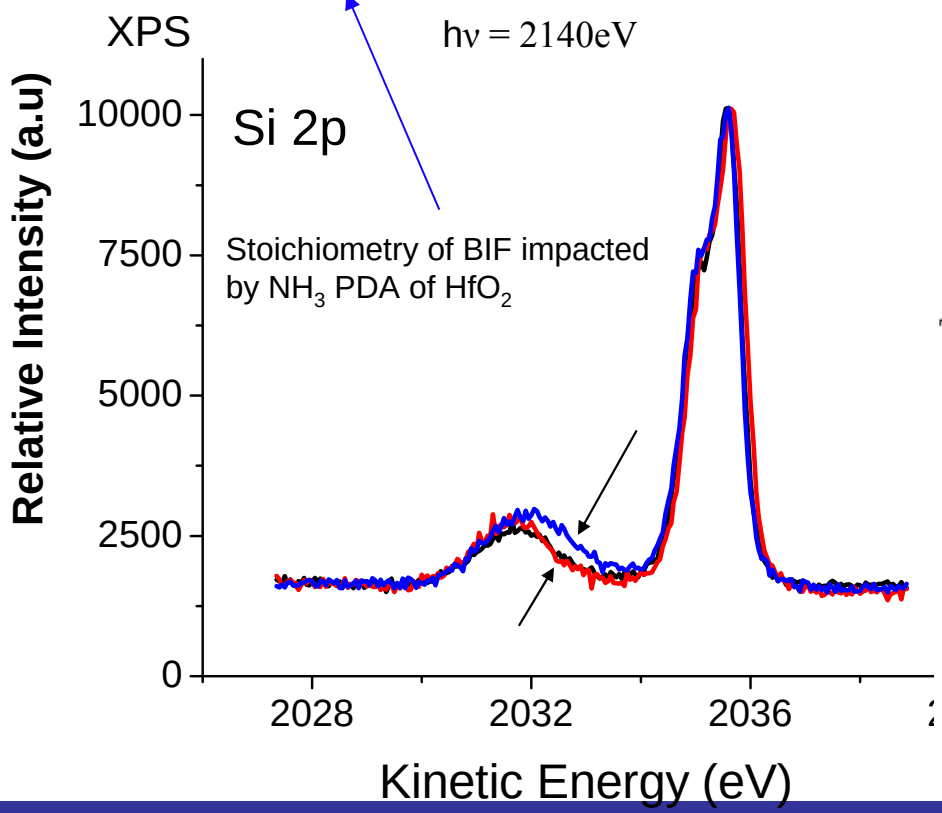


XPS & EXAFS: AlO Cap Layer Spectra

Si 2*p* & Hf L_3 edge - NH_3 Interactions

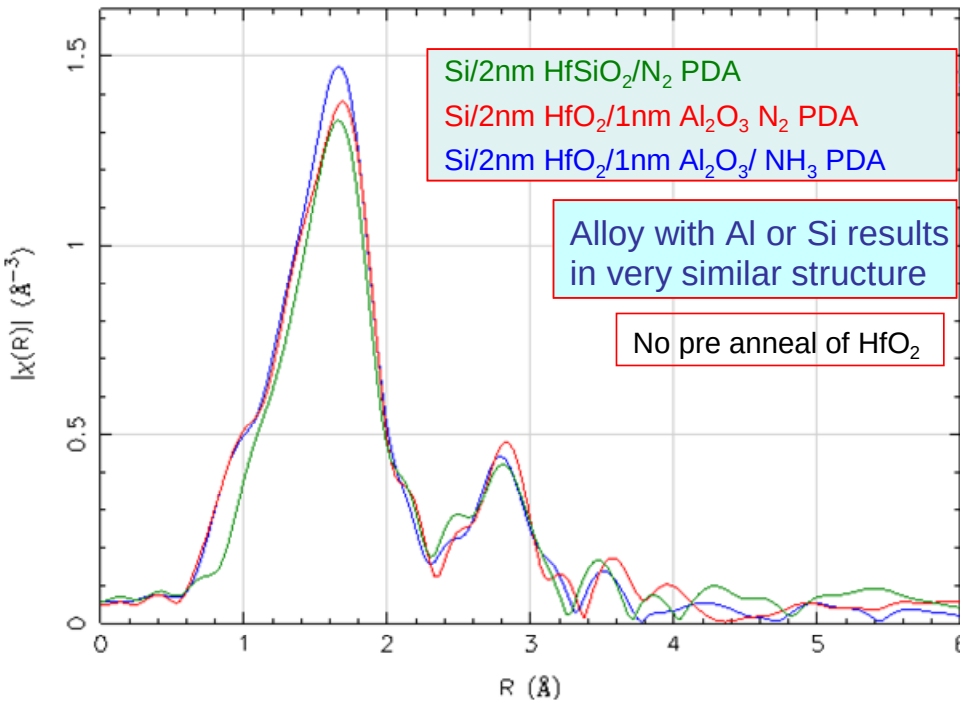
Impact of NH_3 PDA on Si/SiO BIF

K4: Si/2nm HfO_2/1nm Al_2O_3 as-dep
K5: Si/2nm HfO_2/1nm Al_2O_3 NH_3 PDA
K6: Si/2nm HfO_2/ NH_3 PDA/1nm Al_2O_3 /NH_3 PDA



Impact of No HfO_2 PDA => HfAlO

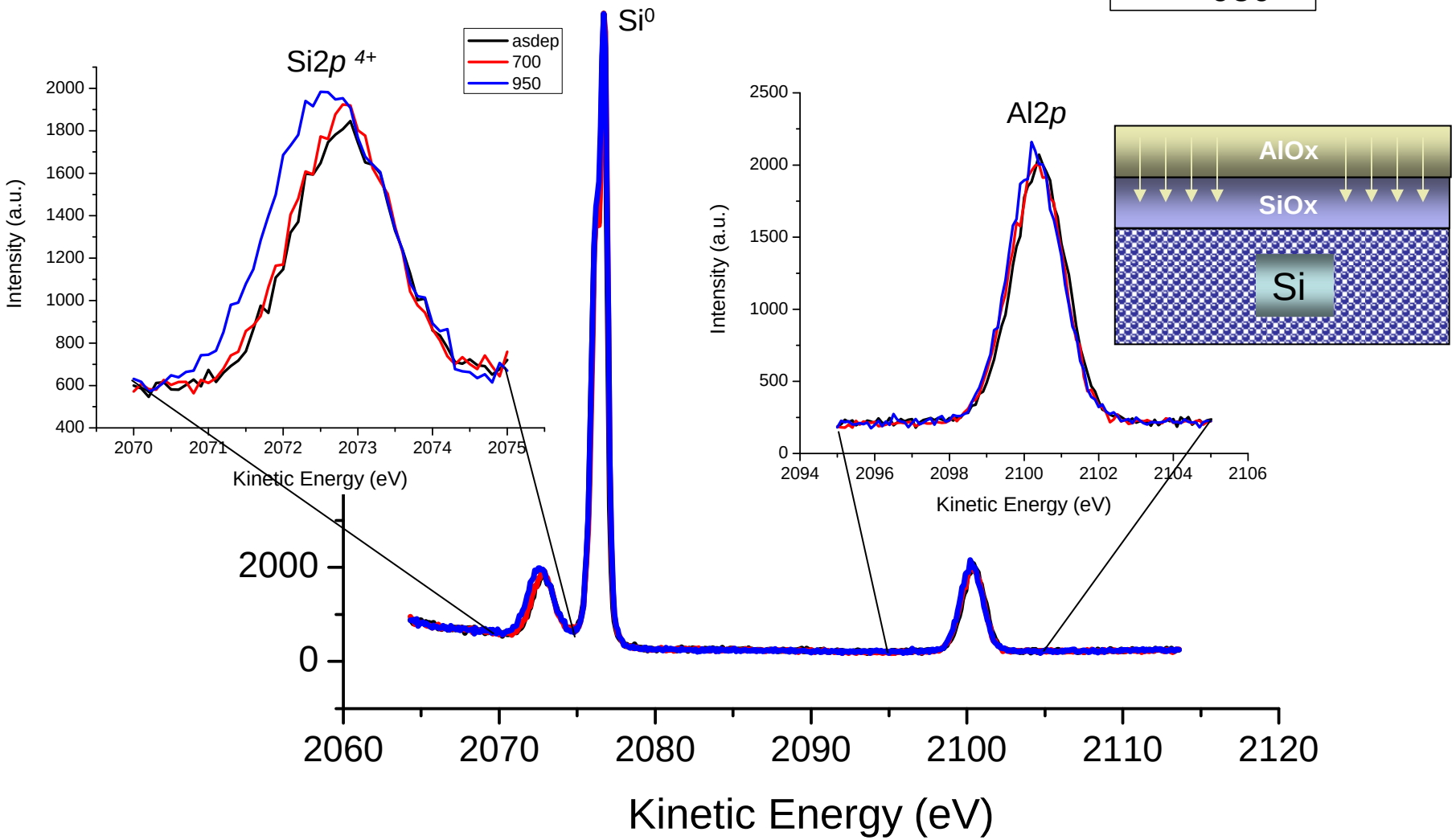
No pre-anneal of HfO_2 –
Al incorporation alloys HfO_2 => HfSiO-like
very similar for N_2 and NH_3 PDA



AlOx/SiOx Intermixing

1nm AlO/1nm chem ox/Si

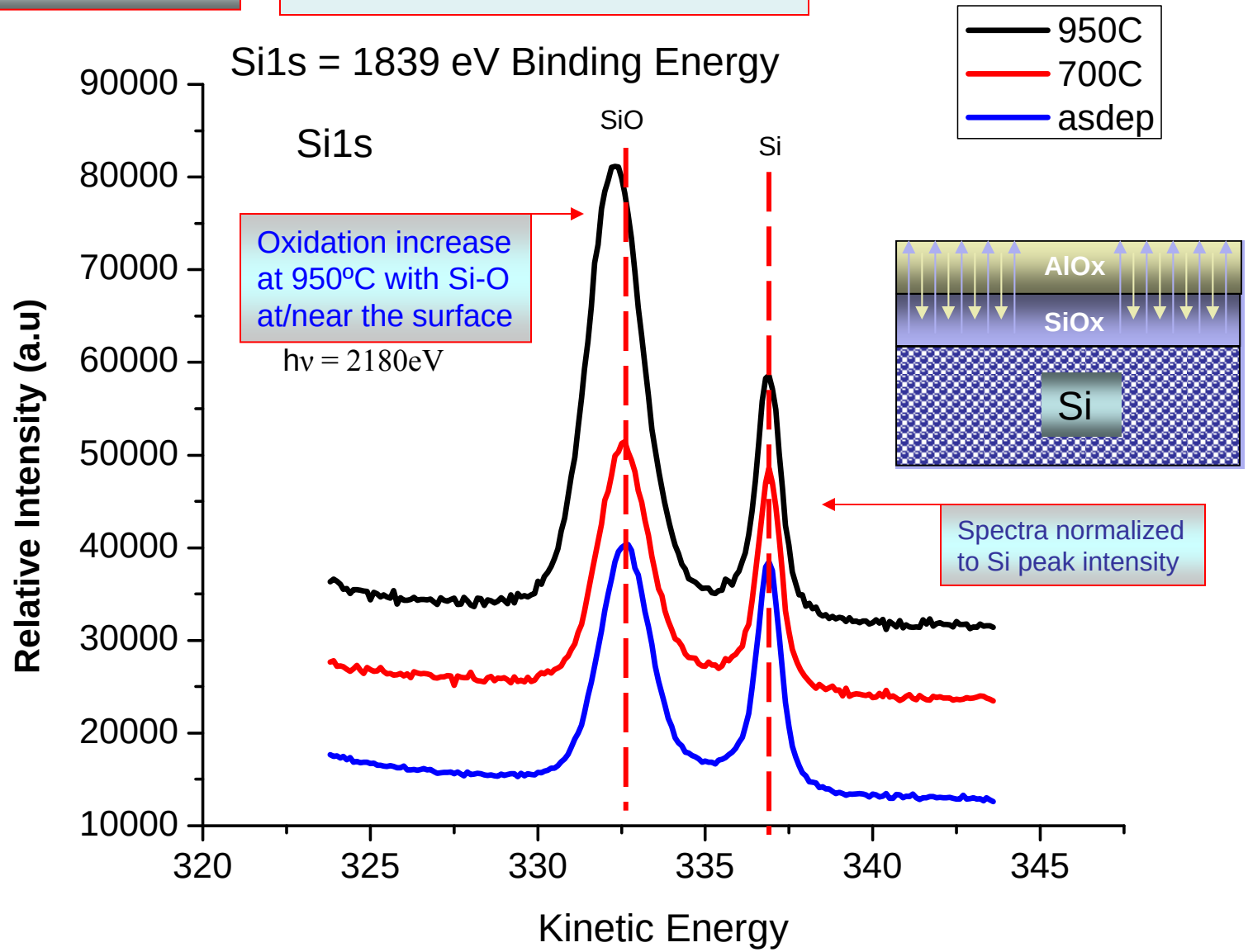
Shallow cores normalized to Si^0, intensity & energy



AlOx/SiOx Intermixing

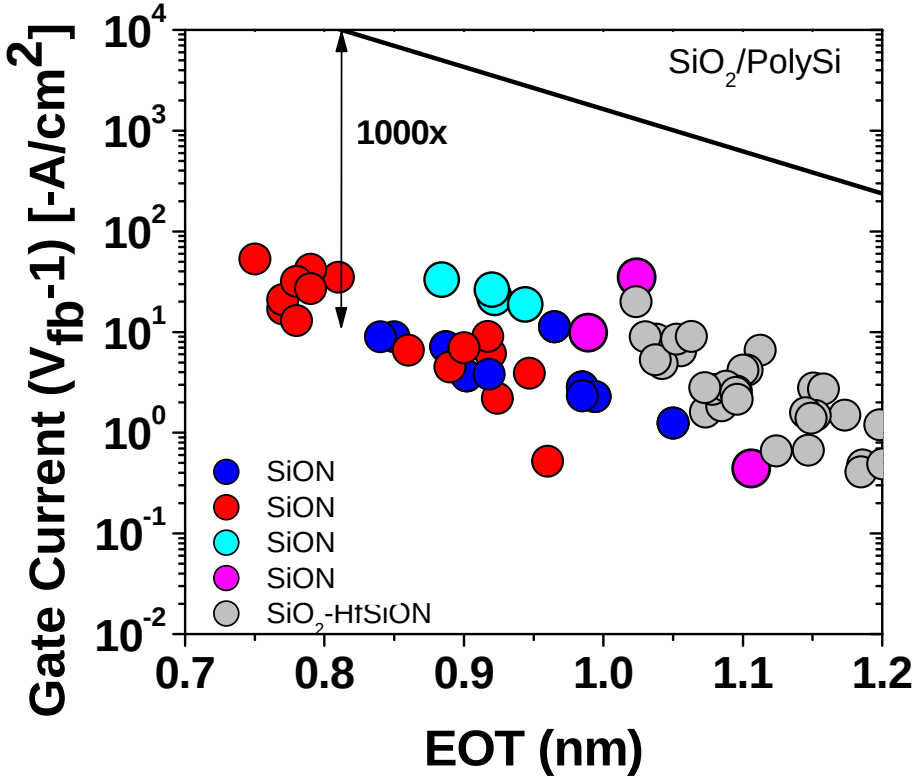
SXPS Advantage

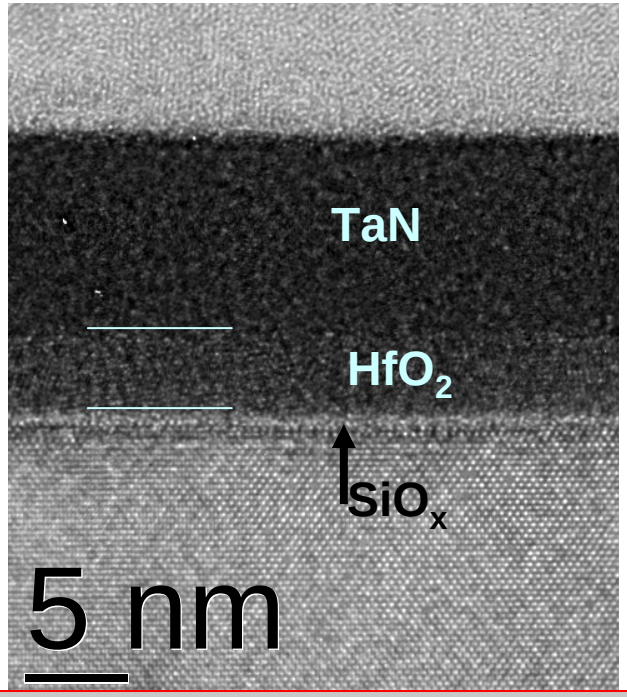
1nm AlO/1nm chem ox/Si



What is the best strategy to EOT = 0.5nm?

New material vs. SiO_x scaling





- **Zero Interface Risk:**
  - **Phonon, dipole, coulomb scatter [1,2,3]**
  - **Transient charging significant [2]**

[1] M. Fischetti et al., J. Appl. Phys., **90**, p. 4587 (2001)
[2] B. H. Lee et al., IEDM Tech. Dig., (2004) p. 689.
[3] H. Ota et al. IEDM Tech. Dig., (2007) p. 65.

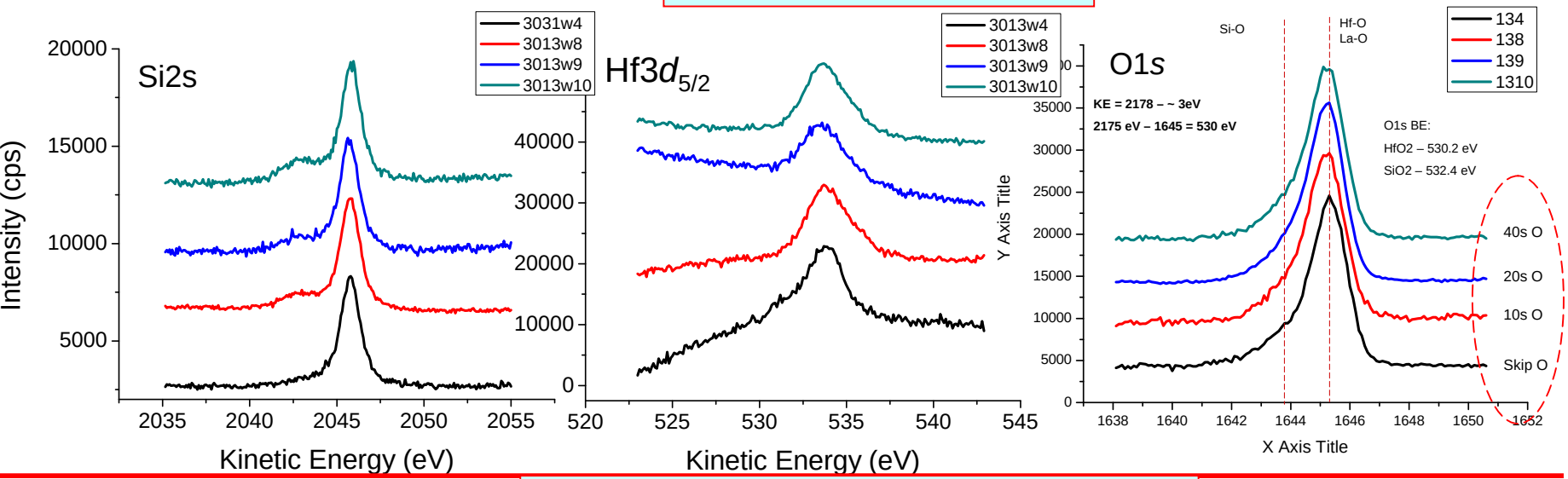
- **Higher-*k* doped HfSiON show no scaling benefit vs. undoped HfSiON.**
- **STRATEGY: Focus on scaling SiOx layer rather than a new material.**

Toward "Zero IF"

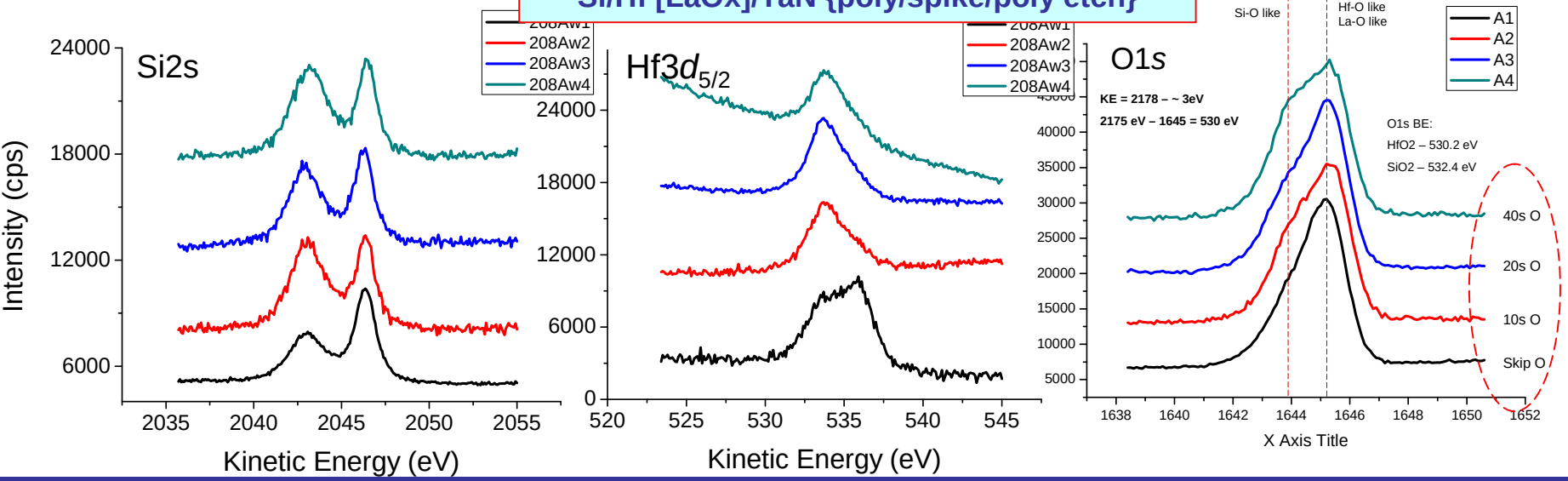
Can't use Si2p^{4+} w/La : La4$d_{3/2}$ = 105eV La4$d_{5/2}$ = 103eV

hν = 2200eV

Si/Hf [LaOx]/TaN as-dep



Si/Hf [LaOx]/TaN {poly/spike/poly etch}

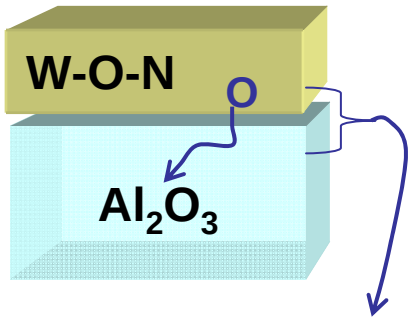


Mid to Late-transition metals are meta-stable and can release oxygen

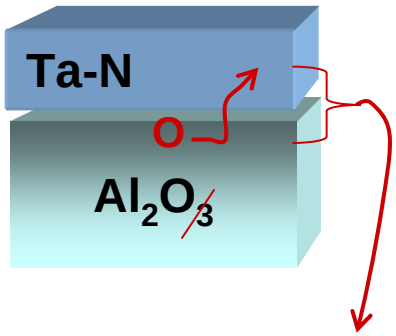
Gibbs Energy of formation: (kJ-mole^{-1} @298K)		
	IrO_2	~ -260
	MoO_2	~ -580
	TiO_2	~ -900

Late Transition Metal-oxides: Less stable

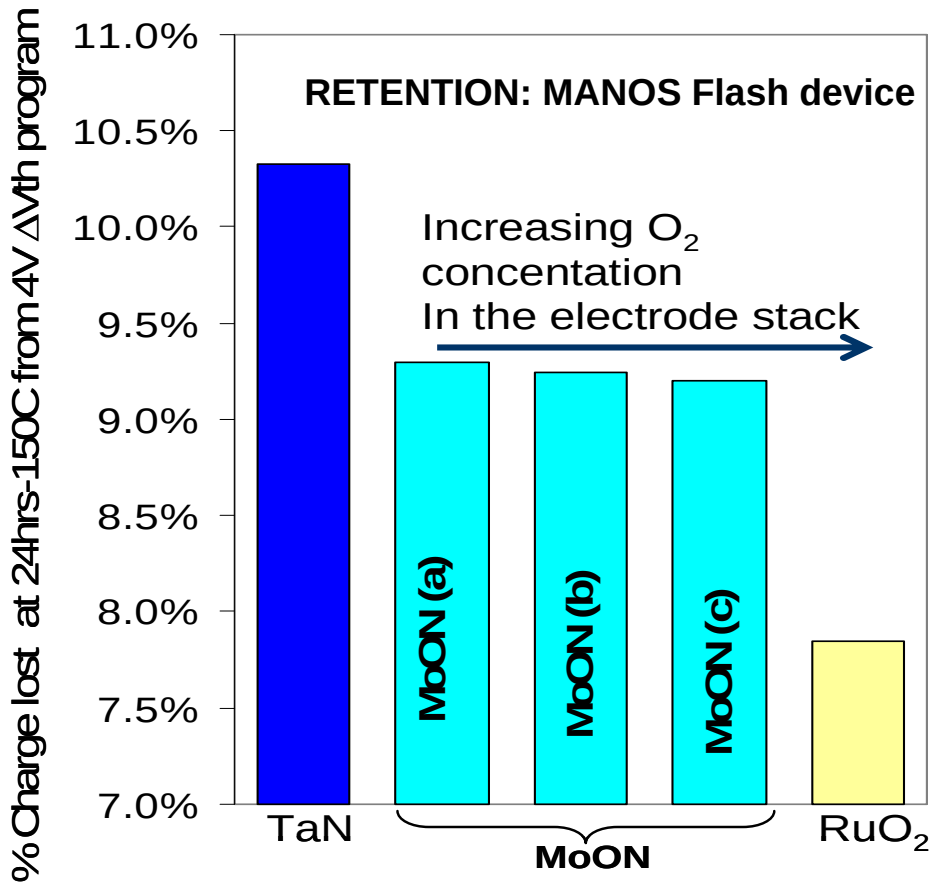
Early Transition Metal-oxides: More stable



Oxygen from electrode passivates vacancies for improved retention



Defects / Oxygen vacancies created near interface



- Retention improvement for oxygen-bearing electrode may be due available free oxygen to passivate defects/vacancies

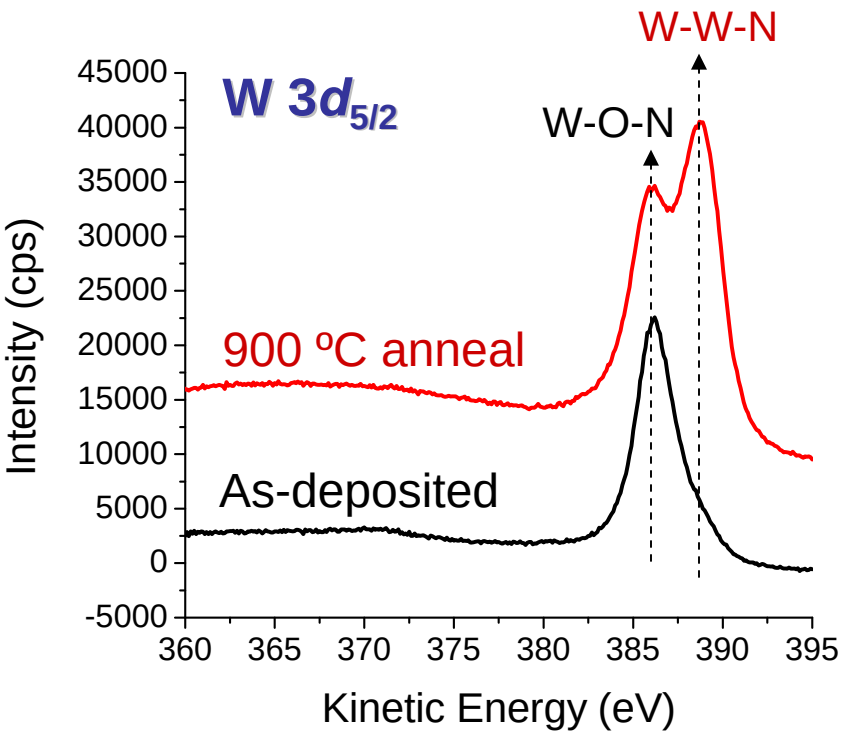
WON/Al_2O_3 interactions as-dep vs. 900°C

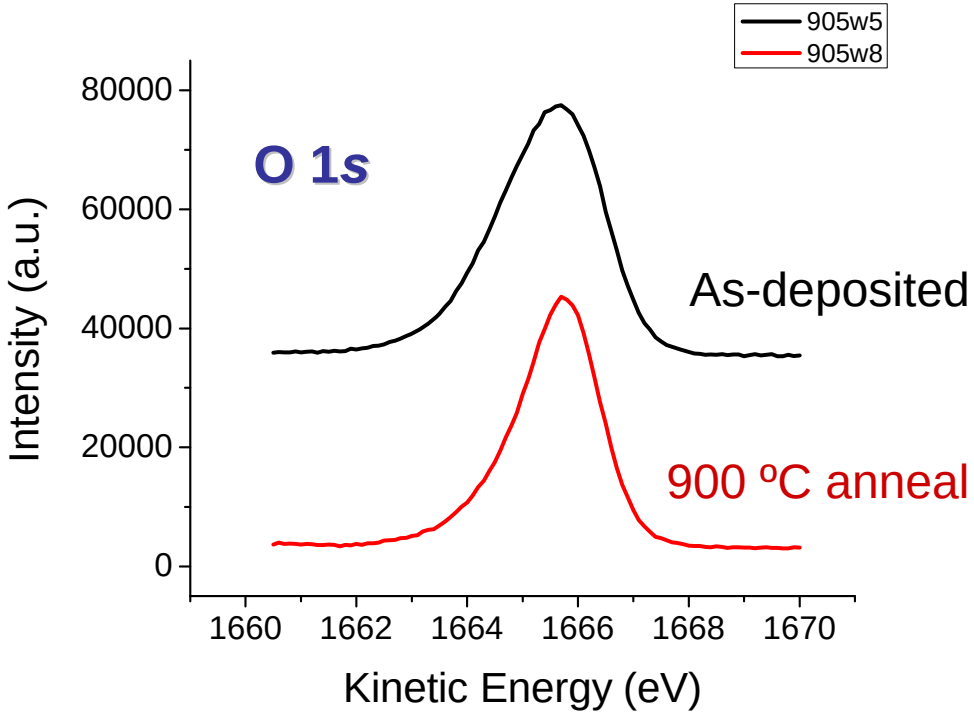
905_5: Al2O3/WON/900C

905_8: Al2O3/WON/as-dep

W reduction => Retention Improvement

hν = 2200eV





W $3d_{5/2}$ core line indicates reduction of WON and narrow-more single component O 1s core line due to 900°C anneal

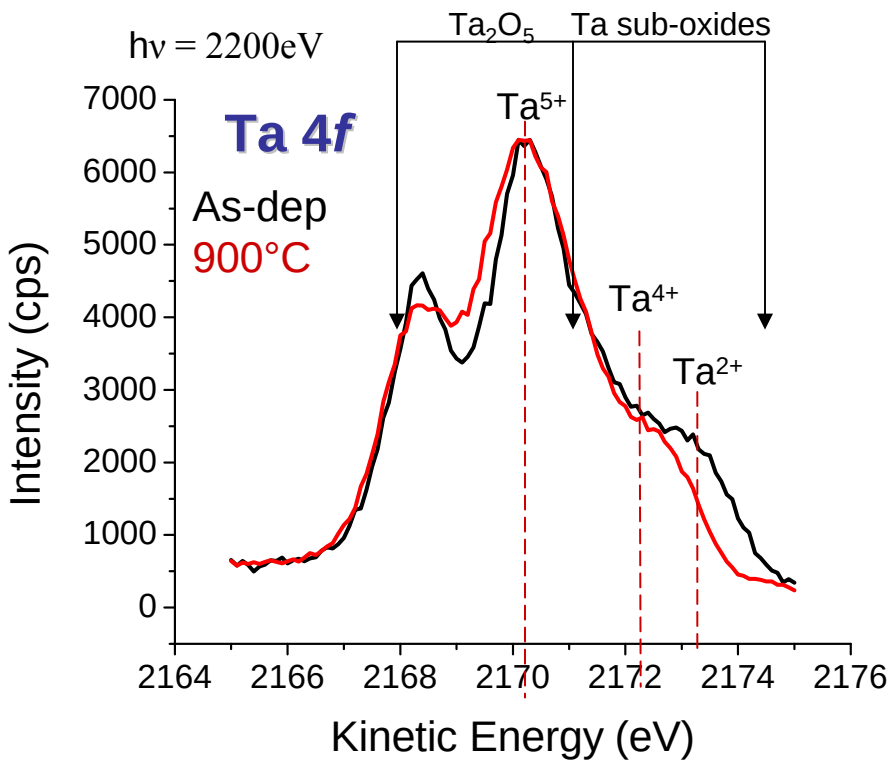
- Loss of O from WON upon anneal may contribute to less defective Al_2O_3 bulk and/or interface

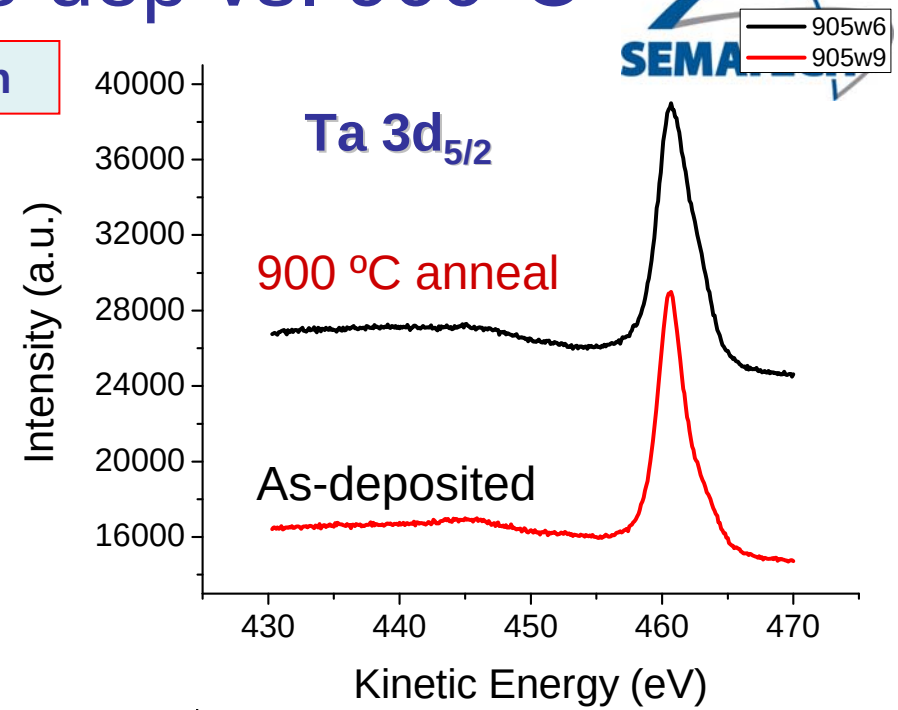
TaN/Al_2O_3 interactions as-dep vs. 900°C

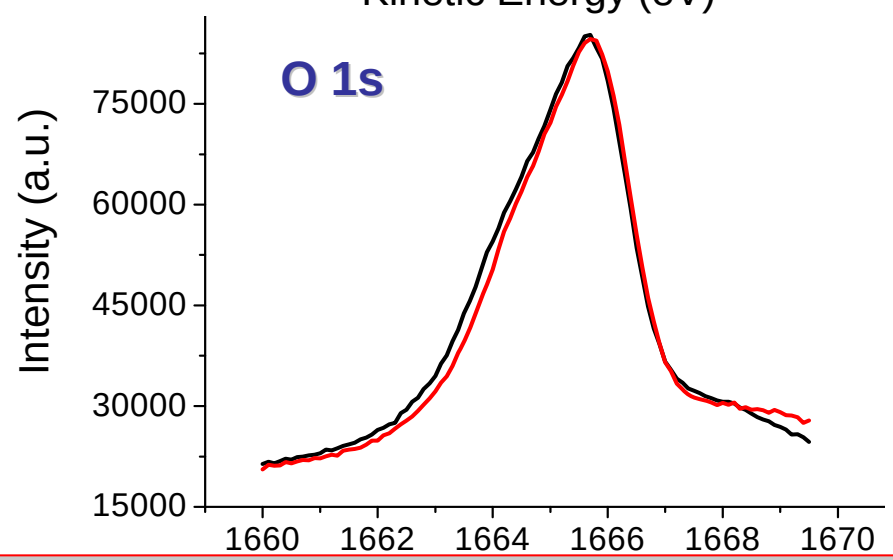
Ta oxidation => Retention Degradation

905_6: Al2O3/TaN/900C

905_9: Al2O3/TaN/as-dep







Ta $3d_{5/2}$ oxidized as deposited with only slight reduction due 900°C anneal

Scavenging of O by Ta may contribute to defects in Al_2O_3 bulk and/or interface

Summary

- We’re in an extremely dynamic and exciting period in semiconductor research – no consensus on the next architecture, - many options will continue to be explored
- Complex new materials systems - physics of single atom thick lattice networks - will be integral to many future technologies
- A suite of measurement instruments & techniques are critically needed to address fundamental engineering problems
- HAXPES will play an increasing role in characterizing heterostructures & buried interfaces – “real” samples
- Increasing need for industry engineers to partner with spectroscopy experts for multiyear investigations

International Symp on Adv. Gate Stack Technology (ISAGST) August 23-26, 2009 ~ San Francisco, California

SEMATECH

- Example topics:
  - High-k dielectrics/electrodes
  - Physics of dielectric defects
  - Modeling
  - Reliability
  - DRAM, flash, ReRAM, spin
  - RF and Mixed Signal
  - III-V, graphene channel
  - Characterization
  - Gate stack for M/NEMS

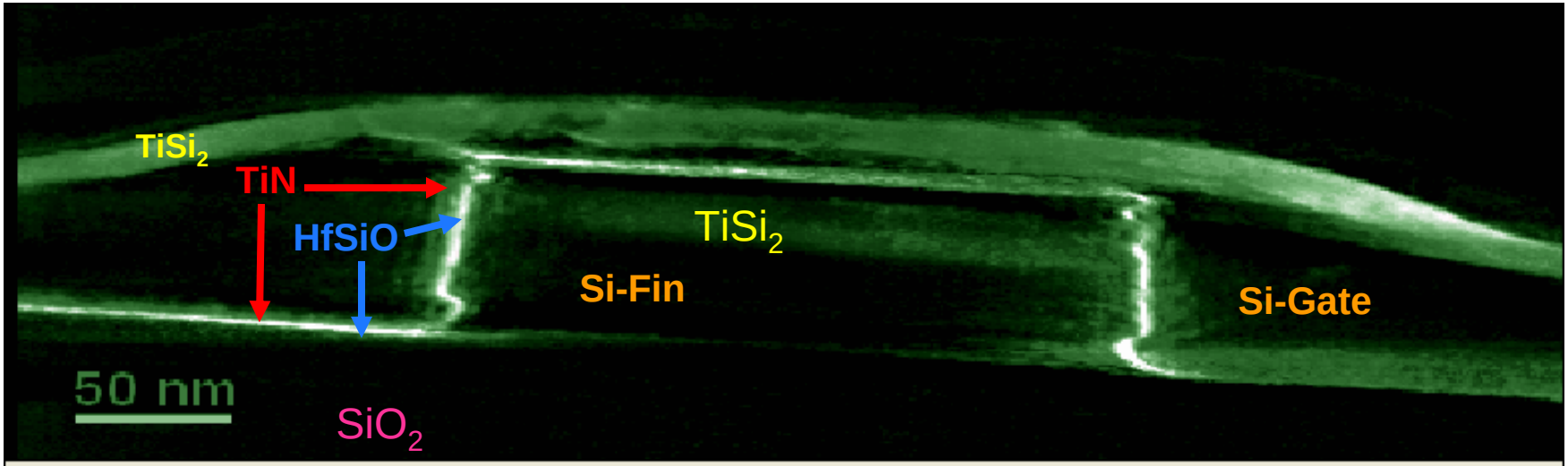
- Confirmed Invited Speakers…more to come
  - Evgeni Gousev, Qualcomm
  - Kirklen Henson, IBM
  - Geoffrey Yeap, Qualcomm
  - Sayeef Saluhuddin, UC-Berkeley
  - Jung Dal Choi, Samsung Semiconductor
  - Krishna Parat, Intel

Abstract Submission Deadline – May 22, 2009
www.sematech.org

Computed Electron Chemical Tomography

Collaboration w/Brendan Foran, The Aerospace Corp.

This movie is a sequence of views of a 3D computed model reconstructed from HAADF-STEM data



3D-FinFET-reconstruction-cal-2.avi

- Image intensity in this representation of the 3D model relates position with higher material density
- For this sample, contrast therefore dominated by the spatial distribution of heavy metal atoms such as titanium and hafnium