Development of a High-Rate Front-End ASIC for X-Ray Spectroscopy and Diffraction Applications

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***Abstract*— We developed a new front-end application-specific integrated circuit (ASIC) to upgrade the Maia X-ray microprobe. The ASIC instruments 32 configurable channels that perform either positive or negative charge amplification, pulse shaping, peak amplitude, and time extraction along with buffered analog storage. At a gain of 3.6 V/fC, 1-μs peaking time, and a temperature of 248 K, an electronic resolution of 13 and 10 e^- rms was measured with and without a silicon drift detector (SDD) sensor, respectively. A spectral resolution of 170-eV full-width at half-maximum (FWHM) at 5.9 keV was obtained with an ^{55}Fe source. The channel linearity was better than ± 1% with rate capabilities up to 40 kcps. The ASIC was fabricated in a commercial 250-nm process with a footprint of 6.3 mm × 3.9 mm and dissipates 167 mW of static power.**

***Index Terms*— Application-specific integrated circuit (ASIC), detector, diffraction (EDX), front end, mixed signal, spectroscopy (XFS), synchrotron applications.**

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I. Introduction

COST effective and nondestructive elemental mapping of complex material matrices with minimal sample preparation have attracted significant interest across a wide range of disciplines and industries. As a result, high-resolution elemental X-ray analysis has become one of the mainstream analytical tools used in exploration, industrial production, pharmaceuticals, forensics, arts, and archeology, where quality, safety, and authenticity are of high importance [1]–[4].

Advances in X-ray sensors and application-specific integrated circuits (ASICs) have played an integral role in the deployment of this technique [5]–[8]. Maia, a compact multichannel X-ray microprobe with a large detector solid angle and high throughput data acquisition system, offered the capacity for rapid sample analysis [9], [10]. In its construct, Maia incorporates an array of 384 silicon pin diodes that are read out by 12 high-energy multielement spectrometer (HERMES) front-end ASICs and 12 simultaneous captures of events with programmable timing and energy readout (SCEPTER) ASICs. In this two-ASIC solution, HERMES provides low-noise charge preamplification and shaping [11], while SCEPTER performs amplitude and timing measurements for each channel along with multiplexing and event buffering [12], [13].

The HERMES front-end ASIC is optimized in 350-nm CMOS technology for an array of silicon p-i-n diode sensors with pixel capacitance of ≈1 pF and leakage current of about 0.5 nA/cm^2 at 27 °C. The noise contribution from the sensor constrained the resolution of the instrument. To better resolve low-energy and closely spaced fluorescence photon lines, the Maia detector is being upgraded with new detectors, a new front-end ASIC developed in 250-nm CMOS technology and a high-speed readout and processing module (RPM).

The new detector is prototyped as two modular assemblies. The first configuration incorporates linear silicon drift detectors (SDDs). This upgrade is facilitated by a multiamplifier readout system (MARS) ASIC prototype with selectable full-scale energy ranges of 12.5, 25, 37.5, and 75 keV in silicon. The values for the respective gains and corresponding full-scale input charge are captured in Table I. The second configuration implements germanium strip detectors. These sensors are read out by a high-energy MARS (HEMARS) ASIC with adjustable full-scale energy ranges of 25, 50, 100,

TABLE I
MARS ASIC AND HEMARS ASIC GAIN SELECTION WITH THE RESPECTIVE FULL-SCALE INPUT CHARGE AND PHOTON ENERGY

Gain (V/fC)	[a]Input Charge (C)	[a]Photon Energy (keV)
MARS		
0.6	3.33	75
1.2	1.66	37.5
1.8	1.10	25
3.6	0.55	12.5
HEMARS		
0.184	10.86	200
0.368	5.43	100
0.736	2.72	50
1.472	1.36	25

[a] Channel full scale value at each gain setting.

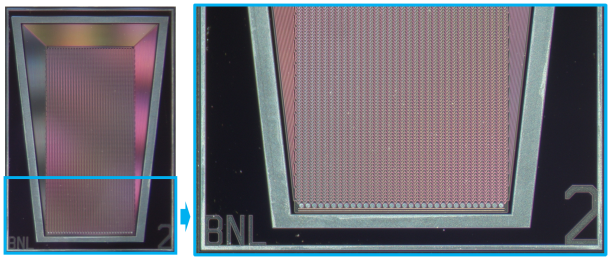

Fig. 1. Photograph of the 32-anode linear SDD, with a zoom-in view of the row of the anode pads.

and 200 keV in germanium. Likewise, the HEMARS full-scale input charge and photon energy for each gain setting are presented in Table I. Each upgrade option requires either the MARS or HEMARS ASIC for charge preamplification, shaping, and signal extraction. The RPM is common to both.

This article is organized as follows. In Section II, an overview of the linear SDD and germanium strip sensors is presented. This is followed by Section III with an architectural description of the MARS and HEMARS front-end ASICs. The experimental setup and the corresponding results are discussed in Sections IV and V, respectively. We conclude with a summary of our findings and an assessment of the future work required improving the design.

II. SENSORS FOR FLUORESCENCE SPECTROSCOPY

A. SDD

At the Brookhaven National Laboratory, we fabricated a multianode linear SDD shown in Fig. 1. SDDs are characterized by very small anode capacitance [5] in the order of 50 fF. Since the anodes are very close to the edge of the chip, the wirebonds to the MARS ASIC can be relatively short, therefore, adding a small parasitic capacitance (of approximately 100 fF). The layout of this particular linear SDD is based on the design suggested in [14], where, on the front side, a series of parallel sawtooth-shaped cathodes drives the electrons to the anode while preventing the lateral diffusion of the electron cloud. The cathodes are connected to each other by means of integrated resistors so that only the cathodes closest to and farthest from the anode row need to be biased at about -10 and -150 V, respectively.

The maximum drift length of the electrons is 1 cm. Differing from the design in [14], the backside is a uniform p+ implant, meant to be a thin entrance window for the X-rays, as is the norm with SDDs for spectroscopic applications [15]. Following the process steps reported in [16], the entrance window is made by a low energy boron implant through a thin (50 nm) screen oxide, and no metal is deposited on the oxide.

The entrance window is biased in the range of -60 to -80 V, close to the depletion voltage of the substrate. The anodes are at a pitch of about 150 μm, which matches the MARS ASIC channel pitch. The sensor has an anode leakage current of about 200 pA at room temperature, dominated by the surface leakage current.

B. Germanium Strip Sensor

We used the MARS and HEMARS ASICs for the testing and development of germanium strip detectors for a variety of synchrotron applications. Germanium has been the material of choice for high-energy X-ray and gamma-ray detection. The availability of detector grade crystal is pivotal in the development of efficient detectors that can operate at or near the Fano limit. The strip sensors used in this article are fabricated at Forschungszentrum Julich [17] and are based on a process that relies on trenching for strip isolation. These detectors are 3-mm thick and are biased just below 300 V for full depletion. The first detector system built with 12 MARS ASICs and 384 strips has a sensor geometry of 8-mm-long strips separated by 30-μm-wide trenches for a pitch of 0.125 mm. The sensor is mounted in thermal contact with a cold finger, and insulating ceramic standoffs isolates the readout board from the cold plate. The ASICs are connected to the sensor through wirebonds, as shown in Fig. 2. A silicon diode mounted near to the ASICs as a temperature monitor shows a temperature of about 223 K, while the sensor is at 100 K.

III. ASIC ARCHITECTURE

The MARS ASIC is developed to readout SDDs with adjustable full-scale photon energy from 12.5 to 75 keV in silicon. The 37.5- and 75-keV energy scales are initially used to prototype germanium-based detection systems. Subsequently, we developed a HEMARS with energy settings from 25 to 200 keV in germanium. The architecture of the ASICs builds on the design presented in [8]. These new front ends are optimized to process either positive or negative charge with continuous event-driven (CED) readout. That is, each channel performs signal processing and readout independent of the others for high throughput. The informational value afforded by the architectural description that ensues applies equally to MARS and HEMARS as they differ only in topology due to the optimization of their respective signal processing chains for either silicon or germanium sensors.

A. MARS and HEMARS Chip-Level Architecture

A block diagram of the MARS/HEMARS ASIC is shown in Fig. 3. The chip comprises a configuration register, a test

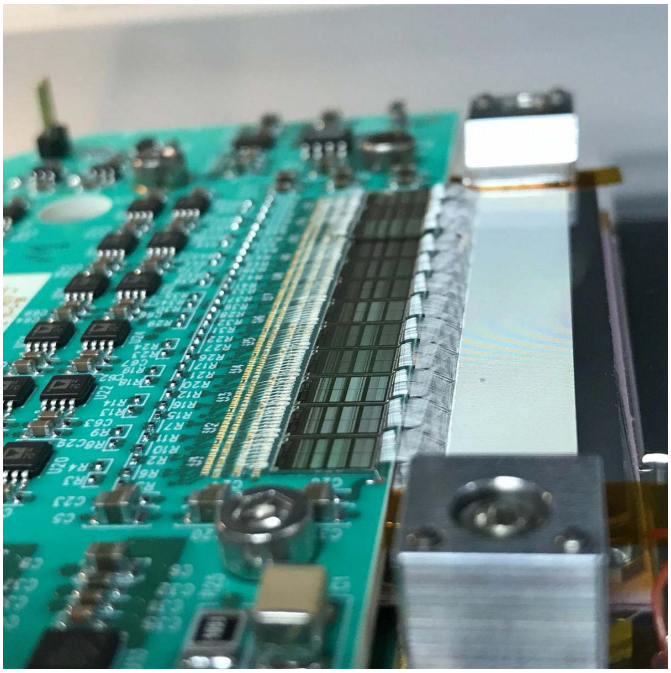

Fig. 2. 384-Germanium strip wirebonded to the MARS ASIC.

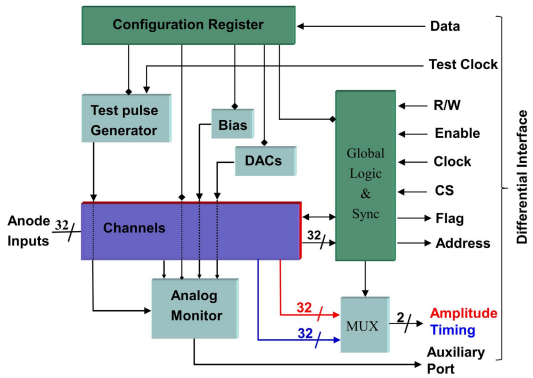

Fig. 3. MARS and HEMARS block diagram with 32-input channels. Through configuration registers, the ASICs implement selectable gain and peaking times along with adjustable bias, DACs, and test pulse generator. Global control logic arbitrates data write-in, acquisition, channel readout, and analog monitoring.

pulse generator, a bias network, two digital-to-analog converters (DACs), 32-input channels, an analog monitor, three 32-to-1 multiplexers, a global logic block, and a differential interface.

For benchtop characterization or *in situ* debugging of the ASIC, an embedded test pulse generator is used to inject positive or negative charge into the front ends. An analog monitor with an auxiliary port provides the capability to verify critical analog circuit blocks. For each measurement setting, an adjustable bias network establishes the dc operating point of the circuits according to the register configuration. The back end of the chip has a global logic and synchronization block that manages the ASIC during serial write-in, signal acquisition, event synchronization, and readout.

The 32-input channels implement the option to process either electrons or holes with programmable gains and adjustable peaking times. When a channel with an above-threshold event finds a peak, the global logic block places a

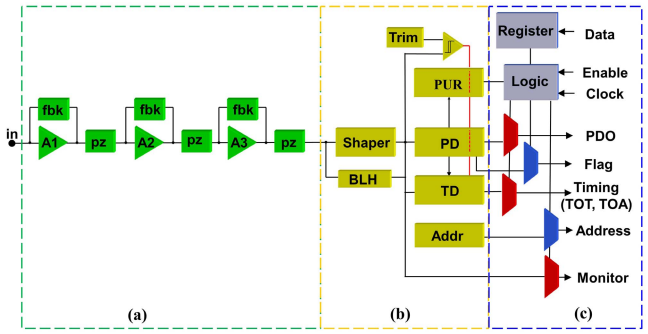

Fig. 4. MARS channel architecture illustrating. (a) Multistage charge amplifier with adaptive feedback and polarity selection. (b) Fifth-order shaper with BLH, discriminator with adjustable trim, PD, and TD for signal extraction. (c) Control logic with signal multiplexers.

token in the channel and releases a flag to the external RPM. The token is used to control the channel multiplexers for sparse readout of the peak amplitude, timing, corresponding address, and flag status. Subsequently, the external RPM digitizes the data on the bus. If multiple channels detect a peak, they are read out sequentially from the lowest to the highest address. Since some channels are being read, while others are acquiring, the ASIC interface is fully differential to minimize digital pickup. The only exception to the differential interface is the auxiliary monitor port, which is used for the sole purpose of debugging.

B. MARS Channel Architecture

The MARS front-end preamplifiers are optimized for 50 fF of input capacitance and leakage currents from 100 fA to 1 nA. The input MOSFET operates at 475 μA of drain current with a geometry (W/L) of 100.8 μm/0.36 μm [18]. The primary application is the readout of SDDs that are sensitive to soft X-ray fluorescence photons.

The channel implementation of MARS is illustrated by the block diagram shown in Fig. 4. The signal processing chain in each of the 32 channels is organized in three subblocks that perform the functions of charge preamplification, signal extraction, and data multiplexing.

The multistage charge amplifier is designed with three cascading stages. The first stage provides a charge gain of 38, and the second charge gain stage is selectable between 14/3, 28/3, 14, and 28. The third stage serves as either a unity gain pass-through for a negative charge or an inversion for the positive charge to ensure signal compatibility at the shaper input. Each amplifier implements continuous adaptive reset in the feedback path followed by pole–zero cancellation [19]. By default, the channels are sensitive to the negative charge, but the polarity can be changed to positive charge sensitivity through a configuration register bit.

A fifth-order shaper provides analog filtering with adjustable peaking times of 0.25, 0.5, 1, and 2 μs. The shaper implementation has one real pole, while two pairs of complex conjugate poles are contributed to the constellation by two multiple feedback (MFB) stages [20]. Also, the shaper contributes a signal gain of $\approx$0.00338 V/fC to the signal for overall channel gains of 0.6, 1.2, 1.8, and 3.6 V/fC. Baseline stabilization is

realized with a bandgap-referenced baseline holder (BLH) in feedback with the shaper [21].

Thresholds are set with a 10-bit DAC and baseline dispersions are compensated by a low hysteresis discriminator with 5-bit trim per channel. The output of the discriminator serves as a trigger for the above-threshold events, extraction of the shaped signal amplitude with the peak detector (PD), and time-over-threshold (TOT) or time-of-arrival (TOA) measurements with the time detector (TD).

The back end of each channel is reserved for local registers, data multiplexers, and control logic. During debugging and calibration, the configurations that are unique to the channel are managed by local registers. Similarly, since each channel operates independently of the others, the channel logic communicates with the global logic that arbitrates event acquisition and CED readout. During acquisition, the control logic ensures that all channels with events below the threshold remain in the acquisition mode. Furthermore, if a channel finds a peak, the control logic processes the peak, prepares the channel for readout, and, then, notifies the global logic of a successful event. The global logic sends a flag to the RPM, which responds by sampling the peak amplitude and timing while reading the channel's address and flag status simultaneously. After the readout is completed, the channel reset then returns to acquisition mode.

C. HEMARS Channel Architecture

The channel architecture of HEMARS is also represented by Fig. 4. The front-end channels are optimized for 50 fF of input capacitance and leakage currents from 100 fA to 1 nA. A charge gain of 30 is implemented in the first preamplifier stage, while the second stage is adjustable to 7/4, 7/2, 7, and 14, respectively. The shaper contributes ≈0.00351 V/fC of gain. The overall channel gain is programmable from 0.184, 0.368, and 0.736 to 1.472 V/fC corresponding to 200, 100, 50, and 25 keV in germanium.

D. ASIC Prototype

A micrograph of the MARS ASIC is shown in Fig. 5. There are 32 analog inputs that interface with the sensor. Each channel is laid out in a linear arrangement from preamplifiers, shaper, peak, and TD to local register and logic. At the back end of the chip are the DACs, the global configuration registers, and global logic. The low-voltage differential signaling (LVDS) pads for the digital inputs and outputs are located on the top-right edge of the chip and isolated from the analog pads to prevent coupling. No pads are allowed on the horizontal sides of the ASIC as the chips are abutted to match the sensor pixel pitch in order to minimize the spreading of the wirebonds. The latter constrains the maximum die-cut size to 6.3 mm × 3.9 mm; 12 MARS ASICs are required to read out the 384 anodes of the Maia detector.

IV. Electronic Hardware Integration

The full-signal-processing hardware shown in Fig. 6 is comprised of an RPM that interfaces with either the HEMARS carrier board or the MARS carrier board through a rigid-flex interconnect printed circuit board. The assembled system

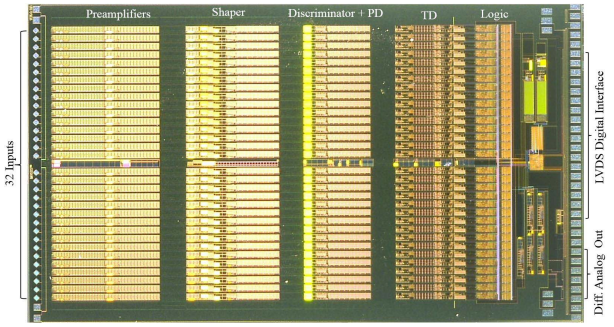

Fig. 5. Micrograph of the MARS ASIC with 32-input channels. Each channel is linearly arranged as a multistage preamplifier, a shaper, discriminator, PD, TD, and logic. The bias is laid out horizontally between two groups of 16 channels. The DACs, registers, and analog buffers are implemented at the back end of the chip.

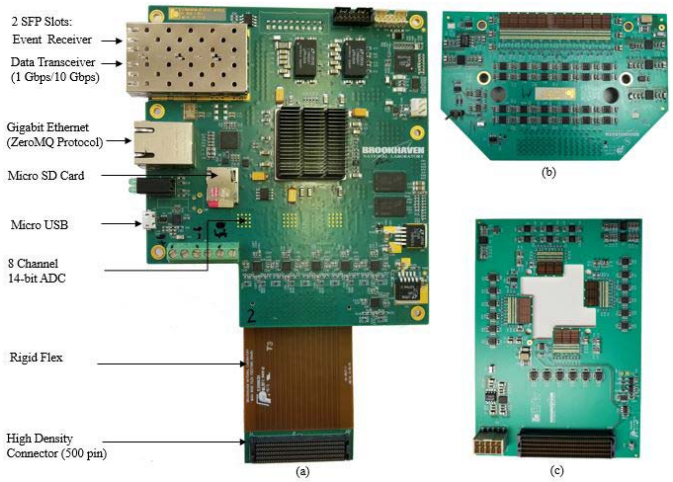

Fig. 6. Maia detector upgrade electronics. (a) External RPM with Zilinx Zynq-7000 SoC FPGA, including embedded ARM Cortex A9 processor. Two 1-Gb/s SFP slots for event receiver and data transmission, Giga-bit Ethernet, and three eight-channel 25 MSPS 14-bit ADC. High-density rigid-flex cable with 500-pin connector. (b) HEMARS carrier board with 12 ASICs mounted in a linear arrangement. (c) MARS carrier board with three ASICs mounted per quadrant, compatible to the Maia detector.

is used for ASIC characterization, X-ray fluorescence spectroscopy, and energy-dispersive X-ray diffraction.

The RPM in Fig. 6(a) includes a Xilinx Zynq-7000 SoC field-programmable gate array (FPGA) with dual-ARM Cortex-A9 processor running Debian Linux. The FPGA bit file, Linux kernel, and root file system are stored on a micro-SD card. For high-speed data, two small form-factor pluggable (SFP) transceiver slots are implemented. One slot is for an embedded event receiver that is compatible with the timing system at the National Synchrotron Light Source II (NSLS II) at the BNL. The other SFP slot uses the User Datagram Protocol (UDP) communication protocol for the transmission of list mode event data from the detector over gigabit Ethernet. Furthermore, the user interface is accessible either through gigabit Ethernet connection (ZeroMQ Protocol) or console login via the micro-universal serial bus (USB) serial port. Three eight-channel analog-to-digital converters (ADCs) with the 14-bit resolution are mounted on the back of Fig. 6(a). The ADCs sample analog data from 12 ASICs, each with dedicated amplitude (PD) and timing (TD) port. With the ADC running continuously at 25 Mb/s, the data throughput is ≈8.4 Gb/s

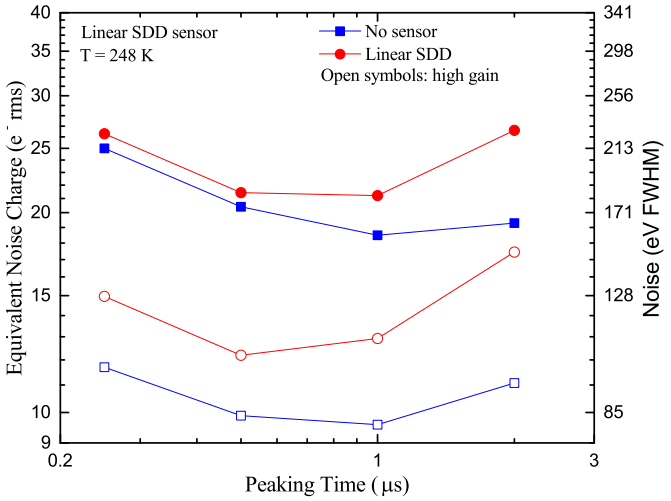

Fig. 7. MARS ENC as a function of peaking time without sensor (blue trace) and with the linear SDD (red trace) at 248 K at the shaper output. The solid symbols are for measurements at 0.6 V/fC (75 keV), while the open symbols are measurements taken at 3.6 V/fC (12.5 keV).

$(3 \times 8 \times 14 \times 25)$ without any metadata headers. Detailed information of the RPM is reported in [22].

The ASIC carrier boards are fabricated from low-loss Rodgers RO4000 laminates and populated with discrete components that are vacuum compatible at 10^{-6} torr. On each carrier board, the ASIC locations are determined by the sensor geometry. The HEMARS carrier board with 12 ASICs installed in a linear arrangement without the sensor is shown in Fig. 6(b). Fig. 2 shows a picture of the same module with the Ge strip sensor wirebonded to the ASICs. Similarly, the MARS carrier board with three ASICs mounted on each quadrant without the SDD is shown in Fig. 6(c). The other discrete components are identical for both boards. Most notable on each carrier are the 500-pin high-density connectors, 24 buffers (two per ASIC) that drive the external ADCs on the RPM, and the low-dropout regulators that supply power to the ASICs. Each detector module is capable of reading out a maximum of 384 Ge strips or 384 SDD anodes.

V. Results

A. Results From the MARS ASIC Prototype

As depicted in Table I, at the highest gain setting of 3.6 V/fC (corresponding to a full-scale charge input of 0.55 fC or full-scale energy of 12.5 keV in silicon) and lowest gain of 0.6 V/fC (corresponding to a full-scale charge input of 3.33 fC or full-scale energy of 75 keV in silicon), a true rms meter was used to measure the noise voltage at the output of the shaper on the auxiliary monitoring port. Fig. 7 shows the equivalent noise charge (ENC) as a function of peaking time with (red trace) and without (blue trace) the linear SDD connected at 248 K. At the highest gain (3.6 V/fC) and 1-μs peaking time, an ENC of 10 e^- rms was obtained which corresponds to a dynamic range (DR) of ≈147. With the sensor connected, the ENC increased to 13 electrons (DR of ≈113). At the lowest gain (0.6 V/fC) and 1-μs peaking time, we measured 21 and 18 e^- rms with and without the sensor, corresponding to a DR of 419 and 488, respectively.

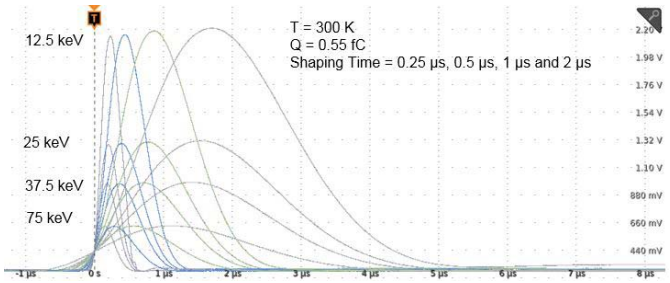

Fig. 8. MARS shaper response to 0.55 fC of injected charge at each energy setting and peaking time.

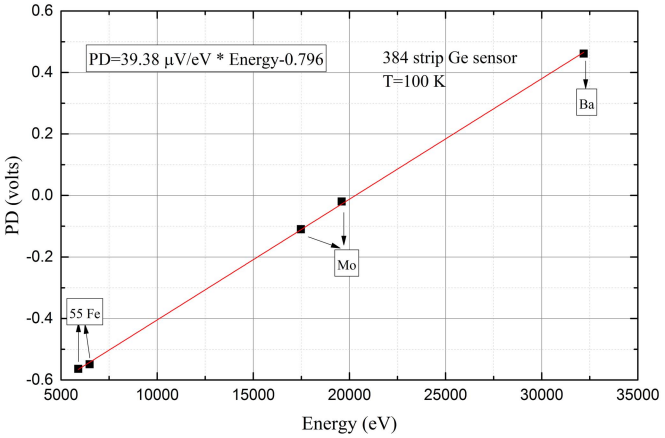

Fig. 9. Energy calibration of detector with a 384 strip Ge sensor at 100 K readout by 12 MARS ASICs (1.2 V/fC). X-ray photons were from ^{55}Fe source and molybdenum and barium targets excited by ^{241}Am. The linearity was better than ± 1%.

The increase in ENC at each gain setting with the sensor connected was due to the added parasitic interconnection capacitance, the sensor anode capacitance (≈100 fF), and the sensor leakage current. Regarding the difference in total ENC between low gain (0.6 V/fC) and high gain (3.6 V/fC), this contribution came from the shaper. Compared with the HERMES front end in [11], the electronic noise without sensor decreased from 14 to 10 e^- rms in MARS. This is an improvement for the Maia upgrade. In addition, the front-end power dissipation was reduced from 11 to 3.6 mW/ch. At the system integration level, the assembly process was simplified as the HERMES and SCEPTER pair were replaced by a one ASIC solution. That is, either MARS or HEMARS performed a complete readout of the sensor since each channel implemented the full-signal-processing chain with dedicated peak and TDs.

The integrated test generator was used to inject 0.55 fC of charge into the front end. The chip was configured so that the shaper output of a channel was multiplexed onto the auxiliary port where it was monitored with an oscilloscope. Fig. 8 shows the recorded waveform at each gain and peaking time. At 3.6 V/fC (full scale), the semi-Gaussian pulse responses had a peak value of approximately 2.2 V and a nearly symmetrical return to baseline. The amplitude of the signal is the difference between the peak value and the channel baseline (≈250 mV). At full-scale signal swing, this amounts to a discrepancy of about 1.5% between the measured and the theoretical value of the pulse amplitude.

At a gain setting of 1.2 V/fC and 1-μs peaking time, the MARS ASIC was used to read out a biased 384 strip

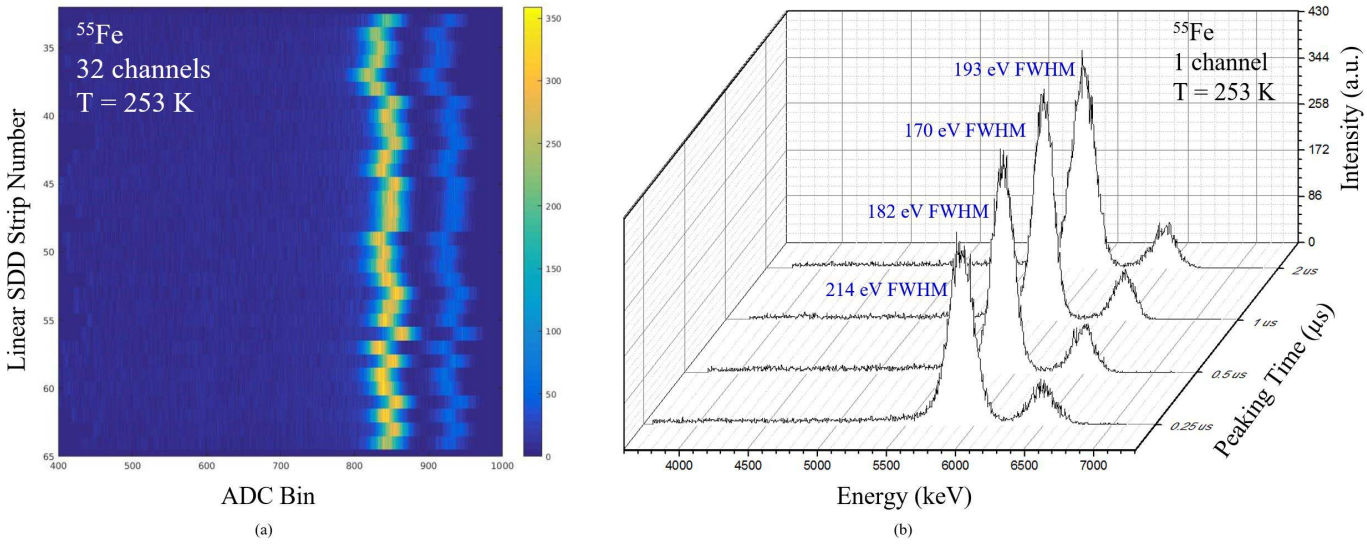

Fig. 10. MARS ASIC readout of a linear SDD without calibration for dispersion in baseline, threshold, and gain. (a) Intensity map from a 32-anode linear SDD with the Mn K_α and K_β lines. (b) Spectral resolution of the Mn K_α peak range from 170- to 214-eV FWHM from 0.25- to 2-μs peaking time.

germanium sensor that was cooled to 100 K. An ^{55}Fe source and an ^{241}Am source used to excite molybdenum (Mo) and barium (Ba) targets were used to determine the ASIC linearity over the 37.5-keV energy range. From left to right, Fig. 9 shows the manganese (Mn) K_α (5.9 keV) and K_β (6.5 keV), Mo K_α (17.4 keV) and K_β (19.6 keV), and Ba K_α (32.2 keV) characteristic X-ray photo peaks. Linearity better than $\pm 1\%$ was achieved.

In addition, spectral measurements with an ^{55}Fe source were taken with a 32-anode linear SDD cooled to 253 K. The MARS ASIC was configured for a gain of 3.6 V/fC (12.5-keV energy range), and the acquisition was executed at each peaking time. Fig. 10(a) shows the intensity map of the 32-ASIC-channel response without calibration for uniformity of response. The Mn K_α (5.9 keV) and K_β (6.5 keV) lines are clearly seen. The fit spectra from one channel are shown in Fig. 10(b). The measured full-width at half-maximum (FWHM) at 5.9 keV was 214, 182, 170, and 193 eV at 0.25-, 0.5-, 1-, and 2-μs peaking times, respectively. These results confirmed the ENC measurement with the linear SDD at a high gain in Fig. 7. Without a radiation source in Fig. 7, the total noise amounted to the measured contributions from the readout electronics, sensor leakage current, and capacitance. For the spectra in Fig. 10(b), signal formed inside the sensor experienced statistical fluctuations that contributed to the noise according to Fano statistics. Inevitably, the photopeak was broadened with an effective resolution given by $\sigma_{\text{eff}} = (\sigma_{\text{stat}}{}^2 + \text{ENC}^2)^{1/2}$.

We investigated the impact of event rate on the photopeak location of spectra collected with the MARS ASIC reading out a 96-pixel silicon p-i-n diode sensor cooled to -20 °C. Both an ^{55}Fe source and the internal test pulse were tuned for event rates of 2.5 and 25 kHz. From the plots shown in Fig. 11(a) and (b), the peak shift was approximately 2 arbitrary unit (a.u.) bins as evidenced by the centroids of the Mn K_α and K_β photopeaks and the test pulse.

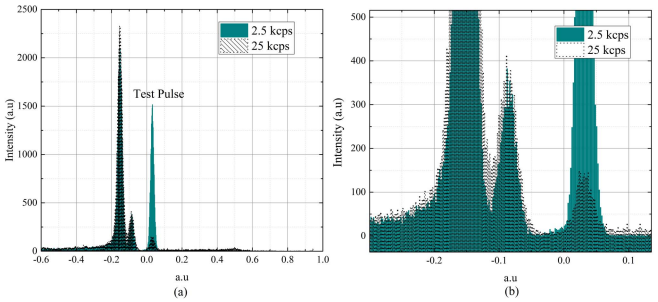

Fig. 11. MARS ASIC readout of a 96 pixel silicon p-i-n diode sensor cooled to -20 °C. (a) ^{55}Fe source and internal test pulse rate of 2.5 (green) and 25 kcps (black). (b) Zoomed-in view segment shows a photopeak and test pulse shifts of 2 a.u. bins.

B. Results From the HEMARS ASIC

In diffraction studies, photons with energies up to 200 keV are of interest. Since the MARS chip was primarily designed for use with silicon-based detectors, the gain setting was limited to 75 keV. Analysis with germanium detectors was geared to be used in high-energy diffraction experiments with photon energy as high as 200 keV. The HEMARS ASIC addressed the latter as its gain selections were optimized for 25 to 200 keV in Ge. Measurements with the germanium sensors were obtained at approximately 100 K to minimize the sensor dark current. Fig. 12 shows the response of all 384 channels to an ^{241}Am radioactive source. This has a strong line at 59.5 keV and several weak lines at lower energies. The measured resolution was 610-eV FWHM at 59.5 keV.

A 192-strip detector with a 0.25-mm pitch was interfaced with the HEMARS chip. A copy of the HEMARS ASIC carrier board from Fig. 2 was used, except to accommodate the 192-strip, alternate ASICs were omitted. Fig. 13 shows the detector assembly. The detector showed an energy resolution of about 770-eV FWHM for a 122-keV line from a ^{57}Co source. Details of these results can be found in [22].

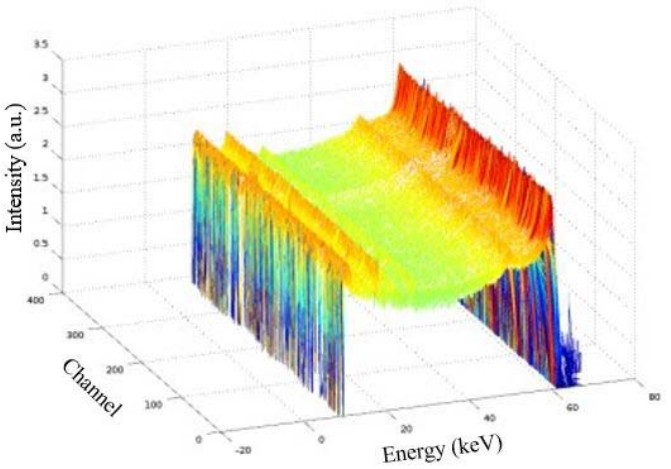

Fig. 12. Spectral response of 12 HEMARS ASICs reading out 384 strips of Ge sensor irradiated by the ^{241}Am source.

Fig. 13. Completed 192-strip detector with HEMARS. The gold pad shows the omitted ASICs.

Fig. 14 shows the measured effect of event rate on peak position with HERMES ASIC and HEMARS ASIC prototypes. Selenium (Se) and tungsten (W) foils were excited with the full white beam spectrum at the Argonne National Laboratory Advance Photon Science (APS) bending magnet 1-BM. This beamline contains photons from 5 keV to energies beyond 100 keV [23]. Germanium strip sensors were used to detect the secondary X-ray photons from the targets. The Se foil spectra acquired with two HERMES ASICs in the original Maia detector reading out a 64-strip germanium sensor shows the Se K_α (11.22 keV) and K_β (12.49 keV) lines, respectively. For this readout system, the photopeak shifted by almost one pulsewidth from 1.5 to 15 kcps. Similar measurements were taken with fluorescence photons from a W target. Here, a 192-strip detector was readout by six HEMARS ASICs in the Maia detector upgrade. The tungsten spectra shows the $K_{\alpha 1}$ (59.32 keV), $K_{\alpha 2}$ (57.98 keV), $K_{\beta 1}$ (67.24 keV), and $K_{\beta 2}$ (69.08 keV) X-ray emission lines, respectively. For rates from 1 to 40 kcps, the peak shift was about two analog-to-digital unit (ADU) bins. This added capability of high rate and high throughput with only two ADU degradation in the peak location was another upgrade to the Maia detector [9].

Regarding the reading out of the MARS ASIC and HEMARS ASIC at high event rates, it was observed that the token passing readout scheme exhibited preferential bias

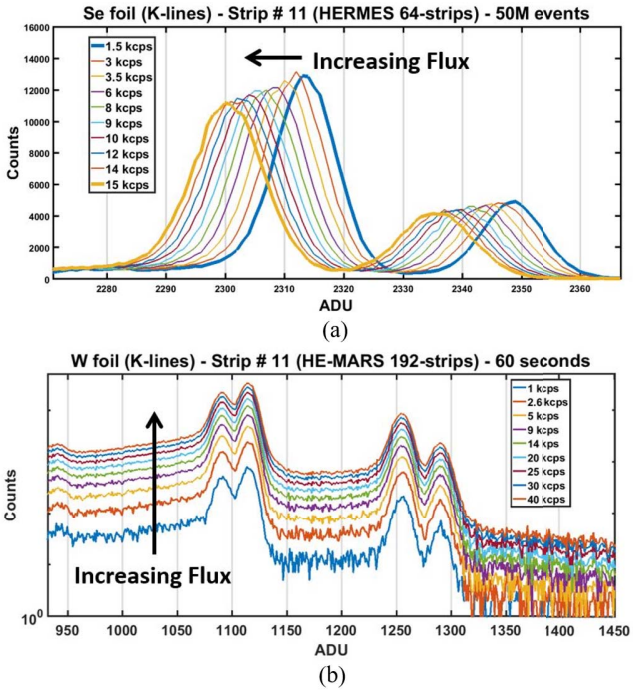

Fig. 14. (a) HERMES X-ray spectra of selenium with a peak shift of approximately one pulsewidth when the flux increased from 1.5 to 15 kcps. (b) HEMARS spectra of tungsten with a peak shift of less than two ADU bins for flux up to 40 kcps.

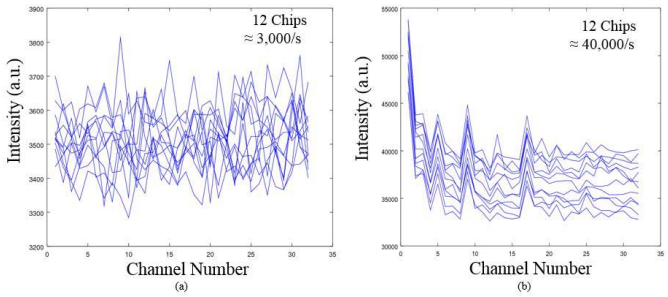

Fig. 15. 12 HEMARS ASIC event response to a flood field illumination from a 17.45-keV X-ray source. (a) At a rate of ≈ 3000/s, the integrated intensity shows normal statistical fluctuations. (b) At a rate of 40 000/s, the low address channels are systematically processed with preference above high-order channels.

toward low address channels. We further investigated this behavior with an X-ray generator producing 17.4-keV photons (Mo K_α) to uniformly irradiate a 384-strip Ge sensor. The intensity on each channel of the HEMARS ASIC was captured in Fig. 15. Each trace represents the count from 32 channels on one ASIC. At a rate of 3000 events/s, the 12 chips reported the expected integrated intensity shown in Fig. 15(a), with the anticipated statistical fluctuations. However, when the rate was increased to 40 000 events/s, it was observed that the integrated intensity of low address channels was higher than those with a higher address. The periodic spikes are explained by the algorithm used in the logic to arbitrate clusters of four channels. Even though the ASIC implemented a sparse readout, the token entered the chip on channel 1 and exited on channel 32. As a result, at high rates, the low-order channels experienced preferential access to the RPM. Ideally, it was

desired for channels to be read in the order in which events arrived. To explain Fig. 15(b), consider a high-rate scenario in which channel 20 acquired an event and signaled to the ASIC global logic that it was ready to be read. The global logic responded by releasing a token that should bypass all channels and stop on channel 20. Now, assume that channel 6 released a flag within a clock cycle of channel 20 reporting that the token would be captured by channel 6. The problem was further exacerbated if, during the time, the RPM takes to digitize the analog outputs of channel 6, and other channels with addresses greater than 6 and less than 20 acquired events. This put channel 20 further in the queue to be read. This issue will be addressed in the next revision to prioritize readout based on the order in which the channels report to the global logic.

VI. Conclusion and Future Work

Compared with the HERMES ASIC, the MARS and HEMARS ASIC prototypes provided improved noise, rate, and power performance for the Maia detector upgrade. In addition, the ASICs have demonstrated the capability to read out both silicon and germanium sensors with high resolutions at rates up to 40 kcps for XFS and EDX experiments at synchrotrons, just to name a few applications.

In our characterization of the ASICs, two issues were observed that will be addressed in the next revision. First, the initial concept for the system-level design required that groups of three ASICs share a common ADC on the RPM. This requirement was met at the ASIC level through the implementation of analog tristates on the PD output and the TD output so that only the chip being read could put data on the analog bus. It was observed that whenever a chip was first accessed for readout, as it came out of tristate, PD and TD were slow to settle. On average, the settling time should be about 10 ns, but TD took as long as 200 ns to settle on the first read, after which it behaves normally. The RPM upgrade implements a parallel readout of the ASICs. Therefore, the tristating capability is no longer required and will be removed. Another improvement involves optimizing the signal path from the peak and TDs to the external ADC, that is, lowering the parasitic load while increasing the driving capability of the buffer. In the next prototype, the on-chip buffer will be revised to drive the external ADC directly.

Second, the issue with the token favoring low address channels at high rates will be addressed by eliminating the token passing scheme. Instead, a FIFO-based logic will be used to record the order in which the channels acquire events and perform the readout in the same manner.

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