Analog Peak Detector and Derandomizer for High-Rate Spectroscopy

Gianluigi De Geronimo, Anand Kandasamy, and Paul O'Connor

***Abstract*—A compact and accurate readout system has been developed for high-rate spectroscopy with multi-element detectors. The fully self-triggered system multiplexes the signals from 32 detectors into a novel peak detector, which also serves as a derandomizer. The captured pulse heights are stored as analog samples before being presented to the ADC along with the corresponding channel addresses. The peak detector incorporates a new two-phase configuration that cancels offsets and other errors found in conventional designs. Offset cancellation gives the peak detector rail-to-rail sensing and driving capability and permits two or more peak detectors to be operated in parallel to serve as a data-driven analog memory.**

First experimental results on the new peak detector and derandomizer (PDD) circuit, fabricated in 0.35 μm CMOS technology, include a 0.2% *absolute* accuracy for pulses with 500-ns peaking time, 2.7-V linear-input range, 3.5-mW power dissipation, 250-mV/s droop rate, and negligible dead time. We have tested the system with 32 CZT detectors and a ^{241}Am source. The spectra collected from the 32-channel system show that the noise performance of the preamp/shaper is not degraded by the multiplexing, peak detecting, and derandomizing operations.

***Index Terms*—CMOS, derandomizer, peak detector.**

I. Introduction

LARGE, highly segmented detectors are becoming more common in high-energy physics, synchrotron radiation research, and medical instrumentation. To process the signals from these detectors, a complex electronics chain is needed. The most flexible method of pulse processing is to digitize the signal directly after the low-noise preamplifier and anti-aliasing filter and to do the filtering, peak detection, and timing operations in the digital domain. However, a per-channel fully digital signal processing chain is impractical for most large multichannel systems.

Other systems need to concentrate the analog data before presenting it to the analog to digital converters (ADCs). Popular techniques include track-and-hold [see Fig. 1(a)] or switched-capacitor analog memory [see Fig. 1(b)]. The track-and-hold needs an accurately-timed trigger to sample the incoming pulse at its peak. Such a trigger is usually unavailable with X-ray detectors. Samples are then sequentially multiplexed to the ADC and during this time the circuit is unable to process new incoming pulses. When occupancy is low, most samples will contain only pedestal values, which are needlessly digitized. The analog memory approach suffers from the same drawbacks except that it can be made deadtimeless with sufficient extra buffer cells and a complex controller.

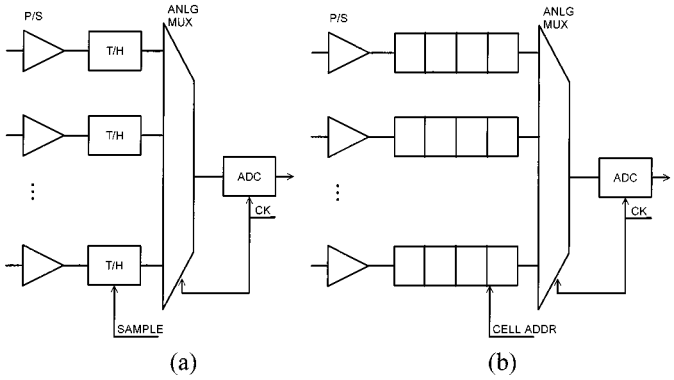

Fig. 1. Popular analog data concentration techniques. (a) The track-and-hold. (b) The switched-capacitor analog memory.

We have developed a readout system which is accurate, efficient and compact. It is self-triggered, self-sparsifying, derandomizing, deadtimeless and targeted at high-rate spectroscopy applications. The main building block of the system is an offset-free two-phase peak detect and hold (PDH) circuit implemented in submicron CMOS, which will be discussed in the next two sections.

II. Two-Phase Peak Detector

CMOS peak detectors employ an MOS current source as rectifying element in the feedback loop of a high-gain differential amplifier [1]–[4]. The major source of static error is the input offset $V_{\rm OS}$ of the differential amplifier [5]. The calibration of the consequent pedestal becomes unpractical in low-voltage submicron CMOS where, due to rail-to-rail configurations, the offset becomes a strong function of the input amplitude. Conventional techniques to reduce the offset unavoidably compromise speed and dynamic accuracy [5]. Therefore, until now, CMOS peak detectors have not been used for high-speed high-precision applications. In addition, the conventional configurations are characterized by limited dynamic range and poor driving capability.

We have developed a novel two-phase configuration that overcomes these limitations [6]. In the first phase [see Fig. 2(a)], the circuit is identical to the classical design. We label this the WRITE phase. The PMOS transistor M1 conducts while the input is increasing; after a positive peak it shuts off and the maximum value is stored on the hold capacitor C_H. The amplifier offset $V_{\rm os}$ corrupts the peak voltage $V_{\rm hold}$ stored on C_H. During the second phase [READ, Fig. 2(b)], the circuit

Manuscript received November 26, 2001; revised January 22, 2002. This work was supported by the U.S. Department of Energy under Contract DE-AC0298CH10886.

The authors are with the Instrumentation Division, Brookhaven National Laboratory, Upton, NY 11973 USA (e-mail: degeronimo@bnl.gov; anand@bnl.gov; poc@bnl.gov).

Digital Object Identifier 10.1109/TNS.2002.801701

0018-9499/02$17.00 © 2002 IEEE

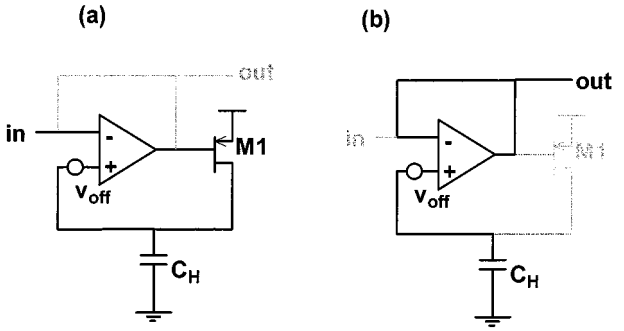

Fig. 2. Simplified schematic of the two-phase peak detector. (a) WRITE phase. (b) READ phase.

is reconfigured by analog switches (not shown) such that the amplifier acts as a unity-gain follower for the voltage $V_{\rm hold}$ held on C_H. The offset voltage $V_{\rm os}$ is now subtracted from the held peak value, thus canceling the error. The gate of M1, previously connected to the amplifier output, is now connected to the positive supply $V_{\rm DD}$.

It can be shown [6] that the total static error $V_{\rm out} - V_{\rm in,peak} = V_{e,\rm dc}$ of the two-phase configuration is given by

$$V_{\rm out} - V_{\rm in,peak} = V_{e,\rm dc} \approx \frac{V_{g,\rm peak} - V_{\rm in,peak}}{A_0} \qquad (1)$$

where $V_{g,\rm peak}$ is the gate voltage of M1 in proximity of the peak and A_0 is the dc voltage gain of the amplifier. The residual error (1) can be minimized by maximizing A_0. With the two-phase approach, the amplifier's finite common-mode rejection is also canceled. Due to the offset cancellation it is also possible to minimize the size of the input MOSFETs of the differential amplifier, disregarding any mismatch and consequent offset. In this way additional sources of error due to the MOSFETs gate capacitance are further minimized [6]. The circuit in the READ configuration also provides strong driving capability.

By sensing the voltage V_g at the gate of M1, the circuit can be made to switch automatically from the WRITE to the READ state. The peak detector is reset by shorting C_H. If we reset C_H to a threshold dc level other than ground, then the peak detector will only respond to peaks exceeding this threshold.

The circuit was fabricated in a 3.3 V, 0.35-μm CMOS DP-4M process. Detailed transistor level schematics can be found in [5] and [6]. The size of the layout of the analog and digital sections were 340×50 μm^2 and 245×50 μm^2, respectively. Semi-Gaussian pulses from an Ortec 672 shaping amplifier were input to the peak detector. Peaking times τ_p ranging from 0.2 to 15 μs and peak amplitudes ranging from 0.3 to 3 V were used.

In Fig. 3, the measured signals $V_{\rm in}$, $V_{\rm hold}$, $V_{\rm out}$, and $V_g/V_{\rm DD}$ from two different samples are shown. No averaging was used for these acquisitions. The input signal $V_{\rm in}$ (dot-dash) is a semi-Gaussian pulse with peak amplitude $V_{\rm in,peak} \approx 600$ mV and peaking time $\tau_p \approx 1.2$ μs. The circuit is reset at $t = 3$ μs.

Fig. 4 shows the difference between the output (held) voltage $V_{\rm out}$ and the true peak height $V_{\rm in,peak}$. For pulses with $\tau_p \geq 500$ ns, the absolute accuracy is better than 0.2% over a dynamic range extending to within 0.3 V of the supply rails. An integral linearity error better than 0.02% was also verified in the 0.5 V–2.5 V range for $\tau_p \geq 500$ ns. The analysis on the error in peak height as function of the peaking time is widely discussed in [5] and [6].

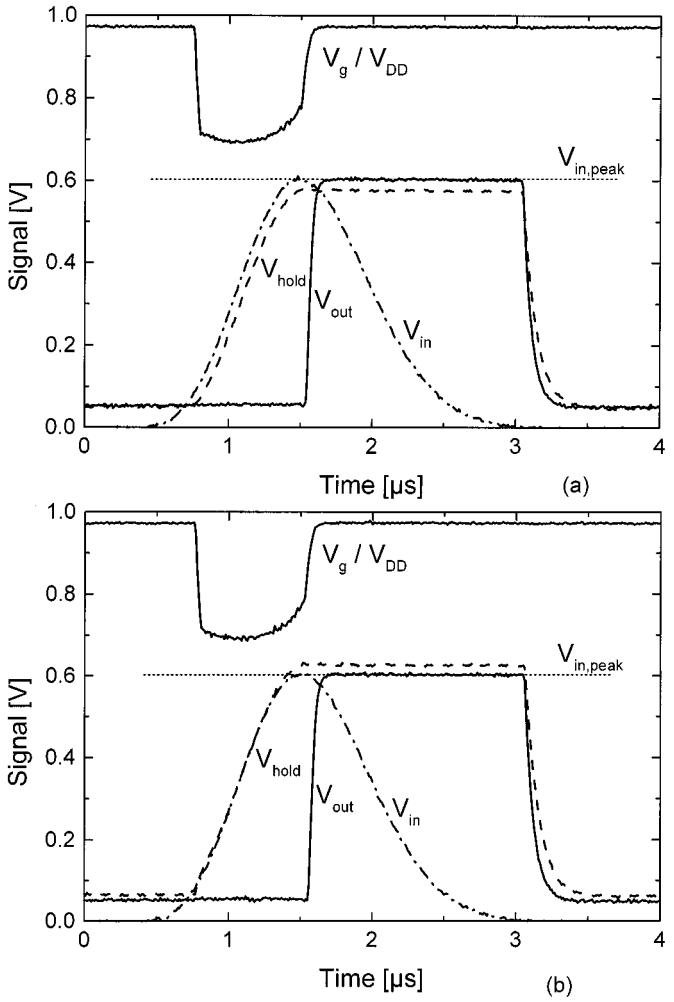

Fig. 3. Measured signals $V_{\rm in}$, $V_{\rm hold}$, $V_{\rm out}$, and $V_g/V_{\rm DD}$ from identical PDH circuits on two different chips. Note that the two circuits show opposite-sign offset errors at the hold node $V_{\rm hold}$, but that these errors are cancelled at the output $V_{\rm out}$.

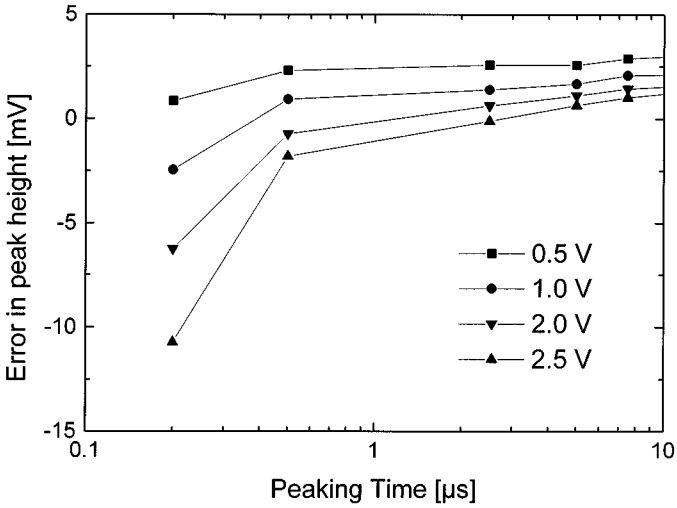

Fig. 4. Measured error of the two-phase peak detector, with semi-Gaussian input pulses of different amplitudes and peaking times.

By sensing the voltage V_g at the gate of M1, the circuit can also provide timing measurements relatively free of amplitude-dependent time walk since it effectively measures the zero-crossing of the derivative of the input pulse. The positive transition of the voltage V_g in correspondence of the peak, followed by a comparator, provides the required timing signal. In Fig. 5 the measured time walk for peak amplitudes ranging from 0.5 to 3 V and peaking times τ_p 200 and 500 ns is shown.

III. Peak Detector and Derandomizer (PDD)

A peak detect and hold circuit that can process and store several pulses in parallel providing the derandomization of times of arrival can greatly relax the requirements on the following ADC. The inherent high *absolute* accuracy of the two-phase PDH opens up the possibility of using several two-phase PDHs in parallel without adding the complexity of a separate and voltage dependent calibration for each PDH.

By combining the peak detection and analog storage functions of the PDH with suitable control logic, the PDD can be made to behave like a data-driven analog first input first output (FIFO). Ideally, it is possible to build a fully self-triggered, self-sparsifying, derandomizing, and deadtimeless readout system as shown in Fig. 6.

In Fig. 7, a simplified schematic of the PDD based on N copies of the two-phase PDH and one input line is shown. The concept can be extended to a version with multiple input lines and multidimensional switching for the processing of pulses form several channels. The block labeled *PDD Logic* keeps track of the next empty PDH and maintains an ordered list of occupied PDH cells awaiting readout.

When a new pulse arrives, it is detected and held on the storage capacitor of the nth peak detector (PDH-n). The PDD logic opens the input switch S_{in}, then selects the $n+1$st PDH available for input and closes the corresponding input switch $S_{\text{in}+1}$. In the mean time it stores the address in a N-deep readout FIFO. Up to N pulses can be processed and stored without requiring the readout.

When the ADC is ready to convert a value, the external logic sends a signal Vread to the PDD. The PDD logic selects the first PDH address from the readout FIFO and closes the corresponding output switch. Once the conversion is completed, the external logic sends a signal Vreset to the PDD, resetting the PDH and making it available for a further input processing.

While one PDH is being read out, another can accept input pulses. By choosing a large enough buffer size N, we can eliminate nearly all dead time while clocking the ADC at the average event rate.

In a more complex system, channel ID and timing information for every hit can be combined with the PDH address and stored in the readout FIFO. Then the data acquisition system can read amplitude, position, and time for every pulse.

A version of the PDD with $N = 2$ was realized in the 0.35-μm CMOS technology from TSMC. Preliminary test results are reported in [6].

Alternative possibilities are to construct a single two-phase PDH with multiple hold capacitors and suitable switches [see Fig. 8(a)], a single two-phase PDH with multiple output storing capacitors [see Fig. 8(b)] or, in general, a combination of more PDHs and multiple-capacitors elements.

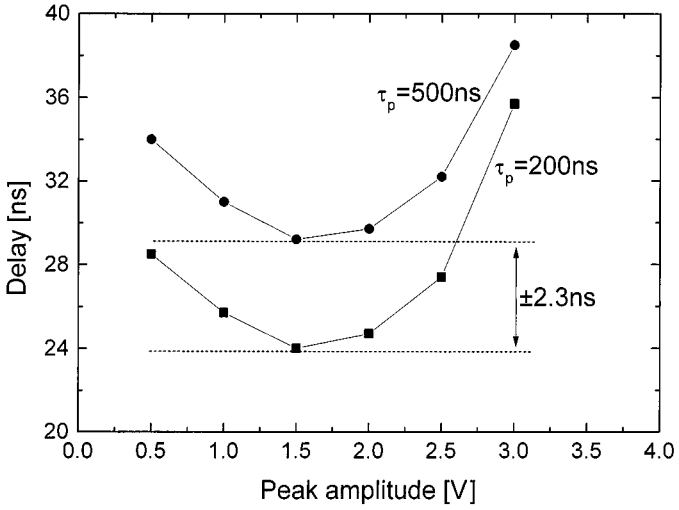

Fig. 5. Measured time walk as function of peak amplitudes for different peaking times.

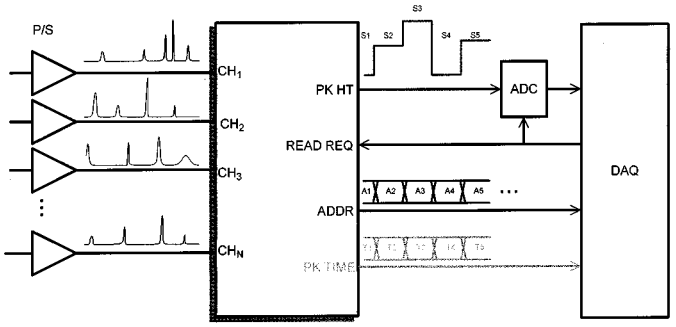

Fig. 6. Ideal self-triggered, self-sparsifying, derandomizing, and dead-timeless multichannel readout system.

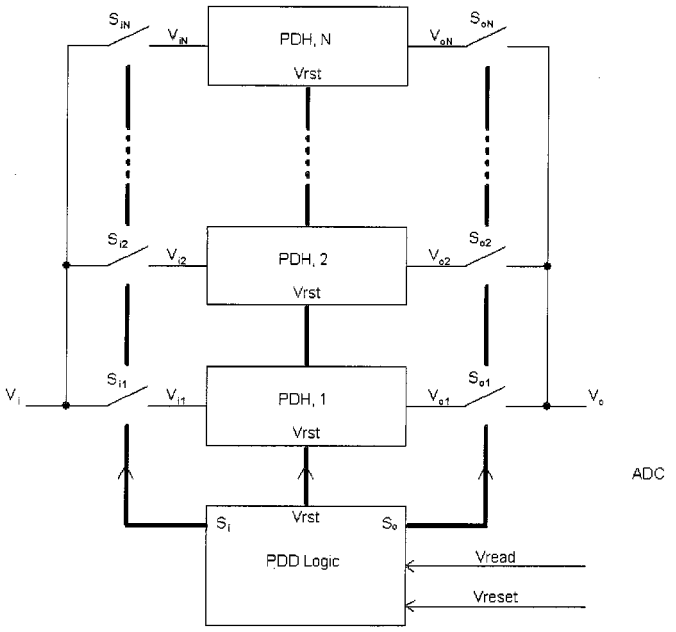

Fig. 7. Simplified schematic of the PDD for storing and derandomizing up to N samples.

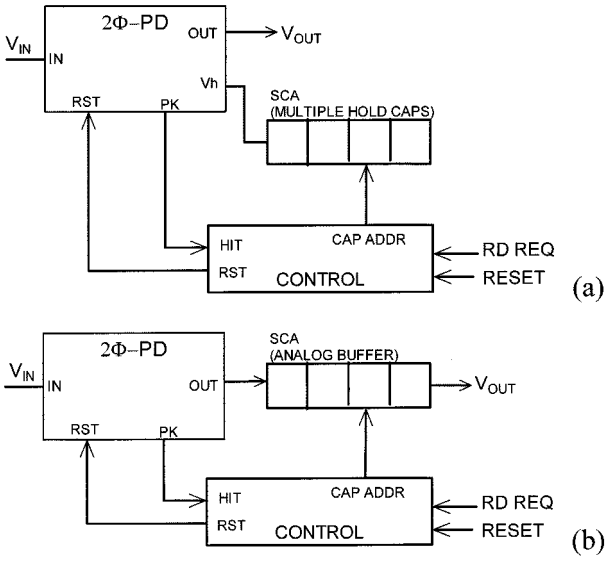

Fig. 8. Alternative possibilities include (a) single two-phase PDH with multiple hold capacitors and suitable switches and (b) single two-phase PDH with multiple output storing capacitors.

IV. Multichannel Readout System

To test the PDD with realistic signals the test system shown in Fig. 9 was constructed. A linear array of 32 CdZnTe (CZT) detectors on 3.5-mm pitch was exposed to ^{241}Am X-rays. Two 16-channel preamplifier/shaper ASICs [7] produced unipolar, 1.2-μs τ_p pulses, which were fed into a custom self-switched multiplexer (SSM).

The SSM chip, developed for an unrelated program, consists of a comparator bank, 32 : 1 switch matrix and arbitration logic. The SSM detects above-threshold inputs and routes them to the PDD input; it also presents the 5-bit address of the selected channel as output. The PDD generates a short pulse (PK_FND) whenever a new peak is detected. In response to a READ request from the data acquisition system (pulser), the next peak sample is presented to the 12-bit ADC. A logic analyzer captures the digital PEAK and corresponding channel ADDRess. After a fixed delay the pulser RESETs the PDD that was read out, making it available to process the next input pulse. The system shown in Fig. 9 consumes only about 0.8 mW per channel (excluding the preamp/shaper) and can fit into a PC board, less than 15 cm on a side.

Fig. 10 shows the waveforms PDD_IN, PK_FND, PDD_OUT, and READ for a typical acquisition. Note that the input pulses (and PK_FND signals) occur randomly, while the READ process is synchronous. The READ rate, 200 kHz in this example, is matched to the average input rate. Whenever a new READ is issued, PDD_OUT changes. It can be seen, for example, that the PDD detected and stored the third pulse before the second pulse was read out, demonstrating correct derandomization.

Note that the SSM/PDD combination efficiently concentrates the analog data before presenting it to the ADC. For example, eight peaks occur in the 50-μs waveform shown in Fig. 10, each peak coming from a different channel. Exactly eight samples are sent to the ADC, which can work at a constant rate of 200 kHz.

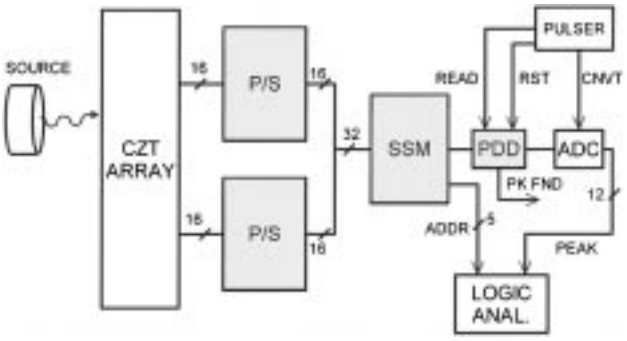

Fig. 9. Simplified block diagram of the multichannel readout system. Shaded blocks are custom CMOS ASICs.

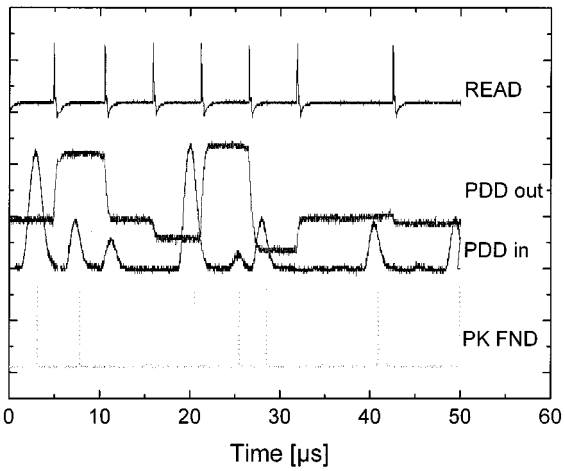

Fig. 10. Waveforms from the multichannel readout system demonstrating correct derandomization.

Let us contrast this to the other approaches outlined in Section I. In the fully digital approach [8], each channel would be equipped with an ADC. Each would need a sampling rate of at least 10 MHz to be able to extract an accurate peak value. During the 50-μs acquisition 32 000 samples would be digitized, but only about 20–30 would be used to extract the eight peak heights. The system would require several watts of power and consume a large board area.

With a track-and-hold scheme [9], it would be difficult to acquire the eight peaks shown in Fig. 10. First, there is no simple way to derive a trigger from the X-rays. Second, the 32 : 1 analog multiplexer could not run fast enough to keep up with the event rate. The fastest analog multiplexer with 12-bit accuracy can only be clocked at about 5 MHz; thus, readout of 32 channels would result in 6.4 μs of deadtime and most of the pulses in Fig. 10 would be blocked.

An analog memory [10] to capture all the peaks shown in Fig. 10 would need several hundred cells per channel and triggering would again be problematic. Without a trigger the entire array would need to be read out and digitized, again resulting in tens of thousands of samples to find only eight pulses.

Fig. 11 displays the source intensity profile determined from the ADDR output of the SSM.

In Fig. 12, we compare the ^{241}Am spectrum of one channel recorded by a commercial MCA and the spectrum collected by

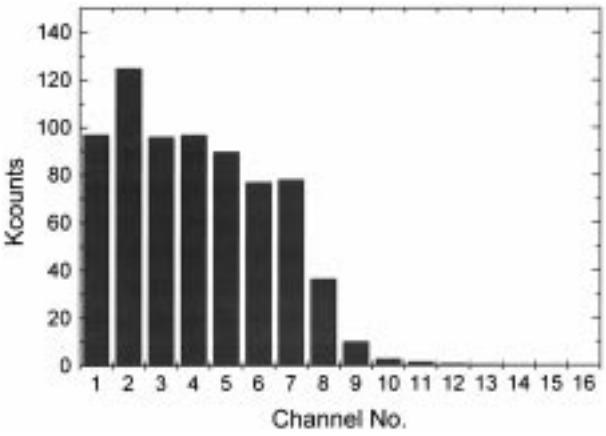

Fig. 11. Source intensity profile. Source is centered over channel 2.

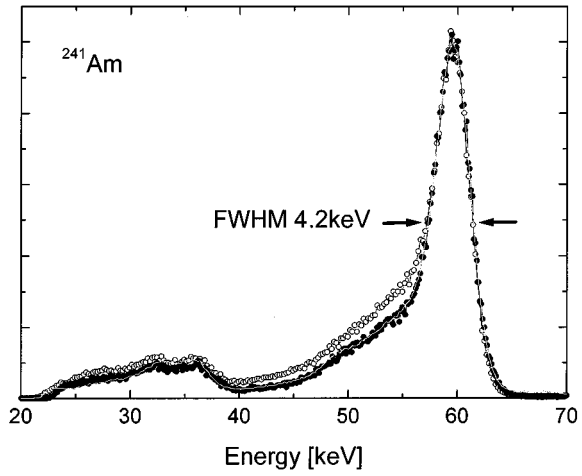

Fig. 12. Spectrum of ^{241}Am. Solid line: commercial MCA. Points: PDD system, single channel. Circles: PDD system, all channels gain adjusted.

this system. Resolution is limited by the CZT detectors used; electronics noise is less than 2 keV. Noise of the peak detector alone is less than 0.03% of full scale.

V. Conclusion

We have developed a compact two-phase peak detector in submicron CMOS that has high absolute accuracy and linearity, rail-to-rail sensing, and a precision timing output. This peak detector has been used as the basis of an efficient multichannel readout system which is self-triggered, self-sparsifying, and nearly deadtimeless. The peak detector-derandomizer (PDD) with a two-event buffer has been used to demonstrate the first step toward a data-driven analog FIFO readout with application to spectroscopy and matrix detectors.

Acknowledgment

The authors would like to thank V. Radeka [Brookhaven National Laboratory (BNL), Upton, NY] and A. Hrisoho [Laboratoire de L'Accelerateur Lineaire (LAL)], Orsay, France) for help and encouragement with this project and J. Triolo (BNL) for technical assistance. They would also like to thank J. Grosholz and F. Ferraro of eV Products, Division of II-VI, Inc., for the support in the development of the SSM chip.

References

[1] M. W. Kruiskamp and D. M. W. Leenaerts, "A CMOS peak detect sample and hold circuit," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 295–298, Feb. 1994.

[2] M. N. Ericson, M. L. Simpson, C. L. Britton, M. D. Allen, R. A. Kroeger, and S. E. Inderhees, "A low-power, CMOS peak detect and hold circuit for nuclear pulse spectroscopy," *IEEE Trans. Nucl. Sci.*, vol. 42, pp. 724–728, Aug. 1995.

[3] C. Fiorini, A. Pullia, P. Novellini, E. Gatti, A. Longoni, and W. Buttler, "A monolithic implementation of a switched-current wheel amplifier for multichannel silicon drift detectors," *IEEE Trans. Nucl. Sci.*, vol. 46, pp. 161–165, June 1999.

[4] U. Jagadish, C. L. Britton Jr., M. N. Ericson, W. L. Bryan, W. G. Schwarz, M. E. Read, and R. A. Kroeger, "A preamplifier-shaper-stretcher integrated circuit system for use with Germanium strip detectors," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 1868–1871, Dec. 2000.

[5] G. De Geronimo, A. Kandasamy, and P. O'Connor, "On the analog CMOS peak detect and hold circuit—Part 1: Analysis of the classical configuration," Nucl. Instrum. Methods.

[6] ——, "Analog CMOS peak detect and hold circuits—Part 2: Offset-free rail-to-rail and derandomizing configuration," Nucl. Instrum. Methods.

[7] G. De Geronimo, P. O'Connor, and J. Grosholz, "A generation of CMOS readout ASIC's for CZT detectors," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 1857–1867, Dec. 2000.

[8] A. Pullia, A. Geraci, and G. Ripamonti, "Quasioptimum γ and X spectroscopy based on real-time digital techniques," *Nucl. Instrum. Methods*, vol. A439, pp. 378–384, 2000.

[9] M. Overdick, A. Czemak, P. Fischer, V. Herzog, A. Kjensmo, T. Kugelmeier, K. Ljunggren, E. Nygård, C. Pietrzik, T. Schwan, S. E. Strand, J. Straver, P. Weilhammer, N. Wermes, and K. Yoshioka, "A bioscope system using double-sided silicon strip detectors and self-triggering read-out chips," *Nucl. Instrum. Methods*, vol. A392, pp. 173–177, 1997.

[10] T. Zimmerman, T. Huffman, J. Srage, R. Stroehmer, R. Yarema, M. Garcia-Sciveras, L. Luo, and O. Milgrome, "SVX3: A deadtimeless readout chip for silicon strip detectors," *Nucl. Instrum. Methods*, vol. A409, pp. 369–374, 1998.