Front-End ASIC for Co-Planar Grid Sensors

Gianluigi De Geronimo, Gabriella Carini, William S. Murray, and Paul O'Connor

***Abstract*—An Application Specific Integrated Circuit for Cadmium Zinc Telluride Co-Planar Grid sensors is presented. The ASIC provides low-noise amplification of grids and cathode signals, difference between grid signals with adjustable relative gain, shaped signals with baseline stabilization, and timing signals. In the current version the peaking time of the shaped pulses is 5 μs and the gain can be switched between 36 mV/fC and 18 mV/fC covering an energy range up to 3 MeV. Designed in CMOS 0.25 μm technology it dissipates 25 mW from a single $+2.5$ V supply. A description of the ASIC and the results of its characterization with CdZnTe CPG sensors are presented. The system is analyzed in terms of resolution, and the impact of the noise correlation due to the inter-grid capacitance is discussed.**

***Index Terms*—ASIC, Co-Planar Grid, noise correlation.**

I. Introduction

THE CO-PLANAR Grid (CPG) sensing technique has been successfully combined with recent advances in Cadmium Zinc Telluride (CZT) manufacturing, resulting in large-volume high-resolution room-temperature gamma-ray spectrometers. Due to their efficiency and compactness the CPG sensors are being considered in an increasing number of applications, ranging from nuclear material safeguard to radioisotope identification in security and defense, environmental remediation, well logging, medical diagnostics, and gamma-ray astronomy [1]–[4].

By subtracting the signals from two co-planar inter-digitized grid electrodes (collecting grid and noncollecting grid) the CPG becomes sensitive to electrons only, overcoming the limit of poor holes mobility typical of the CdZnTe material. In order to compensate for the residual electron trapping, two techniques were proposed. The first consists of lowering below 1 the gain G of the noncollecting grid relative to that of the collecting grid [5]. The second consists of keeping $G = 1$ and weighting each event by measuring its depth of interaction through simultaneous processing of grids and cathode signals [6].

The availability of a front-end application specific integrated circuit (ASIC) capable of amplifying and suitably processing the signals from CPG sensors is attractive, especially in developing portable and battery-operated detection systems. The ASIC presented here serves this purpose, providing simultaneous low-noise amplification of grids, difference and cathode signals, adjustable relative gain, and timing signals.

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II. ASIC Architecture

In Fig. 1, the block diagram of the ASIC is shown. It implements three front-end channels. Two channels provide amplification and processing of the two grids signals (collecting and noncollecting). One channel provides amplification and processing of the cathode signal.

The grid electronics is composed of two low-noise charge amplifiers followed by a difference amplifier. The charge amplifiers have n-channel input MOSFETs and are based on the dual-stage charge gain circuits described in [7] where the first stage is the older configuration [7, Fig. 3] with gain equal to 16 and the second stage is the newer configuration [7, Fig. 4] with gain adjustable to 3 or 6. Before entering the difference amplifier, each signal goes through an additional circuit, not shown in Fig. 1, which realizes the first pole of the shaper [7]. Three additional buffers make available the two unshaped signals (after the first pole) and their difference to dedicated outputs.

In Fig. 2, a detail of the difference amplifier is shown. The relative gain G can be adjusted through a combination of switches (S1, S2, and S3) and an external resistor R_x following the equation

$$G = \frac{35k}{50k}\left(1+\frac{50k}{35k}\right)\frac{R_i//(20k+R_x)}{35k+R_i//(20k+R_x)} \qquad (1)$$

where R_i is the resistance seen between nodes a and b and resulting from the combination of S1 and S2.

If the switch S3 is open the relative gain G equals 1, 0.6 and 0.5 when respectively, S1, S2, and S1+S2 are closed. If the switch S3 is closed, the relative gain G depends on the value of the external resistor R_x, as shown in Fig. 3. It is also possible to disable the noncollecting channel providing an effective relative gain $G = 0$. The difference signal feeds a comparator with externally controllable threshold, thus generating the corresponding timing signal.

The cathode electronics is composed of a low-noise charge amplifier followed by a shaping amplifier. The charge amplifier has an n-channel input MOSFET and is based on the dual-stage charge gain circuits as in the grid case, with the two configurations inverted due to the opposite polarity of the collected charge [7]. A comparator provides the timing of the cathode signals, while a buffer makes the unshaped signal (after the first pole) available to a dedicated output.

In both cases, the shaping is a fifth-order with complex conjugate poles [8] and band-gap referenced (BGR) baseline stabilizer (BLH) [9]. In Fig. 4, the schematic of the shaping amplifier

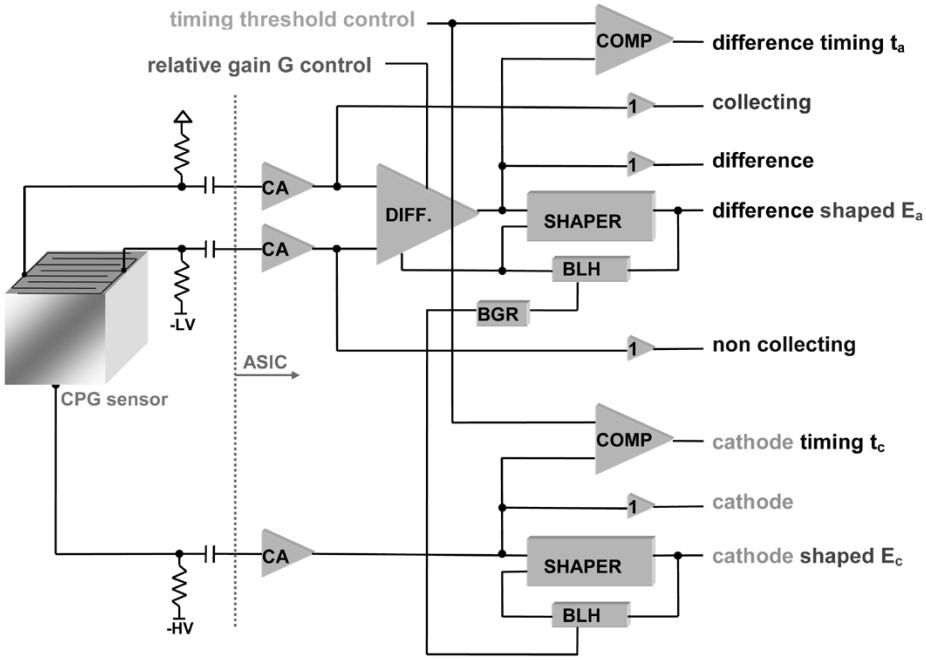

Fig. 1. Block diagram of the ASIC.

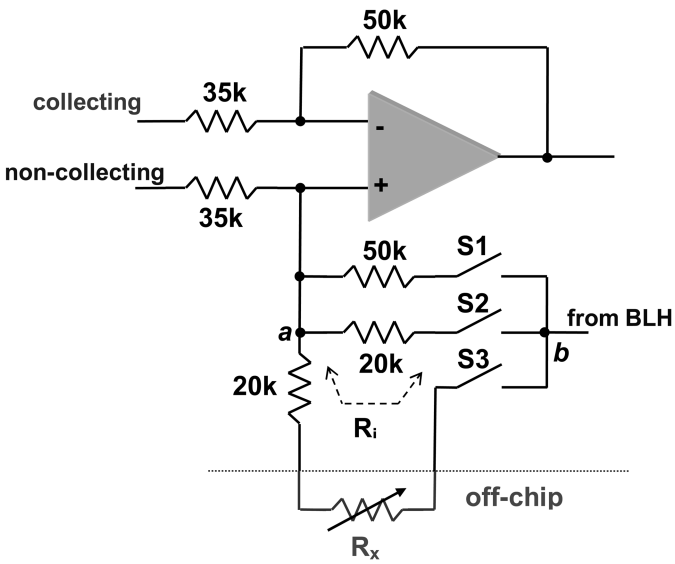

Fig. 2. Schematic of the difference amplifier.

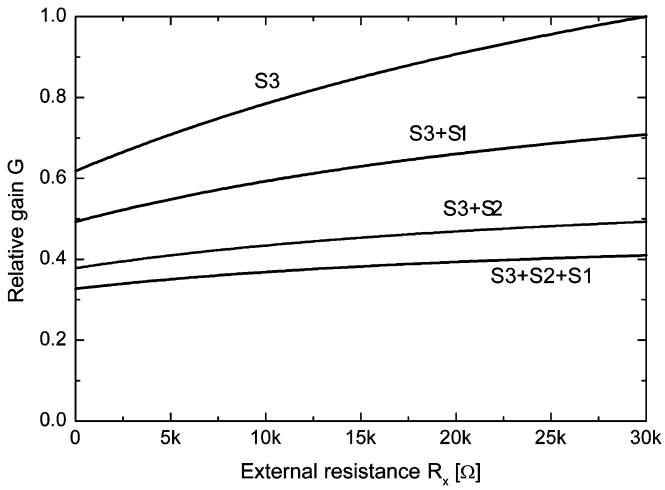

Fig. 3. Relative gain versus external resistance and switches settings (Si indicates that the ith switch is closed.

is shown. As previously discussed, the first pole is actually localized right after the charge amplifier circuit, before the buffer. In this ASIC version, the peaking time is set to 5 μs.

Each channel implements a 500 fF test capacitor which can be externally enabled through dedicated switch. The gain can be switched between 36 mV/fC and 18 mV/fC in order to cover an energy range up to 3 MeV. The total dissipated power is 25 mW from a single +2.5 V supply. The technology is TSMC 0.25 μm and the layout size (shown in Fig. 5) is 3.1×3.1 mm^2.

III. Noise Analysis

The dual-channel electronics for the grid signals requires a dedicated noise analysis. In Fig. 6, a schematic for the evaluation of the equivalent noise charge (ENC) is shown, where S_a, S_g, and S_{ig} are the power spectral densities associated with the respective noise generators. C_a and S_a are the input capacitance and the noise spectral density of charge amplifier. $S_g \approx 2qI_g + 4kT/R_g$ is the spectral density associated with the CPG bulk current I_g and the bias resistor R_g of each grid. $S_{ig} \approx \alpha 2qI_{ig}$ is associated with the inter-grid current component I_g, while C_g and C_{ig} are the grid plus interconnects capacitance and the inter-grid capacitance respectively. Q is the charge released by the sensor and, due to the way the CPG operates, it can be represented as a single generator at input of the collecting grid.

The schematic in Fig. 6 can be easily transformed into the one in Fig. 7, where the correlation between the equivalent noise generators due to C_{ig} and S_{ig} is taken into account.

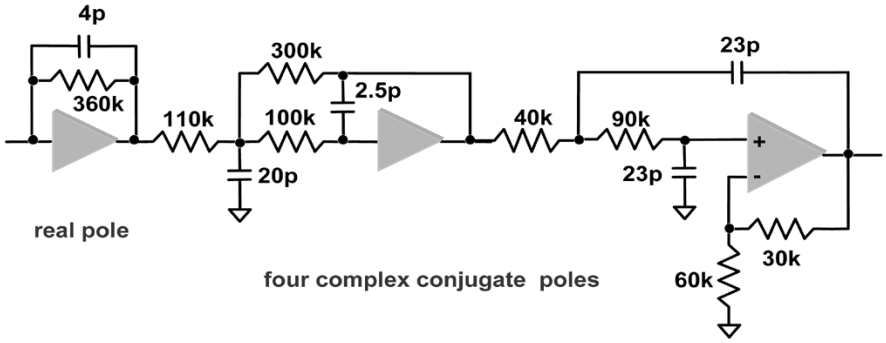

Fig. 4. Schematic of the shaping amplifier. The peaking time is set to 5 μs.

In Fig. 7, $C_T = C_a + C_f + C_g + C_{ig}$ is the total input capacitance. Following Fig. 7, the ENC can be written as

$$\begin{aligned}\mathrm{ENC}^2 = &\left[(C_T + C_{ig}G)^2 + (C_T G + C_{ig})^2\right] \\ &\times \left(\frac{a_w}{\tau_p} S_a + 2\pi a_f A_f\right) \\ &+ \tau_p a_p \left[S_g\left(1+G^2\right) + S_{ig}\left(1+G\right)^2\right] \end{aligned} \quad (2)$$

where S_w and A_f/f are, respectively, the white and $1/f$ noise component of the amplifier noise spectrum S_a, and a_w, a_f, and a_p are coefficients related to the shaper [10]. In the limit for $G = 0$ and $G = 1$, it follows, respectively,

$$\begin{aligned}\mathrm{ENC}^2 = &\left[(C_a + C_g + C_{ig})^2 + C_{ig}^2\right]\left(\frac{a_w}{\tau_p} S_a + 2\pi a_f A_f\right) \\ &+ S_g \tau_p a_p \end{aligned} \quad (3a)$$

$$\begin{aligned}\mathrm{ENC}^2 \approx &2\left(C_a + C_g + 2C_{ig}\right)^2 \left(\frac{a_w}{\tau_p} S_a + 2\pi a_f A_f\right) \\ &+ 2S_g \tau_p a_p. \end{aligned} \quad (3b)$$

In (3) we assumed $C_f \ll C_T$ and, in agreement with the results reported in [11]–[13], the last term was neglected ($\alpha \ll 1$). Since in CPG sensors C_{ig} can be on the order of tens of pF, it may easily dominate compared to the other capacitive terms. It can be observed that the increase in the ENC component related to the series noise when the system operates in dual channel, when compared to the single channel, is not limited to $\sqrt{2}$. It can actually go from $\approx \sqrt{2}$ for $G = 0$ up to $\approx 2\sqrt{2}$ for $G = 1$. The increase in the ENC component related to the parallel noise remains ≈ 1 for $G = 0$ and $\approx \sqrt{2}$ for $G = 1$.

With regards to the second compensation method described in Section I and based on the measurement of the depth of interaction, it might be of interest a comparison between the energy ratio approach and the timing difference approach. In the first case the ratio between the cathode energy and the difference energy is measured. In the second case the delay from the difference timing to the cathode timing is measured. In both cases the result is related to the depth of interaction, but the resolution may be different. Concerning the first approach, the r.m.s. noise σ_{D1} on the measurement of the depth D can be approximated with

$$\sigma_{D1} \approx \frac{D_{\max}}{V_D}\sqrt{\sigma_{VC}^2 + \sigma_{VC}^2 \frac{V_C}{V_D}} \quad (4)$$

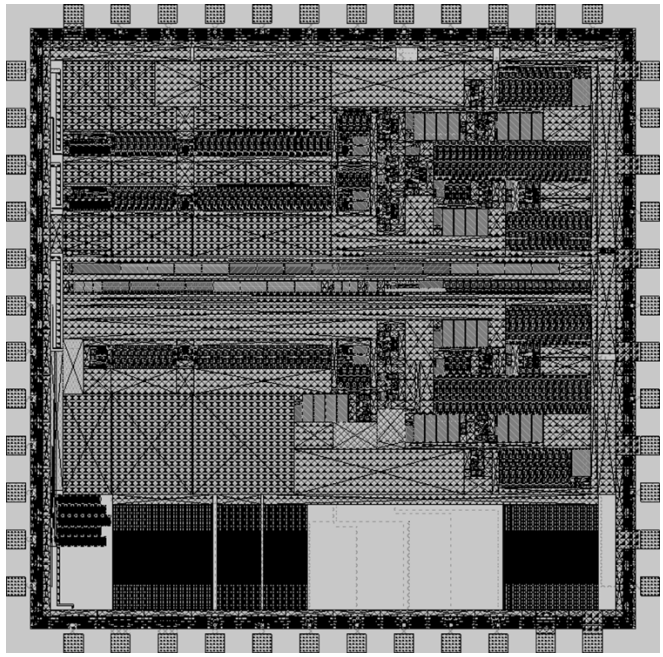

Fig. 5. ASIC layout in TSMC 0.25 μm. The size is 3.1 × 3.1 mm^2.

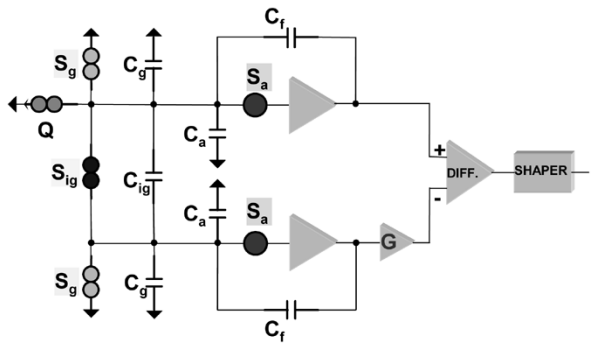

Fig. 6. Schematic of the dual channel electronics for the grid signals, where the components relevant to the evaluation of the ENC are shown.

where $D_{\max}$ is the thickness of the sensor, σ_{VC} and σ_{VD} are respectively the r.m.s. noise of cathode and difference signals, and V_C and V_D are the amplitudes of cathode and difference signals. Concerning the second approach, by taking into account that the slope of the cathode signal, being related to the electrons

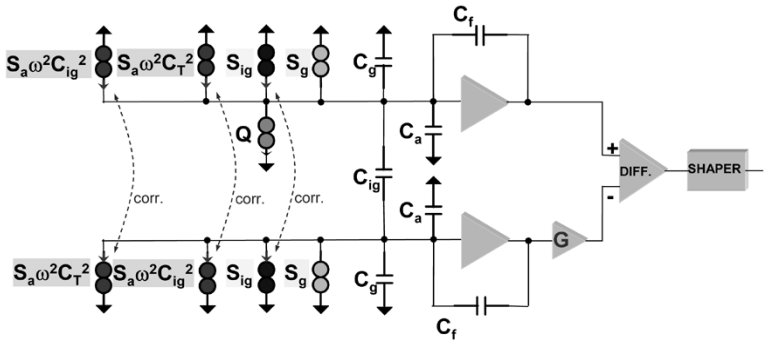

Fig. 7. Schematic of the dual channel electronics for the grid signals, where the components relevant to the evaluation of the ENC are rearranged taking into account the correlation.

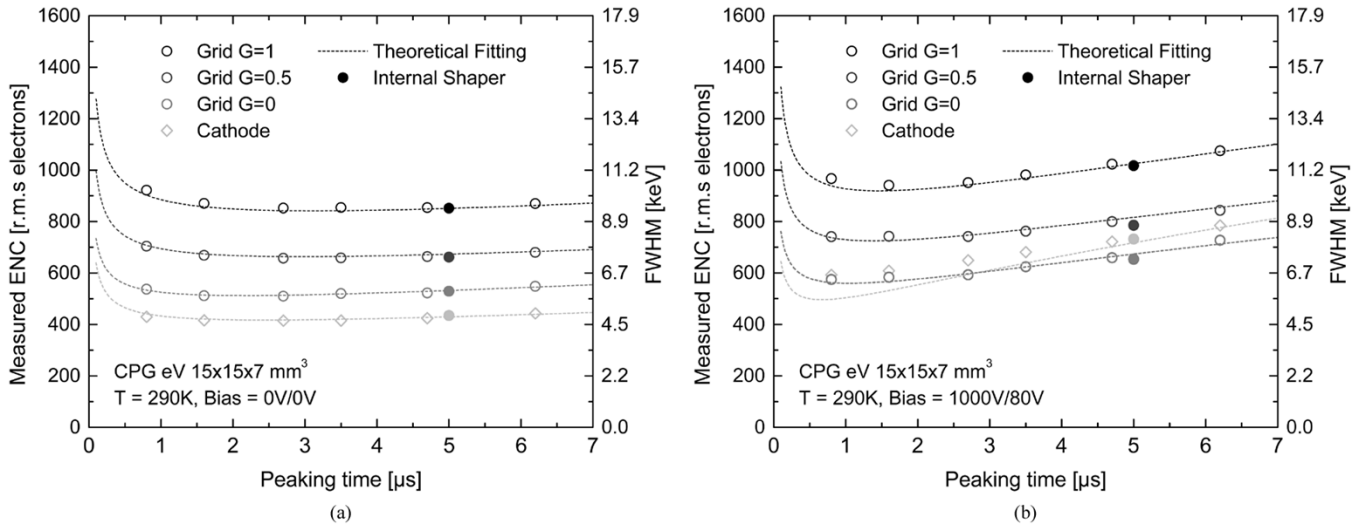

Fig. 8. ENC measurements on the ASIC with the CPG sensor connected and (a) not biased; (b) biased.

traveling in the bulk, is independent of the amplitude, the r.m.s. noise in the measurement can be approximated with

$$\sigma_{D2} \approx D_{\max} \frac{\sigma_{VD}}{V_D} \tag{5}$$

where the term due to the difference signal, characterized by a high slope, was neglected.

A comparison between (4) and (5), along with the ballistic deficit associated with the measurement of the cathode energy, suggest that the second approach may offer better resolution. In addition, if the timing is performed on the grid signals only (e.g., collecting and difference), the depth of interaction can be measured without information from the cathode, with consequent benefits in terms of complexity, power, and real estate.

IV. First Experimental Results

The ASIC was characterized with a $15 \times 15 \times 7$ mm^3 CdZnTe CPG sensor from eV-Products (II–VI Inc.). In Fig. 8(a), measurements of the ENC versus peaking time with the CPG sensor connected to the ASIC and unbiased are shown for the cathode and grid difference with $G = 0$, 0.5, and 1. The measurements with the internal shaper are also shown.

In our case, $C_g \approx 10$ pF, $C_{ig} \approx 14$ pF, $R_g \approx 22$ MΩ. The increase in ENC from $\approx 500e^-$ at $G = 0$ to $\approx 900e^-$ at $G = 1$ confirms the noise correlation discussed in previous section. The

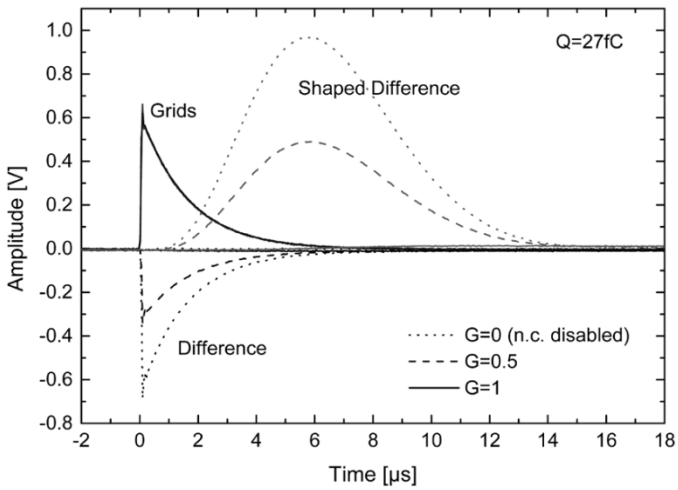

Fig. 9. Measured ASIC response to $Q = 27$ fC for $G = 0$, 0.5 and 1.

ENC of the ASIC, limited to the series noise component, can be roughly approximated with

$$\mathrm{ENC}_{\mathrm{series}} \approx \sqrt{1+G^2}\left\{300 + \frac{7}{\mathrm{pF}} \times \left[C_g + C_{ig}\left(1+G\right)\right]\right\}. \tag{6}$$

In Fig. 8(b), the same measurements of the ENC versus peaking time with the CPG sensor connected and biased at

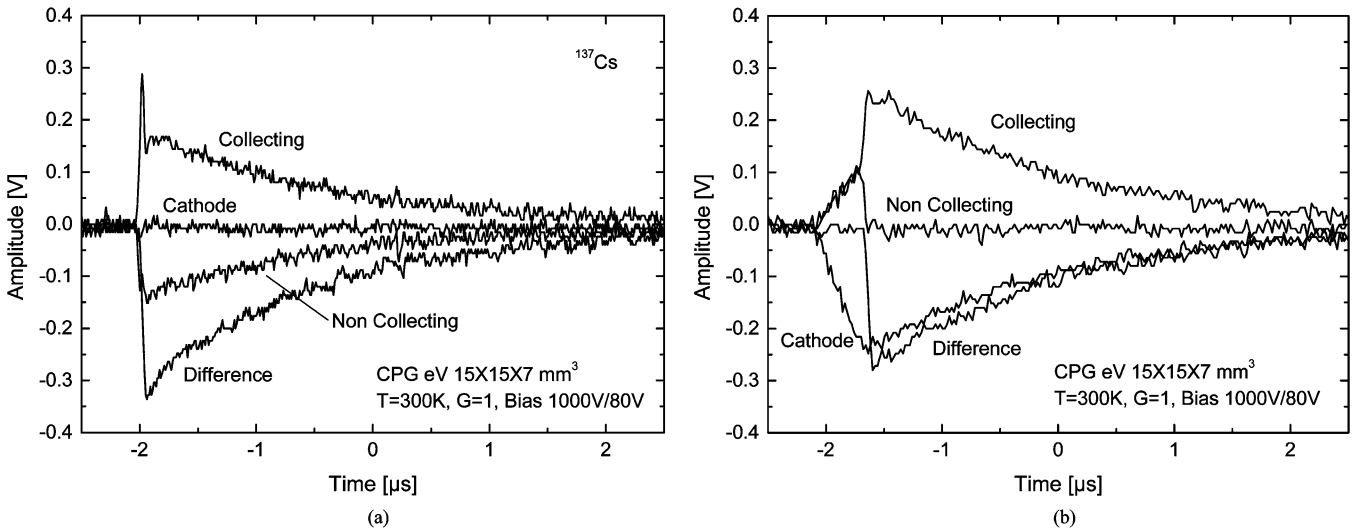

Fig. 10. Measured ASIC-CPG unshaped responses to a ^{137}Cs source with $G = 1$ for an interaction (a) close to grid and (b) close to cathode.

1000 V/80 V (cathode/difference) are shown. Also in this case the measurements with the internal shaper are shown.

In our case $I_g \approx 6$ nA was extracted, in agreement with a measured cathode leakage around 12 nA at 290 K while I_{ig}, measured in the range of tens of nA, contributed to the noise in negligible amount in agreement with the results in [11]–[13]. The cathode ENC at shorter peaking times with sensor biased was higher than expected and needs further investigation.

In Fig. 9, the measured collecting, noncollecting, difference and shaped responses to a charge $Q = 27$ fC injected through test capacitors are shown for the cases $G = 0, 0.5$, and 1. An integral linearity error below $\pm 0.25\%$ for energies up to 1.5 MeV (3 MeV for lower gain setting) was measured.

In Fig. 10, the unshaped responses of the ASIC-CPG to a ^{137}Cs source for (a) interaction close to grid and (b) interaction close to cathode are shown. When the interaction is close to the grid, the cathode signal has low amplitude and the delay from the interaction to the difference signal is negligible. When the interaction is close to the cathode the cathode signal has high amplitude and a time delay from the interaction to the difference signal, due to the transit time of the electrons, can be observed (about 400 ns in this case).

In Fig. 11, the unshaped and shaped responses of the ASIC-CPG to a ^{137}Cs source are shown. Difference and cathode shaped signals can be used for the measurements of the depth of interaction [6].

In Fig. 12, the unshaped and timing responses of the ASIC-CPG to ^{137}Cs signals for (a) interaction close to grid and (b) interaction close to cathode are shown. The delay from the cathode timing (time of interaction) to the grid timing can be used as an alternative method for the measurement of the depth of interaction.

In Fig. 13(a), the spectrum from a ^{137}Cs source is shown. The spectrum was measured at $T = 290$ K using the first compensation technique described in [5, Section I]. A FWHM $\approx$ 16 keV ($\approx 2.4\%$) at 662 keV was measured with $G \approx 0.86$. Fig. 13(b) shows the FWHM versus the relative gain G, measured at $T = 300$ K, on the 662 keV peak of ^{137}Cs and on the

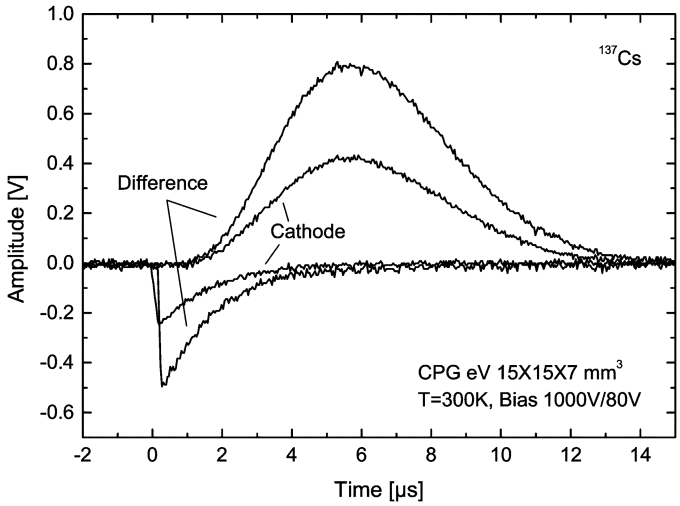

Fig. 11. Measured ASIC-CPG shaped and unshaped responses to a ^{137}Cs source with $G = 1$.

peak from the test pulse. This result is in qualitative agreement with the one reported in [5].

V. Conclusions and Future Work

An ASIC for CPG sensors is being developed. Noise analysis has shown that, due to the correlation associated with the inter-grid capacitance, the series noise contribution form the front-end electronics can be relevant. This problem will be addressed in a next version of the ASIC by replacing the n-channel input MOSFET with a p-channel, characterized by a lower series noise in the frequency range of interest [10]. Measurements with a CPG sensor have been carried out by using the relative gain compensation technique giving results in qualitative agreement with [5]. The characterization of the ASIC-CPG system using the compensation based on the measurement of the depth of interaction is in progress, and the two techniques of difference/cathode amplitude ratio and difference-cathode delay will be compared. For the second technique, the timing from the collecting grid

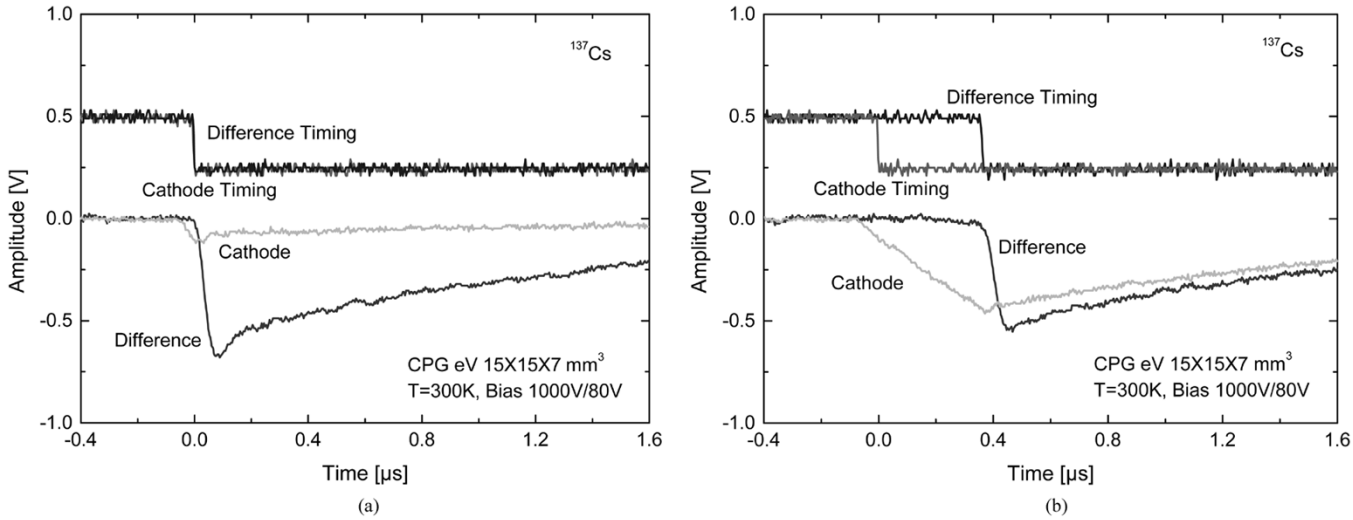

Fig. 12. Measured ASIC-CPG unshaped and timing responses with $G = 1$ to ^{137}Cs signals for an interaction (a) close to grid and (b) close to cathode.

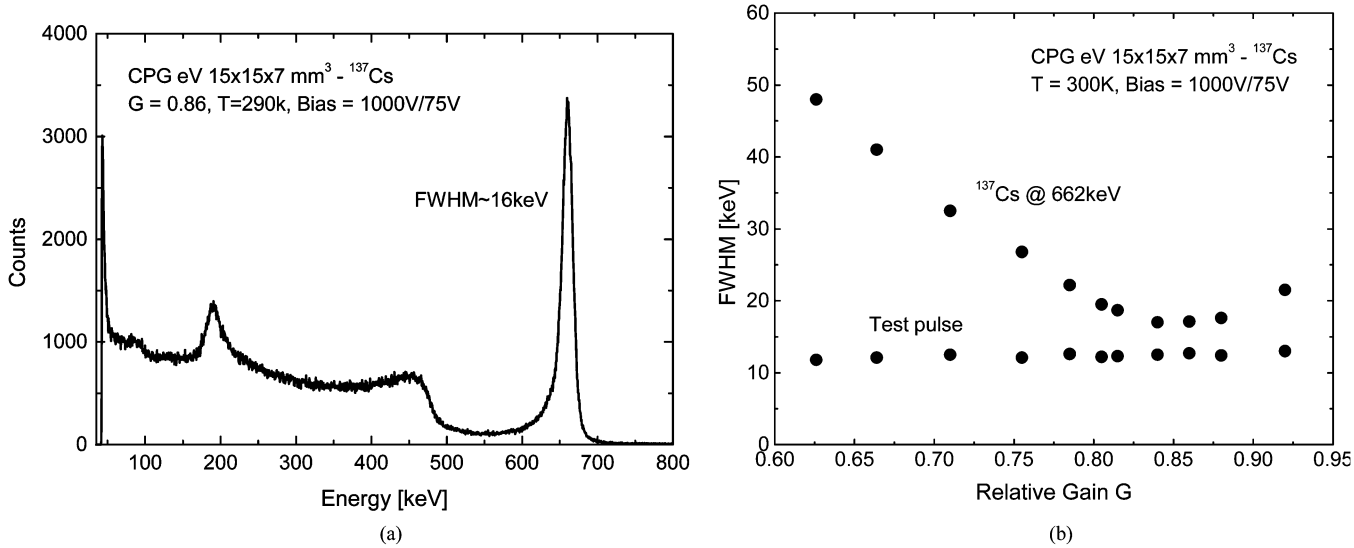

Fig. 13. Spectral measurements using the gain based compensation technique: (a) spectrum from a ^{137}Cs source with $G \approx 0.86$ and (b) FWHM versus G on the 662 keV peak and on the peak from the test pulse.

will be considered as an alternative to the one from the cathode signal.

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