Readout ASIC for 3D Position-Sensitive Detectors

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***Abstract*—We describe an application specific integrated circuit (ASIC) for 3D position-sensitive detectors. It was optimized for pixelated Cadmium–Zinc–Telluride (CZT) sensors, and it measures, corresponding to an ionizing event, the energy and timing of signals from 121 anodes and one cathode. Each channel provides low-noise charge amplification, high-order shaping, along with peak- and timing-detection. The cathode's timing can be measured in three different ways: the first is based on multiple thresholds on the charge amplifier's voltage output; the second uses the threshold crossing of a fast-shaped signal; and the third measures the peak amplitude and timing from a bipolar shaper. With its power of 2 mW per channel the ASIC measures, on a CZT sensor connected and biased, charges up to 100 fC with an electronic resolution better than 200 e^- rms. Our preliminary spectral measurements applying a simple cathode/anode ratio correction demonstrated a single-pixel resolution of 4.8 keV (0.72 %) at 662 keV, with the electronics and leakage current contributing in total with 2.1 keV.**

***Index Terms*—Application specific integrated circuit (ASIC), Cadmium–Zinc–Telluride (CZT), 3D, timing.**

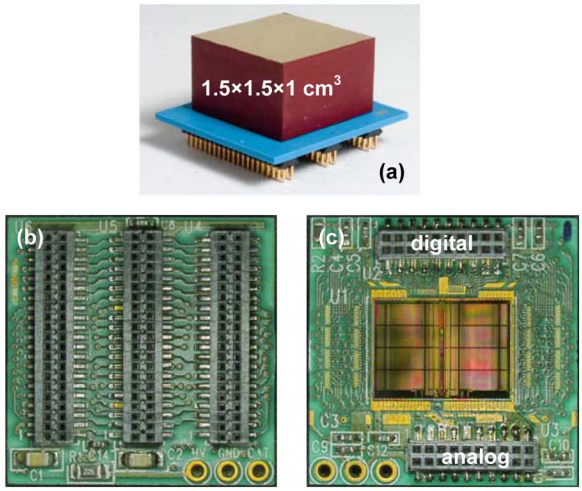

Fig. 1. Sample of (a) 121 anodes pixelated CZT sensor; interposer (b) back view and (c) front (ASIC) view.

I. Introduction

CADMIUM–ZINC–TELLURIDE (CZT) sensors have emerged as leading candidates in room-temperature, large-volume gamma-ray spectrometry for security-, medical-, industrial-, and space-applications [1]–[7]. More recently another wide-bandgap material, mercuric iodide (HgI_2), was suggested as potential candidate [8]–[10]. Both materials can be produced with relatively low dark current, but their spectral resolution is strongly limited by several deficiencies like poor mobility of holes, electron trapping, and extensive non-uniformities. Accordingly, various solutions were proposed that link suitable electrode configurations with bi-parametric signal correction [11], [12], [36], [13]–[19].

The 3-D Position-Sensitive Detector (3DPSD) [20]–[22] combines the pixelation of the anode electrode with the measurement of amplitude and timing. This information is used to reconstruct the position of the ionizing interaction, and to correct the measurement on a voxel-by-voxel basis (voxel stands for volumetric pixel), thus compensating for the deficiencies. With this approach, were registered energy resolutions better than 1% FWHM at 662 keV in CZT, limited only by the resolution of the readout electronics. Additionally, employing the 3D correction method allows the use of lower-grade and larger size detectors in a larger number of applications.

We developed an application specific integrated circuit (ASIC) for 3D position-sensitive detectors. The ASIC provides low-noise charge amplification, filtering, and measurements of amplitude and timing on signals from the cathode and 121 anodes.

In Section II, we introduce the architecture of the ASIC, and discuss some new circuit configurations. Section III describes methods for the timing measurements, wherein an innovative approach consists of applying a bipolar shaping to the cathode signal. Section IV reports our first experimental results.

II. Architecture of the ASIC

The ASIC was designed to read-out the signals from pixelated CZT sensors similar to that in Fig. 1(a), characterized by 11×11 (121) anodes and one cathode. In correspondence to an ionizing event, the ASIC measures the peak amplitude and relative timing from each of these 122 electrodes. It also provides an analog charge-amplifier monitor for the cathode and for the anode-grid signals. Reading out the anode signals entails negative-charge amplification, while that from the cathode and anode-grid requires the opposite.

The ASIC is wire-bonded to a 22×22 mm^2 interposer (Fig. 1) that includes on one side three sockets [Fig. 1(b)], for the CZT sensor's connection, and, on the other side, two sockets [Fig. 1(c)], for the analog- and digital-supplies and signals. The ASIC inputs are symmetrically located along its left and right sides, the analog outputs and supplies are at the bottom, while

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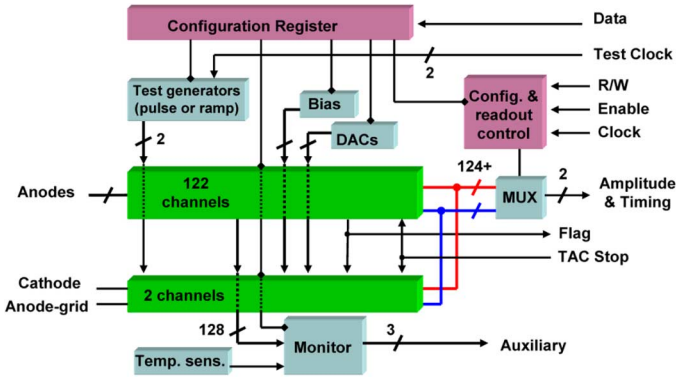

Fig. 2. Block diagram of the ASIC.

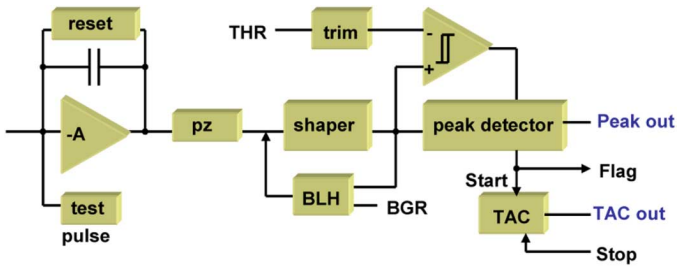

Fig. 3. Block diagram of the anode channel.

the digital signals and supplies are at the top. The three large holes at the bottom of the interposer are for the connection of the cathode signal and for the bias of the anode-grid (≈100 V). The cathode's bias circuitry, not shown, is placed close to the cathode electrode. The interposer is connected to a mother board that assures a regulated supply and can accommodate nine interposers in a 3×3 configuration.

Fig. 2 is a block diagram of the ASIC that comprises 124 channels (122 read-out negative charge, two read-out positive), bias circuitry, six 10-bit DACs, two test-signal generators, one temperature sensor, configuration register, logic for configuration and readout, multiplexers, and analog monitors.

Each of the 122 anode channels, shown in Fig. 3, implements a low-noise charge amplifier with single-stage-compensated adaptive continuous reset [23] having charge gain of 48. The input MOSFET is a p-channel device optimized for 3 pF input capacitance [24], with gate size $\mathrm{L/W} = 0.36\ \mu$m/300 μm (technology is CMOS 0.25 μm) and biased at a drain current of about 100 μA, corresponding to 250 μW dissipated in the input branch. With a transconductance $\mathrm{g_m}$ ≈1.7 mS and a gate capacitance $\mathrm{C_g}$ ≈650 fF the input MOSFET contributes to the ENC with about 75 electrons rms at 3 pF input capacitance (assuming a high order shaper with 1 μs peaking time).

The voltage amplifiers adopted in the charge amplifier and shaper stages implement some new configurations. These configurations, shown in Fig. 4, aim to improving the performance while maintaining the power dissipation within specifications.

The input MOSFET $\mathrm{M_1}$ is followed by a dual-cascode stage $\mathrm{M_{C1}}$, $\mathrm{M_{C2}}$, which increases the amplifier's dc gain and lowers the impedance at the drain node of $\mathrm{M_1}$. The voltage drop across $\mathrm{M_{C1}}$ has negligible impact in our charge amplifier's configurations based on continuous reset. The typical gate width of $\mathrm{M_{C1}}$ is about one third of $\mathrm{M_1}$. We give details about this configuration elsewhere [25].

For voltage amplifiers that must provide negative swing at the output, the capacitor $\mathrm{C_A}$ was introduced. For negative output swings, the voltage at the gain node (drain node of the load $\mathrm{M_L}$) is slew-rate limited by the current in $\mathrm{M_L}$. When this occurs, the input voltage of the amplifier suddenly increases, and the drain voltage of the current source $\mathrm{M_S}$ falls. The capacitor $\mathrm{C_A}$ uses this decrease to send additional current to the gain node, thereby improving the performance for large signals. A typical value of $\mathrm{C_A}$ is about 1 pF.

The output stage consists of a source follower $\mathrm{M_F}$, $\mathrm{M_{FS}}$ assisted by its scaled-down replica $\mathrm{M_{Fa}}$, $\mathrm{M_{FSa}}$ and by a differential amplifier, generating a local feedback. The dc gate voltage of the source $\mathrm{M_{FS}}$ is forced to the gate voltage of $\mathrm{M_{FSa}}$. During transients, the gate voltage of $\mathrm{M_{FS}}$ is dynamically adjusted, increasing or decreasing the drain current so that the loaded output voltage follows its unloaded replica. A fast negative signal applied to the gate of $\mathrm{M_F}$ and $\mathrm{M_{Fa}}$ produces a differential signal at the input of the differential amplifier. As a consequence, the gate of $\mathrm{M_{FS}}$, which is connected to the output of the differential stage, moves in the positive direction. In this way the current in $\mathrm{M_{FS}}$ is dynamically increased and it is not limited by the dc bias value. This increased current allows a faster discharging of the output node with respect to the case of a traditional source follower without local feedback. The circuit works also for positive input signals. In this case the transistor $\mathrm{M_{FS}}$ starts to be switched off by the negative output of the differential stage. In this way a larger fraction of the current flowing in $\mathrm{M_F}$ is sent to the output. However, in this case, the advantage with respect to a simple source follower configuration is limited by the amount of the dc current flowing in $\mathrm{M_{FS}}$. In order to work properly, the time constants of the output node and unloaded replica must be properly set through their current and scaling factor. Typical currents through the $\mathrm{M_{FS}}$, $\mathrm{M_{FSa}}$, and differential stage are, respectively, about 20 μA, 1 μA, and 4 μA. A typical source follower scaling factor is 20. The network $\mathrm{R_{FC}}$, $\mathrm{C_{FC}}$, with typical values of 10 kΩ, 100 fF, provides compensation and bypasses the active loop at the highest frequencies.

The charge amplifier is followed by a 5th order shaper with complex conjugate poles, an adjustable peaking time (0.25 μs, 0.5 μs, 1μs, and 2 μs), and an output baseline stabilized with a Baseline Holder (BLH) [26]. It follows a discriminator with 4-bit trimmer, a peak and timing detector, and a Time-to-Amplitude Converter (TAC) (the duration of ramp is adjustable to 1 μs, 2 μs, 3 μs, and 4 μs). The amplitude of the pulse is measured and stored in an analog memory using a multi-phase peak-detection configuration [27]. The TAC converts the timing of the anode event into a voltage. The ramp starts at a trigger released by the peak detector at the time of the peak, and is stopped by an external trigger common to all TACs [28]. Section III has details of this timing method. The channel includes a mask function and a test capacitor connected to a test-pulse generator, common to all channels, whose amplitude is controlled by a 10-bit DAC. The shaped pulse from it can be routed to an auxiliary analog output (analog monitor). The entire channel is characterized by a gain of about 20 mV/fC (about 18 mV/fC at 0.25 μs peaking time) and dissipates about 1.35 mW.

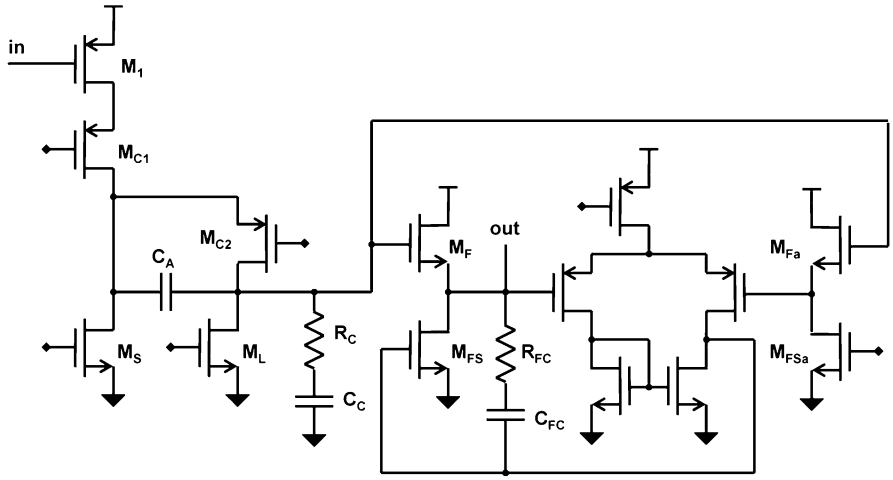

Fig. 4. Schematic of a voltage amplifier implementing some new configurations.

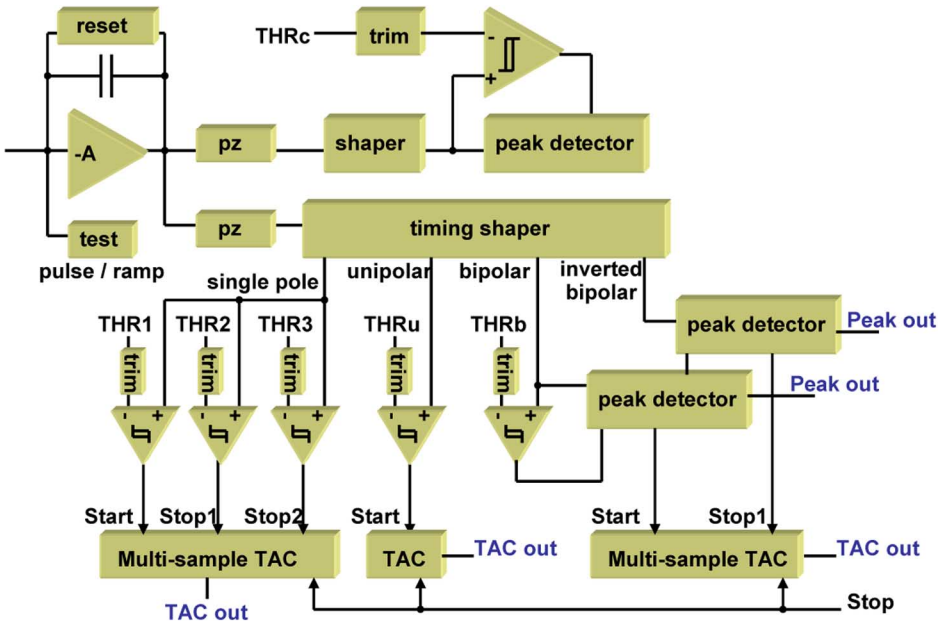

Fig. 5. Block diagram of the cathode channel.

Fig. 5 shows the cathode channel, which implements a low-noise charge amplifier with dual stage adaptive reset having total charge gain of 48. The input MOSFET is a p-channel device optimized for 6 pF input capacitance, with gate size $\mathrm{L/W} = 0.36\ \mu\mathrm{m}/600\ \mu\mathrm{m}$ and biased at a drain current of about 200 μA, corresponding to 500 μW dissipated in the input branch. With a $\mathrm{g_m} \approx 3.4$ mS and a $\mathrm{C_g} \approx 1.3$ pF, it contributes to the ENC with about 100 electrons rms at 6 pF input capacitance (assuming a high order shaper with 1 μs peaking time). The remainder of the channel splits in three sections providing, respectively, energy measurement, timing measurement, and a preamplifier monitor (the latter not shown in Fig. 5).

The cathode's energy section implements a 5th order shaper with complex conjugate poles and an adjustable peaking time (0.25 μs, 0.5 μs, 1 μs, and 2 μs), a BLH, a discriminator with 4-bit trimmer, and a multi-phase peak detector. The cathode's timing section includes a multi-stage shaper with four outputs: the first provides a replica of the charge preamplifier's output, the second a 3rd order unipolar-shaping with complex conjugate poles and an adjustable peaking time (100 ns, 200 ns, 400 ns, and 800 ns), while the third provides a differentiation on the unipolar shaping, meaning a bipolar shaping (peaking time about 50 ns, 100 ns, 200 ns, and 400 ns). The fourth output constitutes an inversion of the third output. These four outputs measure the timing of the cathode's signals via three different timing methods, discussed in detail in Section III. The timing circuits use discriminators with 4-bit trimmers, peak detectors and TACs (ramp durations adjustable to 1 μs, 2 μs, 3 μs, and 4 μs). The channel has a mask function and a test capacitor connected to a pulse or ramp generator, common to all channels, the amplitude of which is controlled by a 10-bit DAC. Test ramps can be generated with adjustable slope and duration, thus simulating actual cathode signals. For monitoring, the charge amplifier's voltage output is available through a dedicated output (preamplifier monitor). The shaped pulse from the energy and timing sections can be routed to the

auxiliary analog output (analog monitor). The whole channel is characterized by a gain of about 20 mV/fC for the energy section, and about 23 mV/fC and 15 mV/fC, respectively, for the unipolar shaper and bipolar shaper in the timing section; it dissipates overall about 5.25 mW.

The ASIC operates in two sequent phases, acquisition and readout, controlled by an external Low Voltage Differential Signal (LVDS) EN. The acquisition phase reads out and processes the signals from the sensor; the readout phase makes the measurements available to the external electronics for analog-to-digital conversion. In the former, EN high, all channels become sensitive to input events. When an event occurs and a first peak is found, the ASIC releases a LVDS flag, FL, and then the external electronics can stop acquisition by lowering the EN. This signal is used as stop trigger for all TACs. Having entered the readout mode, all analog outputs (energy and timing) from all channels are made sequentially available, with a LVDS clock CK, at two dedicated analog outputs.

The ASIC discriminates events based only on anode signals. Once this is enabled (with EN high), should an anode signal exceed the threshold, then the peak amplitude and timing measurements are enabled in all other anodes. The flag FL is released, after a delay of 200 ns, at the time the first peak is found. The anodes process the amplitude and timing of the highest peak (the peak detector has a single analog memory) until the acquisition stops (EN low). In one option, the timing can be measured only from the first peak; this choice option can be valuable for extracting timing information from inductions occurring in those pixels neighboring the ones above threshold. In another option, channels that did not exceed the threshold can be forced to store that amplitude at the time of the first above-threshold peak. This one can be useful to force the sampling of negative amplitudes that may result from induction in the pixels next to the ones above threshold [29], [30].

A cathode signal exceeding the threshold is always processed for peak amplitude and timing, but the event will not trigger the flag FL. The cathode will continue processing the amplitude and timing of the highest peak until the acquisition stops (EN low).

Except for the serial configuration signals, all the digital inputs and outputs are LVDS. The ASIC includes one test-pulse generator for the anodes and one test pulse/ramp generator for the cathode, controlled by independent LVDS clock signals and two 10-bit DACs. The common thresholds are controlled by four 10-bit DACs and a one 4-bit DAC. The temperature sensor is characterized by a nominal response of 1.52 V + 5.67 mV/°C. The outputs from the DACs and temperature sensor can be routed to the auxiliary analog output (analog monitor). The whole ASIC dissipates 250 mW, with an effective power per channel of about 2 mW. Constructed in CMOS 0.25 μm, the die, measuring 11.3 mm $\times$; 8.2 mm, has 208 input/output pads.

III. Timing Methods

An ionizing event produces electron-hole pairs in CZT material in an amount proportional to the energy of the event. Under the applied voltage, the electrons and holes move, respectively, from the point of interaction to the anodes and cathode. The currents induced in both are measured by the associated charge amplifier. Because the holes have poor transport properties, only the electrons effectively contribute to the currents, with the considered time constants.

The signal induced in the cathode, a planar electrode, starts at the time of interaction and stops when the electrons reach the anodes, to which the electrons travel at a speed that depends upon the applied voltage. Neglecting the holes, the duration of the induced signal depends on the applied voltage and depth of interaction: it is longer when the interaction is in the proximity of the cathode (since the electrons travel through the whole sensor), and declines to negligible values as the interaction occurs closer to the anodes. Consequently, for a given energy, the total induced charge is higher when the interaction occurs close to the cathode and decreases to negligible when the interaction is closer to the anodes. The voltage signal at the output of the charge amplifier, which is the integral of the induced current, is, to a first-order, a ramp with a slope proportional to the energy (i.e., to the total charge generated by the ionization) and duration proportional to the depth of interaction. For a given energy, the final amplitude of the ramp is proportional to the depth of interaction.

The signal induced in the anode is subject to the small-pixel effect [31]–[33]. Since it is distributed among all anodes and anodes-grid, it remains negligible until the electrons approach the anodes at a distance of about one pixel pitch. Then a strong current is induced in those anodes that collect the charge. The hole-induced signal remains small for every single pixel, because the holes move slowly towards the cathode or are trapped. Consequently, unlike the cathode, the total induced charge is, to a first order, independent of the depth of interaction and only depends on the event's energy. The voltage signal at the output of the charge amplifier is, to a first-order, a step with amplitude proportional to the energy, independent of the depth of the interaction. Compared to planar electrodes, the small-pixel configuration effectively makes the detector sensitive to only one kind of charges, the electrons.

In the absence of electron trapping, and assuming an ideal small-pixel effect, the total charge measured at the anode (or anodes) is proportional to the event's energy. Taking electron trapping and second-order small-pixel effects into account, then the anode signals show a non-negligible dependence on the depth of interaction that considerably affects spectral performance.

This dependence can be compensated for by measuring, for each event, both the amplitude of the signal at the anode and the depth of the interaction, and by applying to the amplitude the associated corrective coefficient. The depth of interaction can be extracted to a first order from the ratio between the amplitude of the cathode signal and the one of the anode (or sum of anodes). This approach is effective for ionizing events having a single point of interaction or involving only a few anodes. For events with multiple points of interaction or encompassing several anodes, the depth of each point can be more efficiently extracted from measuring the relative drift time associated with each anode signal, i.e., the delay from the time of interaction, measured on the cathode signal, to the time the electrons reach each anode. All these bi-parametric approaches afford correction coefficients for each volumetric pixel (voxel) in the sensor [20]–[22], [32].

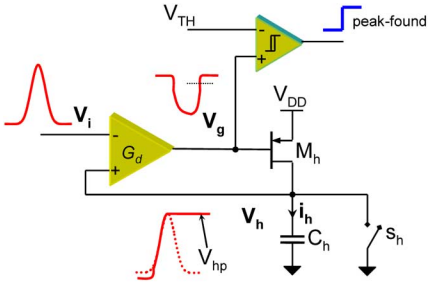

Fig. 6. Block diagram of the peak detector's circuit.

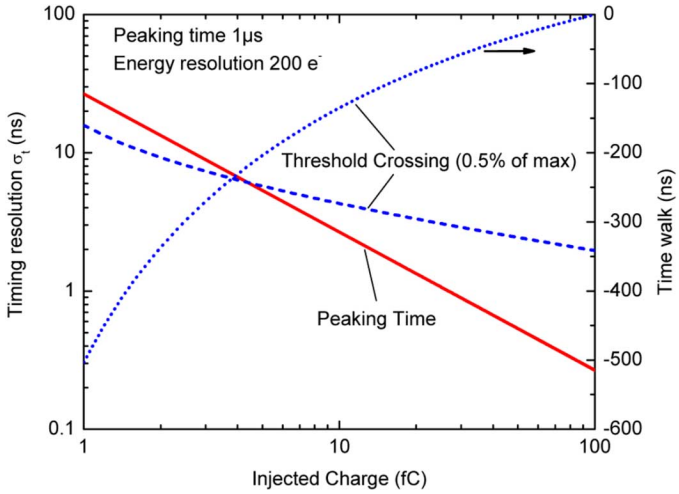

Fig. 7. Theoretical timing resolution from (1) assuming a unipolar shape with peaking time of 1 μs and energy resolution 300 electrons rms. The case of threshold crossing, along with the associated time walk, also is shown.

Techniques were implemented in the ASIC to accurately measure the timing of the anode and cathode signals.

The timing of the former is obtained, as anticipated in the previous Section, by measuring the peaking time of the anode-shaped pulse. In contrast to timing measured from the threshold crossing on unipolar pulses, this peaking-time method has the advantage of being, to a first order, independent of the amplitude. In principle, the timing of the peak-found signal of the peak detector circuit [27], shown in Fig. 6, is equal to the one of the zero-crossings on a bipolar pulse. The current flowing through the hold capacitor C_h during peak detection equals the derivative of the input pulse according to $i_h = C_h dV_i/dt$. When the signal V_i approaches the peak, the current i_h approaches zero, and the voltage, V_g, equals $V_{DD} - V_{THh}$. Immediately after the peak, the signal, V_i, starts falling and, due to the high gain, G_d, of the differential amplifier the output voltage, V_g, sharply increases towards V_{DD} crossing the comparator threshold, V_{TH}, set at a voltage $V_{DD} - V_{THh} < V_{TH} < V_{DD}$, where V_{THh} is the threshold voltage of the controlled current source M_h.

The timing resolution σ_t achievable with this method can be approximated with [34]

$$\sigma_t \approx \frac{\sigma_{ih}}{i_h'(\tau_{p0})} \approx \frac{i_{hp}}{Q}\frac{ENC_b(\tau_{pb})}{i_h'(\tau_{TH})} \approx \frac{ENC_b(\tau_p\eta_p)\tau_p\lambda_p}{Q\rho_p} \quad (1)$$

where σ_{ih} is the noise on the current signal i_h, and i_h' is the derivative calculated at the time, τ_{TH}, of the threshold crossing of the comparator, where $i_h(\tau_{TH}) = i_{hTH}$ then is the current. We note that i_{hTH} is set by the threshold V_{TH}, and, for τ_{TH} approaching the time τ_{p0} at which V_i peaks, it follows that $i_h'(\tau_{TH}) \approx i_h'(\tau_{p0})$. In (1), the noise σ_{ih} is assumed to be dominated by that on the shaped pulse, V_i, from the first front-end stage, and it is calculated in (1) as ENC_b multiplied by the gain from the signal charge Q to the current i_h in C_h (i.e., i_{hp}/Q, where i_{hp} is the peak value of i_h). Therefore, the term ENC_b is calculated assuming a bipolar shape (current i_h) with peaking time τ_{pb}. Normalized coefficients can be adopted [34], yielding the final expression in (1) that depends only on Q and the peaking time τ_p of V_i. For a 5th order shaper with complex conjugate poles, they are $\rho_p 3.65$, $\eta_p = 0.58$, and $\lambda_p = 1.58$ [34]. Assuming a unipolar pulse with peaking time 1 μs and resolution 200 e^- rms, the timing resolution σ_t from (1) can be plotted as done in Fig. 7. In the same figure, the resolution for threshold crossing on the same unipolar pulse is depicted, along with the associated time walk, assuming a threshold at 0.5% of the maximum amplitude.

The results in (1) and Fig. 7 assume there is a negligible contribution to the noise from the shaper, the peak detector, the comparator, and the downstream stages. In practice, overlooking these other contributions (as we partially did) can severely limit the timing resolution. Particular attention must be paid to the residual high-frequency noise components from the last stages of the shaper, and from the differential amplifier of the peak detector. The signal, i_h, decreases with the peaking time, and its slope i_h' (τ_{p0}) declines with the square of the peaking time. On the other hand, these noise components, along with their emphasis by the derivative, are, to a first order, independent of peaking time. The contribution to the timing resolution then is proportional to the square of the peaking time, and can be approximated with $\sigma_{ih\_hf}/i_h'(\tau_{p0})$, where σ_{ih_hf} is the corresponding rms current noise. A resistor placed in series with the capacitor C_h, to help stabilize the peak detector loop, also would filter part of such high-frequency noise. The noise from the comparator can be evaluated as σ_{vc}/ψ_{Vg}, where σ_{vc} is the rms voltage noise at its input, and ψ_{Vg} is the slope of V_g. The slope can be approximated from the Taylor series of the signal, $V_i - V_{ip}$, immediately after the peak, yielding $\psi_{Vg} \approx A \cdot \mathrm{sqrt}(2\, i_h'(\tau_{p0}) V_{ip}/C_h)$ where A is the difference voltage gain. Again, this contribution, usually small, is proportional to the square of the peaking time. Assuming that the timing signal is converted into a voltage using a TAC (as in our case), the series noise from the TAC and its readout can be approximated with $\mathrm{sqrt}(S_{iTAC} T_{TAC})/(\psi_{TAC} C_{TAC})$, where S_{iTAC} is the spectral noise power density of the current flowing into a capacitor C_{TAC} to generate the ramp, T_{TAC} is the ramp's duration, and ψ_{TAC} is its slope. The contribution from the downstream stages (e.g., the buffer, ADC) can be approximated with σ_{vro}/ψ_{TAC} where σ_{vro} is their rms input voltage noise.

For measuring the timing of the cathode signals, we established three different methods: preamplifier multi-threshold,

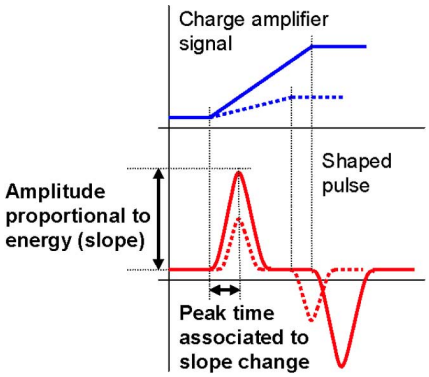

Fig. 8. Diagram illustrating the bipolar peaking time method for measuring the timing of cathode signals. Two cases are illustrated, differing in energy and depth.

unipolar threshold, and bipolar peaking time. All take into account the cathode signal's relatively long induction time.

The preamplifier multi-threshold method is performed directly on the output voltage of the charge amplifier (before the shaping). As discussed, the voltage signal at the output of the charge amplifier is, to a first order, a ramp whose slope is proportional to the energy, and duration to the depth of interaction. By measuring the timing of the crossing of three different thresholds [35] the slope of the signal (i.e., the energy) can be reconstructed, and also the timing at the departing point of the ramp (i.e., the time of interaction). This method still requires energy information from the anodes for those signals that cross only the first threshold. A drawback here is the poor noise filtering, limited to the one introduced by the parasitics in the charge amplifier. For slow signals, as in our case, the noise may easily dominate the signal.

The unipolar threshold method, frequently adopted by designers, consists of measuring the timing at the threshold crossing of a fast-shaped cathode signal. It necessitates having an additional fast shaper associated with the cathode channel. Since the time at the crossing of the threshold depends on the pulse's amplitude and induction time, this measurement exhibits considerable dependence on the energy and depth of interaction. Accordingly, it requires additional calibration based on the energy information from the anodes.

The bipolar peaking time method is based on measuring amplitude and peaking time of the cathode signal filtered by a fast bipolar shaper; hence, an additional fast shaper must be added to the cathode channel. Bipolar-shaped signals exhibit a unipolar response each time the slope of the charge amplifier voltage signal (i.e., the ramp) changes. The amplitude of the resulting unipolar pulse is proportional to the change in slope, and the timing is related only to the time of the change in slope. If the peaking time is small compared to the induction time, the shaped signal responds with a positive unipolar pulse when the ramp departs from the baseline, and with a negative unipolar pulse at the end of the ramp (Fig. 8). The amplitude of the positive pulse is proportional to the slope, and it provides a first-order measurement of the energy. The peaking time is associated with the time the slope changes providing, to a first order, a timing measurement independent of the energy and depth of interaction. For events with single point of interaction, the delay from the positive to the negative peak affords a first order value for the electron drift time (i.e., the depth of interaction). The ASIC measures amplitude and timing of both positive and negative pulses.

By directly measuring the drift time and energy without requiring the information from the anodes, the first and the last methods of cathode timing are expected to offer better overall performance. All three were designed to provide a timing resolution better than 20 ns for charges above 1 fC.

IV. Fabrication and First Experimental Results

We fabricated the first prototype of the ASIC, with a layout size of 11.3 mm $\times$ 8.2 mm, in a commercial CMOS 0.25 μm technology. Fig. 9 is a picture of the die. The 122 anode channels plus two cathode channels are symmetrically arranged with 62 inputs on the left, and 62 on the right. The bias and readout circuitry are in the center, the analog outputs at the bottom, and the digital interface at the top. The channels are, respectively, 100 μm $\times$ 5 mm and 200 μm $\times$ 5 mm for the anode and cathode. The total transistor count is about 300 000.

The ASIC was assembled as shown in Fig. 1(b) and (c), and was characterized without a sensor and, preliminarily, with a 121-pixel CZT sensor of $20 \times 20 \times 5$ mm^3. Fig. 10 plots the response of the anode channel to a 70 fC input charge for four peaking -time values. The baseline is about 245 mV.

Fig. 11 shows the ENC measured on cathode and anode channels as function of the peaking time, including the cases without a sensor, with the sensor unbiased and biased. The measurements were taken with a true rms voltmeter at the channel analog output, available through the monitor function. Spectral measurements with a test pulse and no sensor show an increase in the ENC of about 15%–20%, due to the noise from the peak detector circuit. In a revised version, we will consider reducing this contribution, mainly by optimizing the size of some components. This increase becomes negligible with the sensor connected.

An integral linearity error below $+/-0.3\%$ was measured for output signal amplitudes up to 2.25 V (including the $\approx$250 mV baseline), which corresponds to an input charge of 100 fC. A channel-to-channel dispersion of 5.2 mV rms and 1.5% rms (2% rms at 0.25 μs peaking time) were, respectively, measured on the baseline and gain.

The timing response of the anode channels was characterized, with the test pulse, in terms of resolution and time walk. Fig.12(a) shows the measured resolution as function of the injected charge for the four peaking times. Values below 700 ps were measured at a peaking time of 250 ns for charges above 30 fC, limited by the noise from the TAC and downstream stages. For low amplitudes, the resolution was considerably worse than the theoretical value (1). Further analysis revealed that the increase is dominated by the noise from the shaper and peak detector. For example, we observed that the resolution increases faster than the increase in peaking time (see Section III). Further confirmation comes from the additional measurements (open symbols) shown in Fig. 12(a), obtained by loading the input of the channel with a 3 pF capacitor. Preceding a factor-of-two increase in rms noise at the shaper's output, only a negligible increase is observed in timing resolution (compare

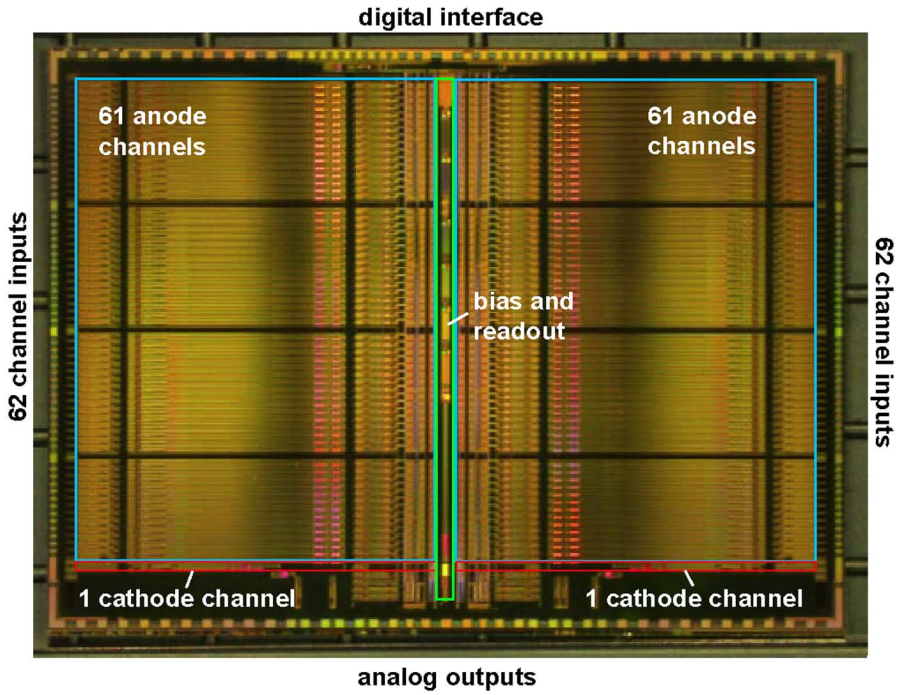

Fig. 9. Die photo, layout size 11.3 mm × 8.2 mm.

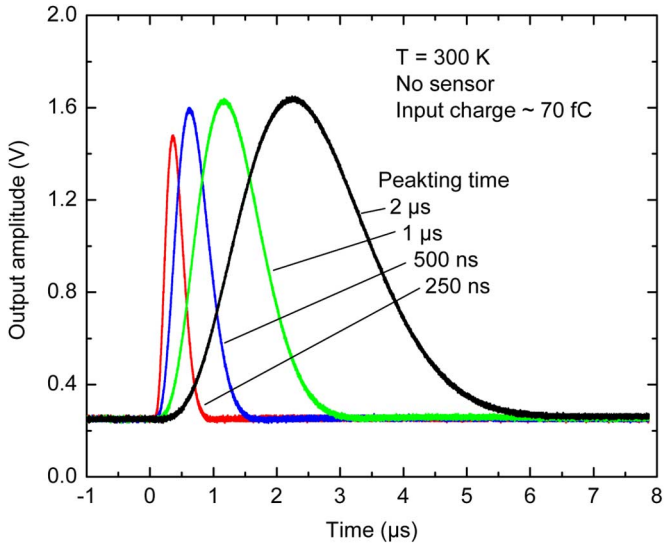

Fig. 10. Measured response to a 70 fC charge for the four peaking time values.

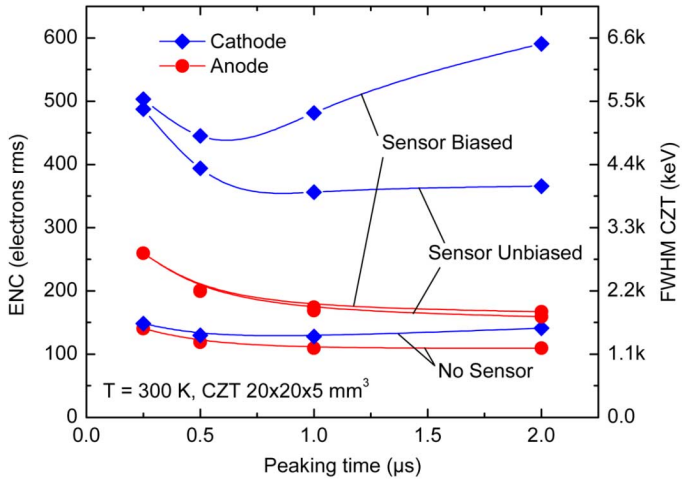

Fig. 11. Measured ENC versus peaking time.

the solid symbols to the open symbols), especially at longer peaking times. We have overlooked the impact of the noise from the shaper and peak detector on the timing resolution; it will be resolved in a later version, mainly by optimizing the size of some components.

Fig. 12(b) shows the measured time walk, referenced to the minimum value, as function of the injected charge for the four peaking times. The time walk is contained within 8 ns and 30 ns, respectively, at the shortest and longest peaking time. Almost identical results were obtained with the 3 pF capacitor at the input.

The timing response of the cathode channel was characterized using the three implemented methods: preamplifier multi-threshold, unipolar threshold, and bipolar peaking time. It was accomplished via injecting charge with the integrated test pulse and test ramp generators. The duration of the ramp was set to 500 ns and the injected charge was altered by changing the ramp's slope. The peaking time in the energy section of the cathode channel was set to 250 ns. The results from this characterization are reported here, while a comparative analysis will be published later.

For the preamplifier multi-threshold, Fig. 13(a) shows the measured resolution as function of the injected charge for the four peaking times. The solid symbols correspond to the 500 ns test ramp, while the open symbols represent the test pulse, for which only the first threshold was characterized.

The first threshold was set at about 0.5 fC, while the second and third thresholds were set to cover as much as possible the

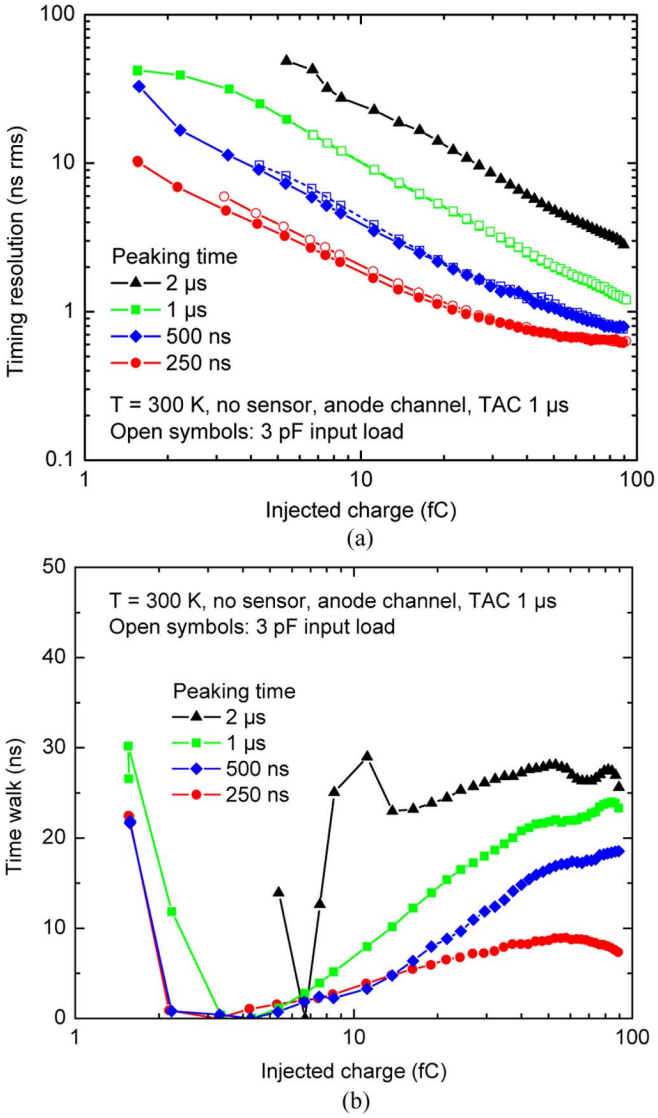

Fig. 12. Measured anode- channel timing resolution (a) and time walk (b).

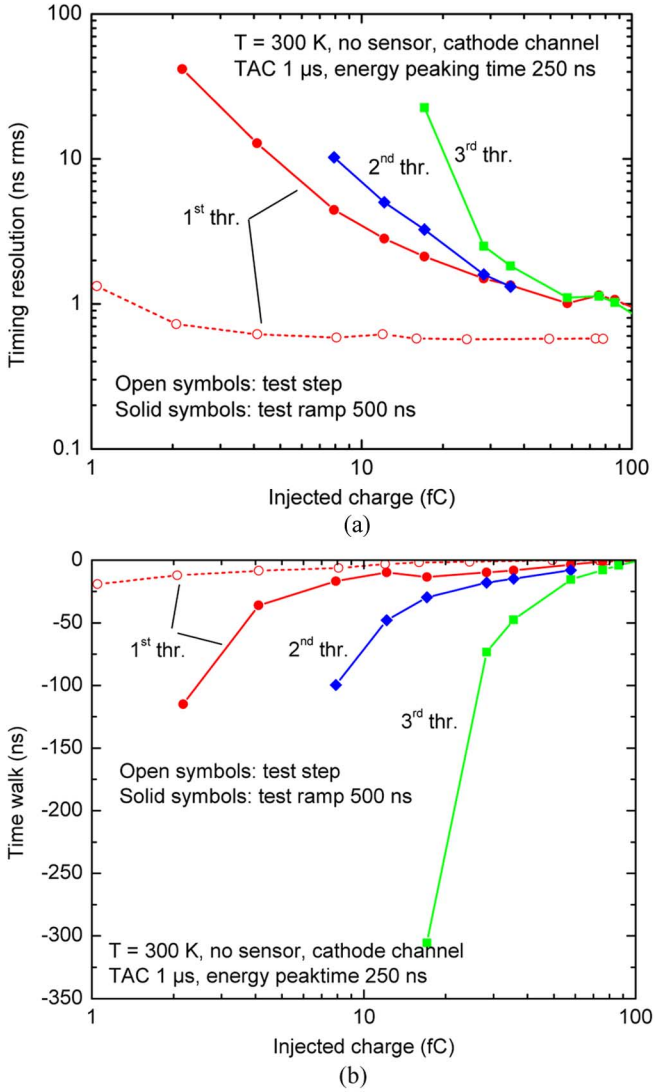

Fig. 13. Measured cathode timing resolution (a) and time walk (b) using the preamplifier multi-threshold method.

range of interest from 1 fC to 100 fC. We noted that, due to the poor signal level, a minimum detectable charge of 2 fC, 8 fC, and 17 fC for the first, second, and third threshold, respectively, were measured with the ramp. Excellent timing resolution was measured with the test pulse, while, in the most realistic case of the ramp, the timing resolution was below 20 ns for charges above 3 fC. Fig. 13(b) shows the corresponding time walk referenced to the maximum value, where, for the first threshold, values in excess of 100 ns were obtained for the test ramp. The difference in timing between the thresholds, properly calibrated, provides a measure of the slope of the test ramp that allows for timewalk correction. To have a difference available, at least two thresholds must be crossed, which in Fig. 14 means having a charge above 8 fC. For signals from the sensor, this also constitutes a direct measurement of the ionized charge (i.e., the energy). Suitable calibration can also provide the corrective coefficient for the time walk associated with the first threshold.

For a unipolar threshold set at about 0.5 fC, Fig. 14(a) shows the measured resolution as function of the injected charge for the four peaking times. The solid symbols correspond to the 500 ns test ramp, and the open symbols to the test pulse. In all cases, we measured a timing resolution below 20 ns. For the ramp, the impact of the reduced speed of the signal on the resolution is apparent. Fig. 14(b) shows the corresponding time walk referenced to the maximum value. Especially in the case of the ramp, the time walk can be as high as 400 ns for low charges.

For the bipolar peaking time, Fig. 15(a) and (b) show the measured resolution of the test ramp as function of the injected charge for the four peaking times. Due to a design error, for a given charge the pulse amplitude was proportional to the peaking time. This reduction in gain strongly affected the performance at low peaking times and will be corrected in a revision. Additionally, we saw considerable pick-up from the digital signals that prevented the characterization for charges below 4 fC. Finally, as in the case of the anode, the noise from the shaper and peak detector strongly affected these measurements, issues that also will be resolved later.

As discussed in Section II, the amplitude of the pulse from the peak detector, being proportional to the slope, is a measure

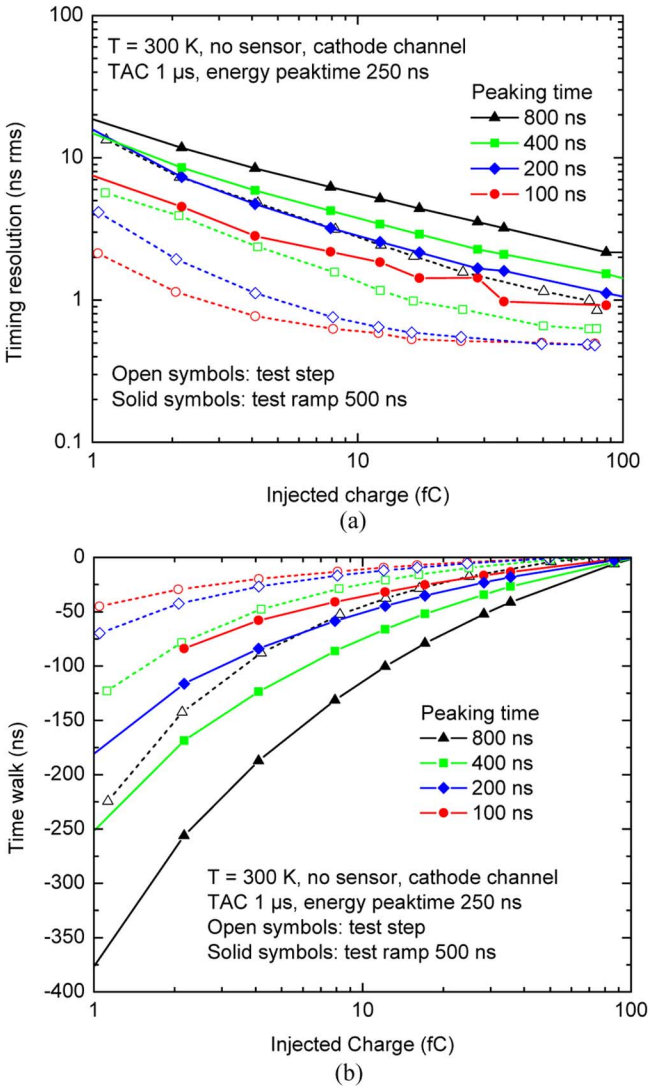

Fig. 14. Measured cathode timing resolution (a), and time walk (b), using the unipolar method.

of the energy. A resolution between 300 and 500 rms electrons was detected in the range of the four peaking times. Fig. 15(c) shows the measured peak amplitude on the positive- and negative-peaks as function of the injected charge (i.e., as a function of the slope).

Fig. 16(a) plots a single pixel spectrum from a ^{137}Cs source acquired at a peaking time of 1 μs. Fig. 16(b) shows the corrected spectrum using the cathode/anode ratio. The resolution is about 4.8 keV (0.72 %) at 662 keV, while the contribution from the electronics and leakage current is on the order of 2.1 keV.

V. Conclusions and Future Work

We demonstrated that the performance of our first prototype of an ASIC for 3D position-sensitive pixelated CZT sensors shows good agreement with the design in its functionality and energy resolution, where less than 200 electrons rms are measured with the sensor connected and biased. Margins for improvement were identified in the anode timing, where a final

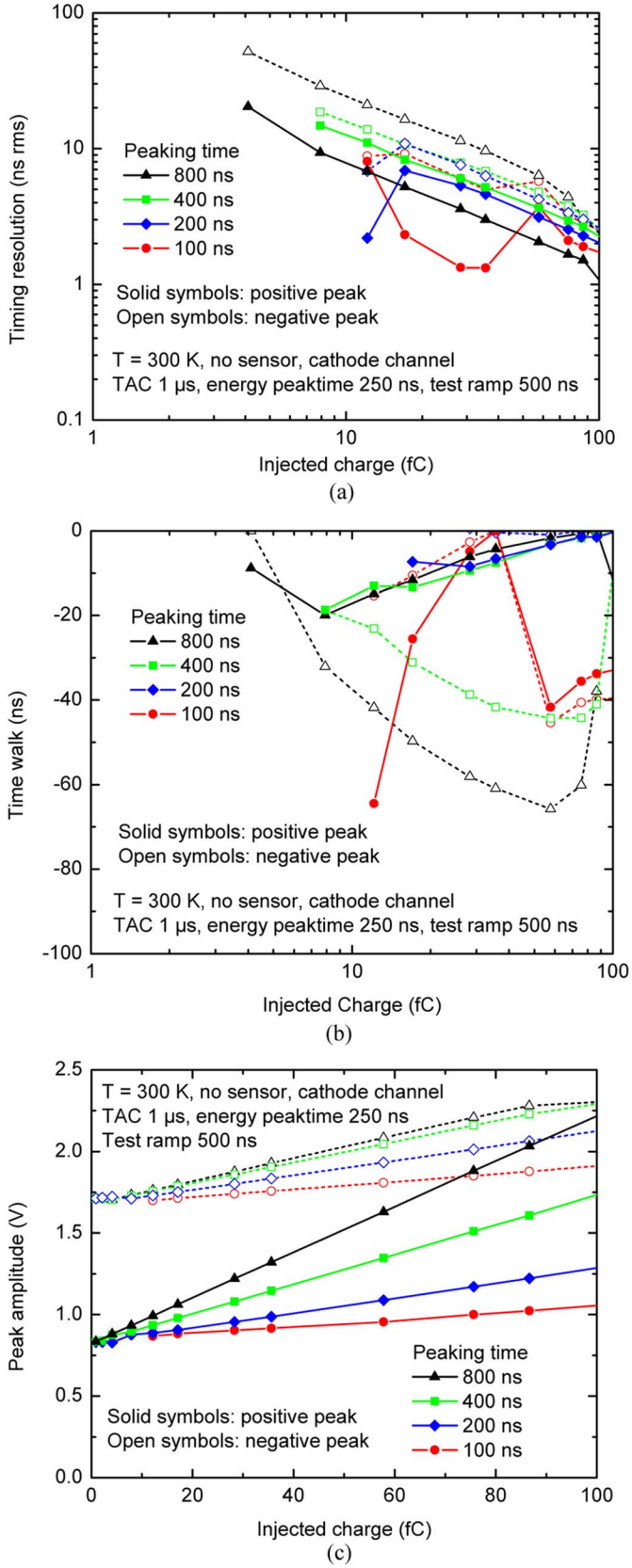

Fig. 15. Measured cathode timing resolution (a), time walk (b), and peak voltage (c) using the bipolar peaking time method.

resolution below 20 ns can reasonably be expected from a revision. Three different methods were characterized for resolving

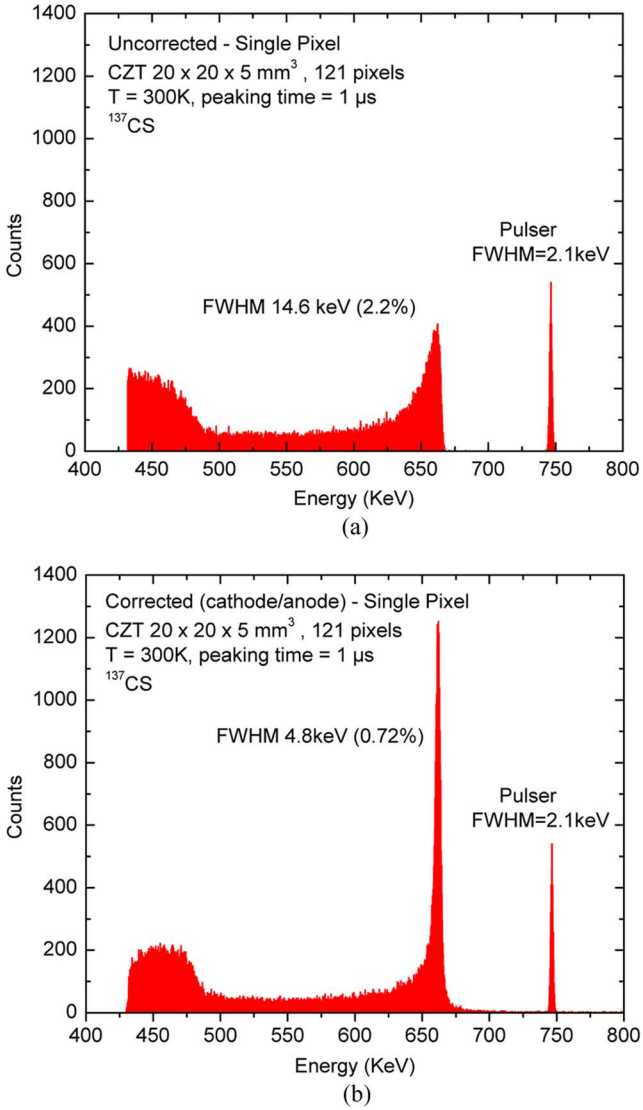

Fig. 16. Single pixel spectrum from a ^{137}Cs source: (a) uncorrected, and (b) corrected using the cathode/anode ratio.

cathode timing that will undergo further comparative analyses. Digital pick-up and low gain affect bipolar timing and will be resolved in a revision. Calibration routines also will be implemented using the integrated test pulse and test ramp. Finally, we will undertake extensive characterization with pixelated CZT sensors.

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