Published by IOP Publishing for Sissa Medialab

Received: *November 2, 2023*
Accepted: *February 12, 2024*
Published: *April 16, 2024*

Topical Workshop on Electronics for Particle Physics
Geremeas, Sardinia, Italy
1–6 October 2023

Integration of EDWARD readout architecture in full-field fluorescence imaging detector

D.S. Gorni,[a,1,*] **G.A. Carini**,[a] **G.W. Deptuch**,[a] **A. Kuczewski**,[b] **P. Maj**,[a] **S. Mandal**,[a] **G. Pinaroli**,[a] **A. Rumaiz**,[b] **D.P. Siddons**[b] **and N. St. John**[a]

[a] *Brookhaven National Laboratory, Instrumentation Division, Upton, NY 11973-5000, U.S.A.*
[b] *Brookhaven National Laboratory, National Synchrotron Light Source II, Upton, NY 11973-5000, U.S.A.*

E-mail: dgorni@bnl.gov

Abstract: Data bandwidth, timing resolution and resource utilization in readouts of radiation detectors are a constant challenge. Event driven solutions are pushing against well-trenched framed solutions. The idea for an asynchronous readout architecture called **EDWARD** (**E**vent-**D**riven **W**ith **A**ccess and **R**eset **D**ecoder) was presented at the TWEPP 2021 conference. Here we show the progress of our work which resulted in two chip prototypes. The first one, named 3FI65P1, is a full device with the analog pixel circuitry suited for full-field fluorescence imaging. It is already manufactured, and preliminary results are presented. The second chip, named EDWARD65P1, contains digital pulse generators with Poisson-exponential distribution in each pixel for extraction of the performance matrix of the EDWARD architecture alone.

Keywords: Digital electronic circuits; Electronic detector readout concepts (solid-state); VLSI circuits

*Corresponding author.

[1] This manuscript has been authored by employees of Brookhaven Science Associates, LLC under Contract No. DE-SC0012704 with the U.S. Department of Energy. The publisher by accepting the manuscript for publication acknowledges that the United States Government retains a non-exclusive, paid-up, irrevocable, world-wide license to publish or reproduce the published form of this manuscript, or allow others to do so, for United States Government purposes.

https://doi.org/10.1088/1748-0221/19/04/C04035

2024 JINST 19 C04035

Contents

1 Introduction

The **EDWARD** (**E**vent-**D**riven **W**ith **A**ccess and **R**eset **D**ecoder) readout architecture [1, 2] allows efficient readout of data from a chip with multiple data sources, such as pixelated detectors. The architecture is distinguished by working in a fully asynchronous manner, meaning the request for readout can occur at any time, and the arbitration between requests is devoid of priority. These features eliminate the need to use the frame clock to snapshot the state of the matrix, which would be necessary to avoid switching between channels during a readout [3]. This functionality of the EDWARD architecture is achieved thanks to arbitration based on a binary tree, the basic unit of which is an arbiter based on the Seitz' arbiter structure [4]. Other advantage of the EDWARD architecture is automatic synchronization to an external clock provided, for example, by an acquisition module, which allows the chip to send data out using a standard communication protocol.

2 3FI65P1 chip

The **3FI65P1** (**F**ull-**F**ield X-ray **F**luorescence **I**maging) ASIC was designed for the purpose of reading out signals that originate in interactions of X-ray photons in a pixelated Silicon sensor [5]. A microphotograph of the 3FI65P1 die is shown in figure 1. It is a square ASIC built in a 65 nm CMOS process with all I/O wire-bonding pads for analog and digital signal, needed to operate the ASIC, grouped along one side of the die and an array of 32 × 32 octagonal with a bump-bonding pads for connecting to a pixelated sensor. The ASIC features a matrix of 32 × 32 pixels laid out on a square floorplan with a pitch of 100 µm. The matrix of pixels is built in a modular fashion with 16 groups, laid out in an array of 4 × 4 groups, each consisting of 64 pixels, where, in turn, the pixels in the group are arranged in an 8 × 8 pixel matrix.

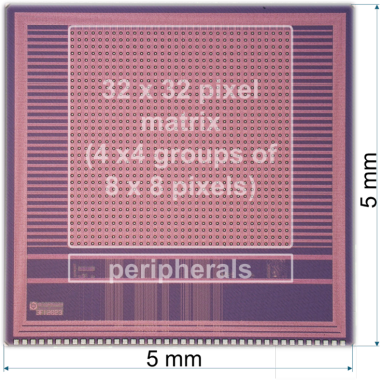

Figure 1. A microphotograph of the 3FI65P1 ASIC with the locations of the matrix of pixels and the peripheral circuitry together with the dimensions of the ASIC marked.

3 CTR platform

The digital portion, implemented in the integrated circuit 3FI65P1, primarily makes up the **CTR** (**C**onfiguration-**T**estability-**R**eadout) platform, in which configuration, testability, and readout elements intertwine to intermesh and work effectively together. To achieve this morphism effect, CTR components have been implemented from a single, fully parameterized RTL code. The CTR logic was synthesized and implemented using CAD tools what was of paramount importance for portability of the developed solution. The CTR logic was laid out both within the analog islands in a group and between different groups within the matrix. The main elements of the CTR platform are in the group logic space (reaching the density of about 84%), while the space between groups mainly contains only a part of the arbitration tree between groups (placed and routed at lower density of about 2%) and the shared data buses. The configuration of the pixels can be set by a digital interface, allowing bidirectional communication with the ASIC. This interface is compatible with the I2C standard externally and forks into a proprietarily developed **SPB** (**S**erial-**P**arallel **B**us) interface inside the chip. There are 8 bits of data, one SYNC line and one STROBE line that form the internal SPB that reaches each pixel. One of these configuration settings related to the EDWARD readout interface is, for example, that a set pixel may start requesting to be read out regardless of the **AFE** (**A**nalog **F**ront-**E**nd) [6] state. Exemplary waveforms, carrying out commands on the I2C's SCL and SDA lines used to change configuration are shown in figure 2. The sequence consists of the START symbol, chip address with R/W bit, group address and, finally, pixel address, followed by three groups of the actual configuration bits and one group of dummy data and the STOP symbol.

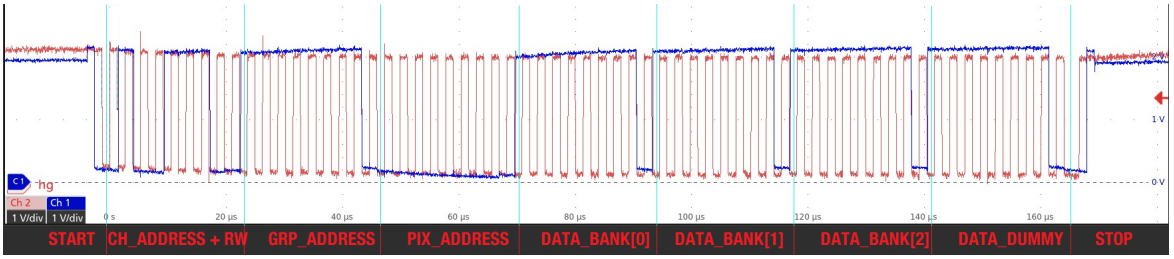

Figure 2. Exemplary I2C command waveforms on the SCL and SDA lines used for slow control.

2024 JINST 19 C04035

The CTR platform is extremely modular and allows for easy scaling. Its simplified block diagram is shown in figure 3. All groups are linked onto a common 14-bit-wide digital data bus, through which the addresses of pixels, retrieved using the EDWARD protocol, are transmitted. Furthermore, an individual analog line is utilized to concurrently deliver analog values representing peak amplitudes of analog signals from an extremum detector within an AFE block, in tandem with the pixel hit addresses. The digital data is serialized and sent off-chip. Serialization is performed based on an externally supplied clock with the nominal frequency of 250 MHz. The chip features a built-in clock divider by 14 that acts as a serializer frame clock and determines time intervals within which individual pixels can possess access to the shared data transmission resources as orchestrated by the EDWARD protocol. In summary this clocking scheme of the serializer yields the pixel data readout rate of 17.86 MHz.

4 EDWARD65P1 chip

The EDWARD65P1 prototype is based on the skeleton of the 3FI65P1, maintaining its dimensions. In this prototype the AFE circuitry is replaced by logic, which block diagram is depicted in figure 4. It contains a pulse generator with the Poisson-exponential distribution [7]. This structure allows even better study of the temporal properties of the EDWARD architecture — timing resolution, delay, maximum acceptable rate, and the signal integrity of the received data thanks to the ability to programmatically change the rate at which readout requests are generated. Simulation results for such an event generator are shown in figure 5. It shows the effect of the event generation rate on the readout delay, defined as the time from the readout request to the latching of the event information in the peripheral part of the system. The delay is illustrated in the form of histograms:

- When only one pixel is active (figure 5a), the readout delay has a uniform distribution,
- When the generation rate is relatively low (compared to the readout rate) (figure 5b), the data is read out from the pixel with the first active acknowledgement generated, but sometimes the pixel has to wait for servicing of other requesting pixels,
- When the token generation rate increases (figure 5c), the average readout delay increases due to more pixels simultaneously waiting to be read out,
- In the extreme case (figure 5d), the readout delay seeks a limit equal to the frame readout, i.e., each pixel must wait for all other pixels to read.

5 Testing

The digital part of the 3FI65P1 ASIC underwent testing to confirm the functionality of the CTR platform and to validate the EDWARD protocol's capability to retrieve addresses of pixels requesting being readout without any loss. The testing involved configuring of the chip to set those pixels that should be requesting readouts, triggering of the programmed pixels for requesting readouts using an external, global for the 3FI65P1 ASIC trigger, reading the serial data from the acquisition system, and repeating the steps several times, each time with the new configuration. Each pixel programmed to request its readout can be read out one time, and needs to be every time, newly triggered by the external trigger to request its readout again. The programming of configuration of the pixels was managed by software written in LabView and the communication with the 3FI65P1 ASIC was handled

2024 JINST 19 C04035

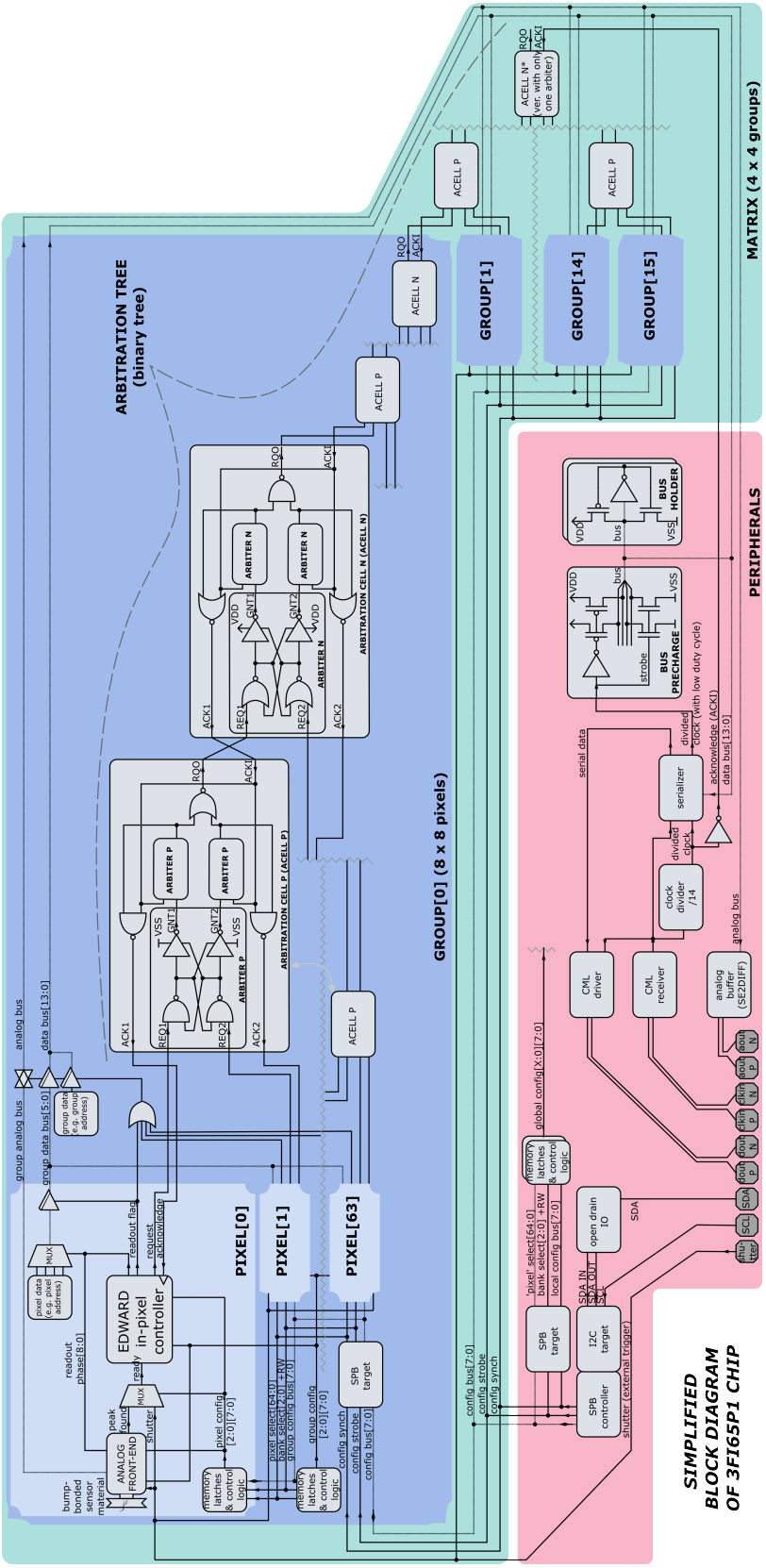

Figure 3. Simplified block diagram of the 3FI65P1 showing the elements of the CTR platform.

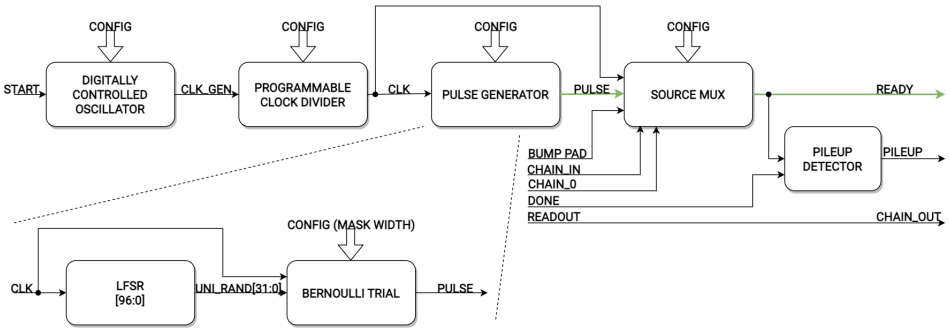

Figure 4. Block diagram for the signal generator implemented in the EDWARD65P1 chip.

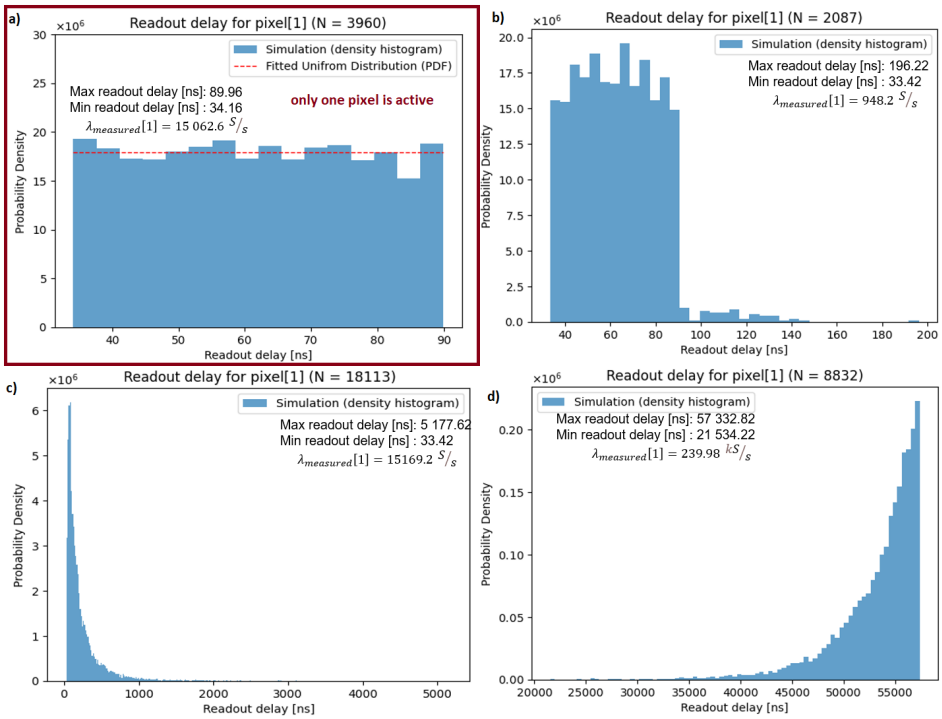

Figure 5. Histograms of readout delay for different values of event generation rates λ (a) when only one pixel generates events (b) λ is low compared to the readout clock frequency ($f_{\text{clk}} = 17.86\,\text{MHz}$) (c) λ is comparable to f_{clk} (d) λ is high compared to f_{clk}.

by the sbRIO controller. Due to the simplicity of the testbench, the clock supplied to the circuit had frequency of 20 MHz. Each pixel was assigned a predetermined non-zero value stored in software with a maximum value of 255. The number of readouts for each pixel is shown as an intensity map in 6. First it is given as intended in the software in figure 6a, and then, in figure 6b, the result of the performed readouts is shown. Before each trigger, the software-stored value of the counter for each pixel was decremented, and zero-value pixels were not any more programmed to be present in the readouts. The performed test allowed testing of all elements of the CTR platform, i.e., sending configurations, testing with an external trigger, and checking data integrity in the readout using the EDWARD protocol. The number of readouts from pixels fully matches the pattern programmed to all the pixels in the 3FI65P1 ASIC, i.e., no data loss or unexpected readouts were observed.

2024 JINST 19 C04035

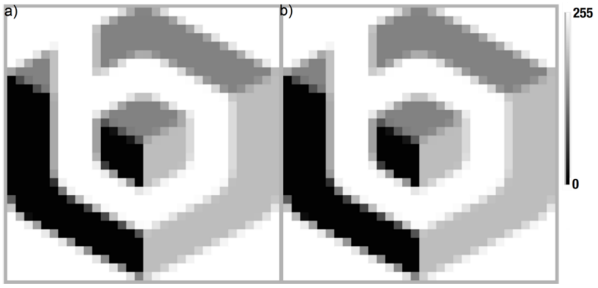

Figure 6. The number of readouts for all pixels represented in a form of an intensity map a) as programmed using the I2C-SPB interface b) as actually read out from the pixels; no difference between them is observed.

6 Summary

The results showed here — both the simulations for the EDWARD65P1 chip from the previous report and the measurements for the 3FI65P1 chip in the current report solidify the EDWARD protocol as viable, and the first in the community, preserving data integrity, truly event-driven readout. The successful operation of the designed readout architecture was shown and timing latency with its stochastic dependence on the event generation rates was assessed. The use of the proposed architecture in the next generation of chips will allow not only to reduce power consumption by operating based on the event driven principle, but also to obtain much higher temporal resolution of the received data by getting rid of the need for frame readout. The latter property of the chip may be particularly useful for the new detector for the future EIC (Electron-Ion Collider).

References

[1] D.S. Gorni et al., *Event driven readout architecture with non-priority arbitration for radiation detectors*, 2022 *JINST* **17** C04027.

[2] D. Gorni, G. Deptuch and S. Miryala, *Event-driven readout system with non-priority arbitration for multichannel data sources*, International application published under the Patent Cooperation Treaty (PCT), October 2022.

[3] P. Yang et al., *Low-power priority Address-Encoder and Reset-Decoder data-driven readout for Monolithic Active Pixel Sensors for tracker system*, *Nucl. Instrum. Meth. A* **785** (2015) 61.

[4] C.L. Seitz, *Ideas about arbiters*, Lambda (1980), pp. 10–14.

[5] D.P. Siddons et al., *A coded aperture microscope for X-ray fluorescence full-field imaging*, *J. Synchrotron Radiat.* **27** (2020) 1703.

[6] G. Pinaroli et al., *Development of small pixel CZT detectors for future hard x-ray missions*, *Proc. SPIE* **12678** (2023) 126780P.

[7] A. Veiga and E. Spinelli, *A pulse generator with poisson-exponential distribution for emulation of radioactive decay events*, in the proceedings of the *2016 IEEE 7th Latin American Symposium on Circuits & Systems (LASCAS)*, Florianopolis, Brazil (2016), p. 31–34 [DOI:10.1109/LASCAS.2016.7451002].

2024 JINST 19 C04035