The need for such a facility at BNL:

With new and future facilities and experiments in photon science, nuclear-, particle- and astro-physics, very challenging, innovative and sophisticated detectors will be needed, beyond the scope of what is commercially available, and only a dedicated facility such as the BNL Semiconductor Detector Development and Processing Laboratory (SDDPL) can provide necessary solutions.
**Brookhaven National Laboratory’s Semiconductor Detector Development and Processing Lab (SDDPL)** is a unique facility that has been developing detectors for more than 20 years, serving the scientific community in the United States and abroad. Detectors developed and fabricated in the Instrumentation Division have been used in nuclear and high energy physics, photon (materials and life) science and experiments for X-ray astronomy.

The 500 sq ft Class-100 cleanroom supports detector and monolithic JFET technology in 4” and 6” high resistivity (≥ 4000 Ω-cm) silicon (Si) wafers.

SDDPL is staffed by 1 Ph.D. and 1 Professional from Instrumentation, 1 Ph.D. from NSLS and 1 Professional from Physics.

**National Lithography and Processing Lab (SDDPL)** is a unique facility that has been developing detectors for more than 20 years, serving the scientific community in the United States and abroad. Detectors developed and fabricated in the Instrumentation Division have been used in nuclear and high energy physics, photon (materials and life) science and experiments for X-ray astronomy.

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**Detector-ASIC Integration**

Specialized wire-bonding techniques are often required in order to satisfy physics requirements of the detector assembly. For example, extremely long bonds as illustrated in the adjacent figure, or bonding between different levels of a multi-layer support stack. Again, close collaboration between the engineer and the bonding specialist is essential. All of these operations involve unprotected detectors and Application Specific Integrated Circuits (ASICs) and hence should be performed in a clean environment (Class-100), unlike conventional electronics assembly.

To arrive at a complete detector system it takes about 12 to 18 individuals with different expertise.

**Commercial Fabrication vs. In-house Fabrication**

**Yield**:

Typical Integrated Circuit (IC) fabrication consists of a wafer with hundreds or thousands of identical devices. It is acceptable for these foundries to have defects spread over the entire area of the wafer, which results in an acceptable 80 to 90% yield.

In detector fabrication, a detector can occupy an entire wafer and in some cases even a single defect can render the entire detector unusable, i.e., yield of 0%.

It is not possible to fabricate wafer-scale devices in a conventional semiconductor foundry, since their technology involves masks made on thin reticles typically 20mm x 20mm. This is, therefore, the maximum size device which can be lithographed.

Modern foundries base their production on 8”, 10” or 12” diameter wafers. The high-purity material we need is not available in these sizes. The maximum size available is 6”. This effectively excludes us from using such foundries.

**Use of Dedicated Detector Lab vs. Multi-User Clean Room Facilities**

Dedicated to high resistivity silicon wafers:

A typical integrated circuit foundry, or a user facility, processes mainly low resistivity silicon wafers where devices are formed only in the top few microns of silicon from the wafer surface. The wafer bulk has no active electronic components.

In detector fabrication, the entire volume of the wafer is required. A gettering of defects in the entire wafer is implemented in the beginning of detector fabrication. Although this high resistivity starting material is remarkably pure, it is still necessary to reduce the impurity levels even further. This is achieved by high-temperature processes performed under the cleanest possible conditions to avoid introducing further contaminants. The maintenance of high quality/high resistivity, no contamination, and no defects is carried out during the entire detector fabrication run.

As an indication of the difference in importance of this property between ourselves and industry, typical carrier lifetime in a CMOS structure is of the order of microseconds. In a good detector it is expected to be in the millisecond range, one thousand times better than commercial production. Obviously, in a multi-user, multi-purpose cleanroom in which a wide range of different materials are permitted, such an improvement will not be possible. In a commercial foundry, this process is simply not available since more economical processes suffice for their purpose.

**Cross-contamination**

Many different/unknown samples and various incompatible materials are typically used in a multi-user clean room facility fabrication process, which will certainly introduce contaminations and impurities to Si wafers via cross-contamination. This is absolutely unacceptable to the detector fabrication.

In detector fabrication at BNL, only high quality, high resistivity Si wafers and Al metal are used in the detector processing facility, which makes the fabrication environment well contained and reduces the susceptibility for cross-contamination.
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Simulation and Design
Dedicated software for 2-D and 3-D simulation of semiconductor processing and devices is used for implementing new concepts in fabrication and design. The close collaboration of physicists and engineers is vital for making new ideas a reality for specific experiment needs. A good simulation will prevent some potential problems in the actual detector processing and provide insurance for a good detector fabrication run.

Lithography masks are made using various CAD tools after exhaustive simulations. Close collaboration and frequent feedback between the physicists, engineers and lithography mask designers are crucial for a successful detector fabrication run.

Fabrication
The majority of steps required for the fabrication of the detectors are performed in-house to guarantee the quality and repeatability of a very unique process. In fact, detector fabrication requires the strictly controlled environment of a typical integrated circuit foundry together with the flexibility of a pure R&D lab where the risk of pursuing novel approaches for fabrication can be taken. A modern detector is typically a double-sided device where the full detector thickness (200-600 μm) of the wafer, as well as the majority of the wafer area (typically ≥ 36 cm²), constitute the active medium for interaction with the radiation. The integrity of these features at micron levels must be maintained over such a large area.

This implies that the high quality and high resistivity silicon wafers are used to obtain detection sensitivity throughout the full detector thickness at a reasonable operating bias voltage (∼200 volts). In addition, the wafer resistivity must be maintained during the entire detector fabrication. Any contamination in a processing step among a typical total of more than 150 steps will compromise the wafer quality and resistivity, and therefore the detector quality. Furthermore, rigorous inspections have to be made after each lithography step (among a typical 8-14 photo lithography steps) to ensure that no defects will be introduced over the entire detector area.

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