WORKSHOP #9

Advanced Metrologies for Addressing Critical Microelectronics Challenges

Chang-Yong Nam (CFN), Yong Chu (NSLS-II), and Gabriella Carini (Instrumentation Division)

Microelectronic devices are vital to every aspect of our lives, economy, and national security. For the past six decades, Moore's law has driven a rapid reduction of semiconductor device size down to single-digit nanometers, enabling unprecedented increase in performance and energy efficiency of microelectronic devices and computing. However, these transformative devices are now facing tremendous technical and economic challenges, limited by quantum mechanical limit, ever-increasing complexity in device structures and fabrication processes, and traditional von Neumann computing architecture incapable of delivering the sustainable high performance and energy efficiency direly needed in the near future. NSLS-II and CFN, as national user facilities and being located near the regional microelectronics industry hub, are uniquely positioned to contribute to the microelectronics research community and industry by providing unique, state-of-the-art resources well suited to addressing important materials and metrology challenges in microelectronics device development and engineering. Instrumentation Division has complementary microelectronics expertise that encompasses design and development from device to circuits and application, particularly in non-conventional environments. The workshop targets laying the foundations for these potential collaborations by inviting relevant academic, industrial, and facility experts, identifying key scientific and technological challenges NSLS-II and CFN can address, and potential investment to further enhance required capabilities at BNL.

Start Time (ET)	Title	Speaker (Affiliation)
12:30 pm	Opening remark	
12:30 pm – 01:10 pm	Keynote: Albany Nanotech and Microelectronics Challenges in the Next Decade	Satyavolu Papa Rao SUNY Polytech/NY CREATES
01:10 pm – 01:20 pm	NSLS-II Overview	Yong Chu NSLS-II/BNL
01:20 pm – 01:30 pm	CFN Overview	Chang-Yong Nam CFN/BNL
01:30 pm – 01:40 pm	Instrumentation Division Overview	Gabriella Carini Instrumentation Division/BNL
01:40 pm – 01:50 pm	Break	
01:50 pm – 02:20 pm	Advanced Packaging Architectures for Heterogeneous Integration	Ravi Mahajan Intel

02:20 pm – 02:50 pm	Metrology Challenges for Next-Generation Semiconductor Manufacturing	Daniel Schmidt IBM Albany
02:50 pm – 03:20 pm	Microelectronics Metrology at NIST	Joseph Kline NIST
03:20 pm – 03:30 pm	Group Photo; Break	
03:30 pm – 04:00 pm	X-ray Tomography of Integrated Circuits	Michael Sutherland Defense Microelectronics Activity (DMEA)
04:00 pm – 04:30 pm	Harnessing Synchrotrons to Accelerate the Development of High NA EUV Lithography	Patrick Naulleau Lawrence Berkeley National Lab
04:30 am – 04:50 pm	Novel Full-Field Imaging Spectrometers on NIST NSLS-II Beamline 7ID	Edward Principe Synchrotron Research Inc.
04:50 pm – 05:20 pm	Panel Discussion	
05:20 pm	Workshop adjourns	

Invited Speaker Bio-Sketch

Satyavolu "Pops" Papa Rao serves as the Vice President for Research for NY CREATES. For more than two decades, Pops has forged a path as a sought-after technical leader in advanced electronics and materials. Today, much of his research is focused on quantum technologies, specifically the fabrication of high-performance superconducting qubits using 300mm scale advanced processes, single-flux-quantum logic circuits, superconducting optoelectronics for neuromorphic computing, and AlN-based electrooptic integrated circuits. Prior to joining the NY CREATES team, Pops served as the Director of Process Technology for SEMATECH in Albany. His tenure at SEMATECH was preceded by technology leadership positions, including in advanced CMP processes, Si solar cells with all-plated copper front-grid metallization, and nano-structures for DNA nucleotide recognition at IBM Research and on process R&D for memory and logic devices for Texas Instruments. Pops obtained his Bachelor of Technology in Metallurgical Engineering from IIT-Madras, India, and his Ph.D. in Electronic Materials from MIT in 1996.

Ravi Mahajan is an Intel Fellow responsible for Assembly and Packaging Technology Pathfinding for future silicon nodes. Ravi also represents Intel in academia through research advisory boards, conference leadership and participation in various student initiatives. He has led Pathfinding efforts to define Package Architectures, Technologies and Assembly Processes for multiple Intel silicon nodes including 90nm, 65nm, 45nm, 32nm, 22nm and 7nm silicon. Ravi joined Intel in 1992 after earning his Ph.D. in Mechanical Engineering from Lehigh University. He holds the original patents for silicon bridges that became the foundation for Intel's EMIB technology. His early insights have led to high-performance, cost-effective cooling solutions for high-end microprocessors and the proliferation of photo-mechanics techniques for thermo-mechanical stress model validation. His contributions during his Intel career have earned him numerous industry honors, including the SRC's 2015 Mahboob Khan Outstanding Industry Liaison Award, the 2016 THERMI Award from SEMITHERM, the 2016 Allan Kraus Thermal Management Medal & the 2018 InterPACK Achievement award from ASME, the 2019 "Outstanding Service and Leadership to the IEEE" Awards from IEEE Phoenix Section & Region 6 and most recently the 2020 Richard Chu ITherm Award and the 2020 ASME EPPD Excellence in Mechanics Award. He is one of the founding editors for the Intel Assembly and Test Technology Journal (IATTJ) and currently VP of Publications & Managing Editor-in-Chief of the IEEE Transactions of the CPMT. He has long been associated with ASME's InterPACK conference and was Conference Co-Chair of the 2017 Conference. Ravi is a Fellow of two leading societies, ASME and IEEE. He was elected to the National Academy of Engineering in 2022 for contributions to advanced microelectronics packaging architectures and their thermal management.

Daniel Schmidt is a Senior Engineer at IBM Research in Albany, NY and leads optical metrology developments for next generation semiconductor manufacturing. He received his undergraduate degree in Microsystems Technology in Germany and earned a PhD in Electrical Engineering from the University of Nebraska-Lincoln in 2010. After three years of postdoctoral research, Daniel accepted a position as Senior Research Fellow at the National University of Singapore. In 2016, he left academia to start an industry career at GlobalFoundries before joining IBM Research in 2018. Daniel is the author or co-author of more than 100 conference papers, 60 journal articles, three book chapters, and currently serves as a committee member and session chair at SPIE.

R. Joseph Kline leads the Metrology for Nanolithography project at NIST and investigates X-ray based dimensional metrology of nanostructures. He received his Ph.D. in Materials Science and Engineering at Stanford University. He has published more than 100 articles, given more than 50 invited presentations,

and has received awards including the Presidential Early Career Award for Science and Engineering, the Department of Commerce Gold Award, and the Arthur S. Flemming Award.

Michael Sutherland has been working at Defense Microelectronics Activity for the last seven years developing capabilities to image large areas of integrated circuits destructively using an SEM and non-destructively using X-ray tomography. He has partnered with beamline FXI-18 at NSLS-II over the last two years to develop the software to take thousands of X-ray tomographies in a large mosaic at a time. The data is streamed using Tiled to a cluster computer for filtering, alignment, reconstruction, and analysis. The current goal of the project is to validate an integrated circuit against a known design file to verify that it was manufactured correctly.

Patrick Naulleau received his B.S. and M.S. degrees in electrical engineering from the Rochester Institute of Technology, Rochester, NY, in 1991 and 1993, respectively. He received his Ph.D. in electrical engineering from the University of Michigan, Ann Arbor in 1997 specializing in optical signal processing and coherence theory. In 1997 Dr. Naulleau joined Berkeley Lab on the EUV LLC program building the world's first EUV scanner. From June 2005 through March 2008, Dr. Naulleau additionally joined the faculty at the University at Albany, SUNY as Associate Professor, also concentrating in the area of EUV lithography. In April 2010 Dr. Naulleau took the position of Director of the Center for X-ray Optic at Lawrence Berkeley National Laboratory. Dr. Naulleau has over 390 publications as well as 19 Patents and is a Fellow of OSA (now Optica) and SPIE.

Edward L. Principe obtained a Ph.D. in engineering science from The Pennsylvania State University and MSME and BSME from University of Central Florida. He is founder and President of Synchrotron Research Inc., a designer and manufacturer of imaging NEXAFS tools. He has worked for more than 22 years in the area of instrument development for both ultrahigh-vacuum and high-vacuum microscopy and spectroscopy equipment. Dr. Principe has been involved in the advanced application of FIB systems in combination with Auger electron spectroscopy, time-of-flight SIMS, energy-dispersive spectroscopy, and a variety of FIB-based 3-D tomographic methods. His industry experience in advanced materials characterization includes FIB, FE-SEM, HR-TEM, XPS, Auger and synchrotron methods for general materials research and the semiconductor industry. Previous employment includes working 7 years for Carl Zeiss NTS as a Principal Scientist in the area of FIB-SEM, 5 years as FIB-SEM Product Manager for Tescan USA and 3 years as failure analysis Technical Staff for Applied Materials (FIB-Auger, defect-review tool).